Cyclone FPGA Family

ES-CYCFPGA-1.3 Errata Sheet

Introduction

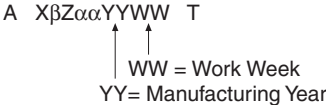
This errata sheet provides updated information on Cyclone® devices. This document addresses known issues and includes methods to work around the issues.

Power-Up Current

Altera has identified a silicon issue affecting Cyclone® EP1C6 devices. The EP1C6 engineering sample (ES) and production devices can require up to 1.2 A of current on the V_{CCINT} voltage supply to successfully power up. The duration of the I_{CCINT} power-up requirement is dependent on the V_{CCINT} voltage supply rise time. The power-up current consumption drops when the V_{CCINT} supply reaches approximately 0.75 V. For example, if the V_{CCINT} rise time has a linear rise of 15 ms, the current consumption spike will drop by 7.5 ms.

Only a subset of the EP1C6 silicon requires a power-up current up to 1.2 A. You can identify EP1C6 devices that meet the maximum power-up current requirement of 500 mA by the date code. Devices that have a top-side date code marking of "0313" (work week (WW) 13, 2003) or later have a maximum power-up current requirement of 175mA for commercial grade devices and 210mA for industrial grade devices. Figure 1 shows the format of the top-side date code.

Figure 1. Format of the Top-side Date Code



In addition to identification through the date code, affected devices can also be identified by lot code. Not all devices manufactured previous to WW13, 2003 exceed the power-up current specification. Table 1 contains a comprehensive list of device lot codes that can require up to 1.2 A of power-up current on the V_{CCINT} supply. All other lot codes, regardless of date code, have a maximum power-up current requirement of 175mA for commercial grade devices and 210mA for industrial grade devices.

Table 1. EP1C6 Device Codes with a Maximum Power-Up Current Requirement of 1.2 A

Device Lot Codes		
NAB9G00113D	NAB9G00111C	EAB9G00193D
NAB9G00113E	EAA9G00092F	EAB9G00193I
NAB9G00113I	EAA9G00092G	NAA9G00071Q
NAB9G00111B	NAA9G00071I	EAB9G00193E
QAB9G00112C	EAB9G00193C	EAB9G00193J
EAA9G00092E	EAB9G00193G	EAB9G00193K
NAA9G00071S	NAA9G00071P	NAA9G00071D

Error Detection CRC Issue

A single event upset (SEU) can cause configuration RAM bits to change. The Error Detection CRC feature on Cyclone devices detects a configuration RAM bit flip due to such events. However, the Error Detection CRC circuitry itself may corrupt the configuration RAM bits in certain cases, possibly resulting in functional failures. This issue affects all Cyclone devices.

The solution to this issue is to restrict the use of certain routing resources. This solution is available beginning with version 5.0 SP2 of the Quartus II software. The solution takes effect only when the Error Detection CRC feature is enabled. Designers using the Error Detection CRC feature need to recompile their designs using the updated software to prevent the issue from happening.

This solution may increase fit time and routing resource usage. The solution may also decrease device core f_{MAX}. Designers must check recompiled results to ensure all original design targets are still met. If the design cannot meet constraints and timing after recompilation, designers can disable the Error Detection CRC feature without any performance, fit time, and routing resource changes. Contact Altera Technical Support for this option.

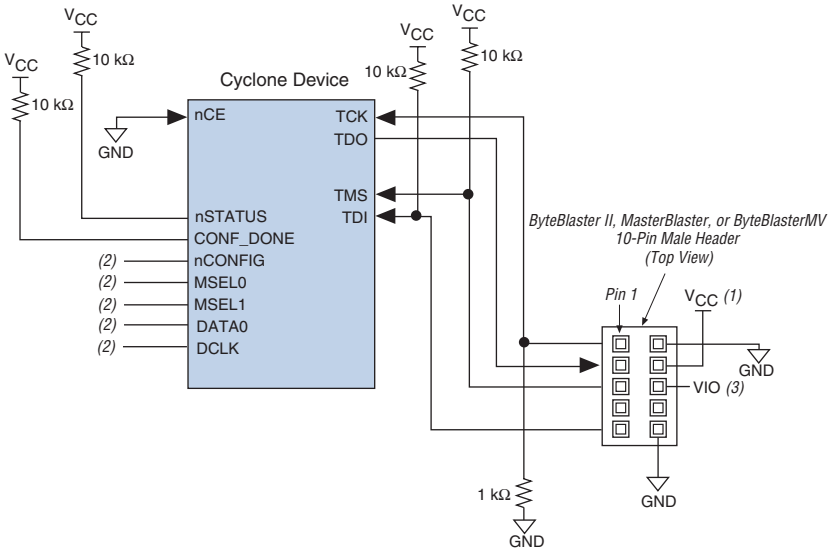
JTAG TCK Pull-Down Resistor

Altera has identified a documentation issue in two separate figures:

- Figure 13-19, *Cyclone Device Handbook* ver 1.5 (Chapter 13. Configuring Cyclone FPGAs)
- Figure 5-19, *Configuration Handbook* ver 1.5 (Chapter 5. Configuring Cyclone FPGAs)

Both figures show an external pull-down resistor to GND on the TCK signal of the JTAG interface. Figure 2 below shows the correct resistor value of "1kΩ" instead of "10kΩ".

Figure 2. JTAG Configuration of Single Cyclone FPGA



Notes to Figure 2:

(1) You should connect the pull-up resistor to the same supply voltage as the download cable.

(2) You should connect the `nCONFIG`, `MSEL0`, and `MSEL1` pins to support a non-JTAG configuration scheme. If you only use JTAG configuration, connect `nCONFIG` to V_{CC}, and `MSEL0` and `MSEL1` to ground. Pull `DATA0` and `DCLK` to high or low.

(3) V_{IO} is a reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlaster MV, this pin is a no connect. In the USB Blaster and ByteBlaster II, this pin is connected to `nCE` when it is used for Active Serial programming; otherwise it is a no connect.

(4) `nCE` must be connected to GND or driven low for successful configuration.

Cyclone FPGAs have an internal weak pull-up resistance on TCK in the range of 15kΩ to 50kΩ An external pull-down resistor value of 1kΩ ensures that a valid low-level signal is present on TCK when left un-driven, regardless of the actual value of the internal weak pull-up resistance.

Document Revision History

Table 2–1 shows the revision history for this document.

Table 2–1. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
January 2007 v1.3	• Added document revision history. • Updated "Power-Up Current" section.	
July 2006 v1.2	Added the "JTAG TCK Pull-Down Resistor" section.	
v1.1	Added the "Error Detection CRC Issue" section.	