MPLDs

Mask-Programmed Logic Devices

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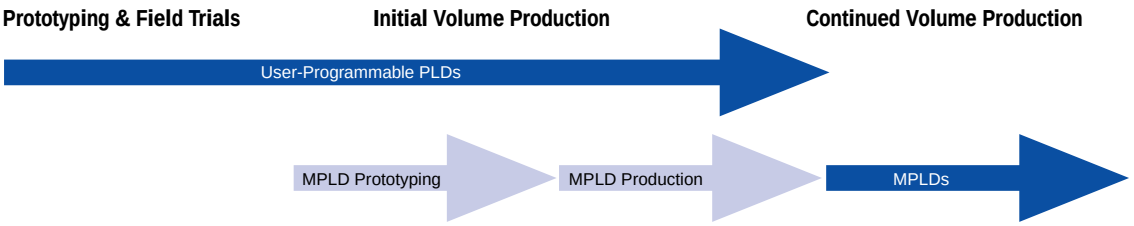
Features

- Masked versions of Altera programmable logic devices (PLDs)
- Reduced cost for high-volume production
- Available for all Altera devices
- Pin-, function-, and timing-compatible with original device
- Conversion process performed by Altera
- Fast turn-around to shorten time-to-market
- Low power consumption

General Description

Altera Mask-Programmed Logic Devices (MPLDs) provide a masked alternative to PLDs. By using a generic CMOS process and removing all programmable cells, Altera passes considerable savings on to customers who anticipate high-volume production. In addition, Altera performs the PLD-to-MPLD conversion so that customer redesign effort is not required. The combination of Altera PLDs and MPLDs provides the best of both worlds: the fast time-to-market of PLDs, and the low cost of MPLDs. See Figure 1.

Figure 1. High-Volume Production Flow with Altera PLDs & MPLDs



MPLD Compatibility

Each Altera MPLD is pin-, function-, and timing-compatible with the original PLD. This compatibility ensures that the MPLD can replace the original Altera device, while providing lower cost and maintaining the production flow. In addition, the MPLD typically consumes less power than the equivalent PLD, depending on the design and operating conditions.

The pin-out and DC specifications of the MPLD will match those of the original device. Altera ensures functional compatibility by mapping the logic within the PLD (for example, product terms, programmable flipflops, etc.) directly to specially designed elements within the MPLD. Altera's proprietary logic synthesis program uses netlist files generated by the MAX+PLUS II software to describe the final synthesis, placement, and routing of the original design. The conversion process accounts for all architecture-specific features—such as wide fan-in product terms, carry chains, and cascade chains—commonly found in programmable logic applications.

Quick, Seamless Conversion

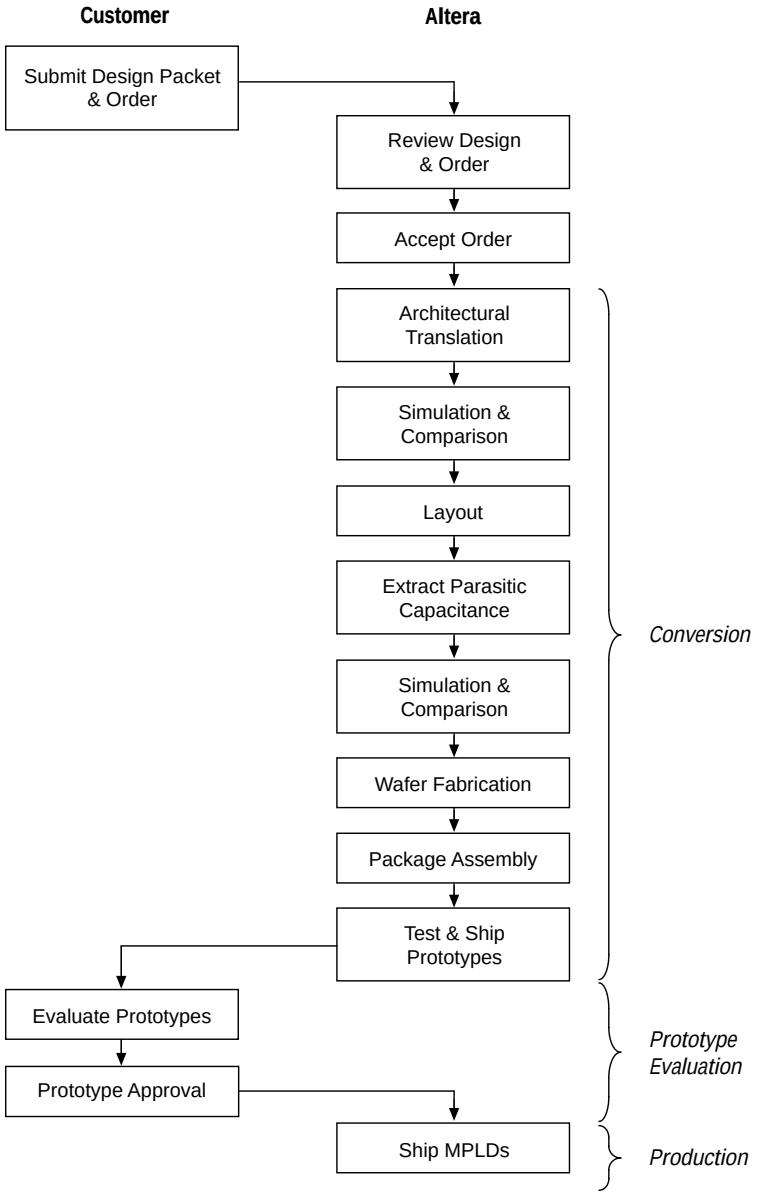
One of the principal objectives of Altera's MPLD conversion program is to minimize the engineering time and resources required for the conversion. The engineer simply submits design files created with the MAX+PLUS II software and Altera delivers MPLDs within weeks of the design sign-off.

The design conversion includes architectural translation, simulation and comparison, layout, extraction of parasitic capacitance, additional simulation and comparison, wafer fabrication, and package assembly.

Go to the ***MPLD Conversion Information & Order Forms*** workbook, available from an Altera sales representative, for the instructions and forms necessary to initiate the PLD-to-MPLD conversion.

The MPLD conversion flow chart shows how easily a programmable Altera device can be converted into an MPLD. See Figure 2.

Figure 2. MPLD Conversion Flow



Conclusion

The two most important design goals for engineers today are reducing time-to-market and minimizing system cost. Together, Altera PLDs and MPLDs provide a solution that addresses these concerns, allowing companies to take products to market quickly, lower the end-product cost, and eliminate the risks associated with ASIC design conversions.