E3 Mapper MegaCore Function (E3MAP)

March 9, 2001; ver. 1.0 Data Sheet

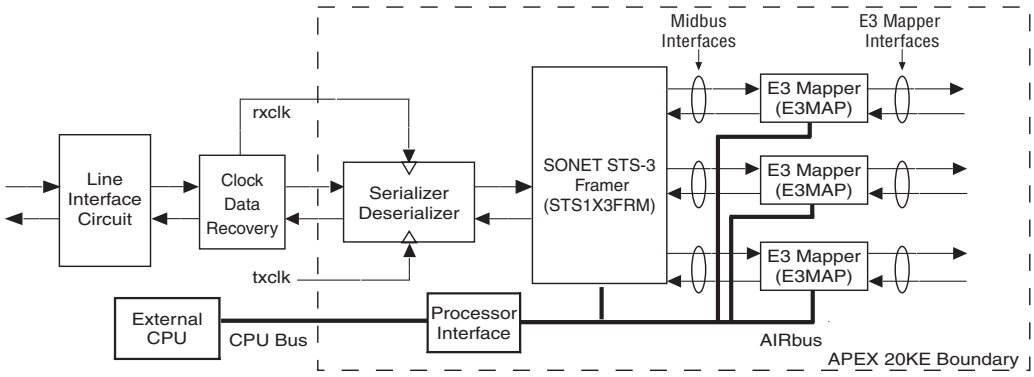
Features

- Easy-to-use MegaWizard® Plug-In generates MegaCore® variants
- Quartus™ II software and OpenCore™ feature allow place-and-route, and static timing analysis of designs prior to licensing
- Secure Register Transfer Level (RTL) simulation models allow simulation with user designs in third-party simulators
- Asynchronously maps clear channel synchronous / asynchronous transport of E3 signal over Synchronous Optical Network (SONET) Synchronous Transport Signal level 1 (STS-1) / Synchronous Digital Hierarchy (SDH) Administrative Unit level 3 (AU-3)
- Provides serial interface connection to an E3 framer (optional)
- Supports nominal E3 rates of 34.368 megabits per second (Mbps)+ / -687 bits per second (bps)
- Provides outputs to allow control of plesiochronous E3 oscillator
- Complies with all applicable standards, including:
  - International Telecommunication Union, *Network node interface for the synchronous digital hierarchy (SDH), ITU-T G. 707*, March 1996
- Optimized for the Altera® APEX™ 20KE device architecture

Typical Applications

Figure 1 shows an example system implementation of the E3MAP interfacing with other Altera MegaCore variants via the Midbus, and E3 Mapper interfaces. See "Interfaces & Protocols" on page 3.

Figure 1. Typical Application



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Functional Description

The E3MAP interfaces to a data bit stream at a data rate of up to 34.368 Mbps +/- 687—via bit stuffing—to accommodate standard E3 rates. The E3MAP maps and demaps STS-1, STS-3, and STS-12 data paths (via AU-3). The E3MAP comprises two major blocks, EXTRACT and INSERT, illustrated in Figure 2.

☞ The following list of functions is based on a full feature E3MAP.

EXTRACT

- Supports the standard E3 rate via adaptive control of the external Voltage Controlled Oscillator (VCO)
  - A software programmable threshold asserts either `vco_increase`, or `vco_decrease`, when violated. This indicates a change is required in the transmitter E3 clock rate. See "Core Clocking" on page 5. The FIFO buffer is 32 bytes deep.
- Accepts data bytes from a SONET/SDH framer
- Performs destuffing
- Extracts E3 stream, and forwards it optionally to an E3 framer

INSERT

- Performs asynchronous mapping
- Uses a 32-byte FIFO buffer
- Performs payload bit stuffing
- Provides payload bytes to a SONET/SDH framer
- Accepts an E3 bit stream that is either raw or from an E3 framer

☞ While it is expected that the E3 input stream will be within the standard limits of 34.368 Mbps +/- 687 bps, the E3MAP supports rates between 34.344 Mbps and 34.392 Mbps.

Interfaces & Protocols

Three interfaces—illustrated in Figure 2—support the E3MAP: the Middle interface (Midbus), the Access to Internal Registers (AIRbus) interface, and the E3 Mapper interface.

Midbus

The Midbus interface is a simple synchronous full-duplex data path bus. The E3MAP Midbus transports data over a single-byte lane in each direction. The required frequency varies depending on the SONET/SDH framer supported.

In the receive direction (RX), the data is transferred from the Midbus master to the slave (E3MAP). In the transmit direction (TX), data is transferred from the slave (E3MAP) to the Midbus master. In each direction the Midbus can carry eight bits per clock cycle. It includes midbus receive data (`mrxdat[7:0]`) and midbus receive enable (`mrxena`) lines to indicate a valid data transfer in the RX direction, and midbus transmit data (`mtxdat[7:0]`) and midbus transmit enable (`mtxena`) lines to indicate a valid data request in the TX direction.

AIRbus

The AIRbus interface provides access to internal registers using a simple synchronous internal processor bus protocol. This consists of separate read (`rdata`) and write (`wdata`) data buses, a data transfer acknowledge (`dtack`) signal, and a select (`sel`) signal. An address bus (`addr[3:0]`) and read (`read`) signal indicate the location and type of access within the block. The `rdata` buses and `dtack` signals can be merged from multiple blocks using a simple OR function. The `dtack` signal is sustained until the block `sel` is removed (four-way handshaking) meaning the AIRbus can cross clock domain boundaries. The E3MAP is an AIRbus slave with a data width of eight bits.

For more detailed information on the Midbus and AIRbus refer to the Altera web site at http://www.altera.com/IPmegastore.

E3 Mapper Interface

The E3 Mapper interface is used to convey full E3 data, including framing, to the mapper.

For more detailed information on the E3 Mapper interface refer to the E3 Mapper MegaCore Function user guide.

Figure 2. Block Diagram

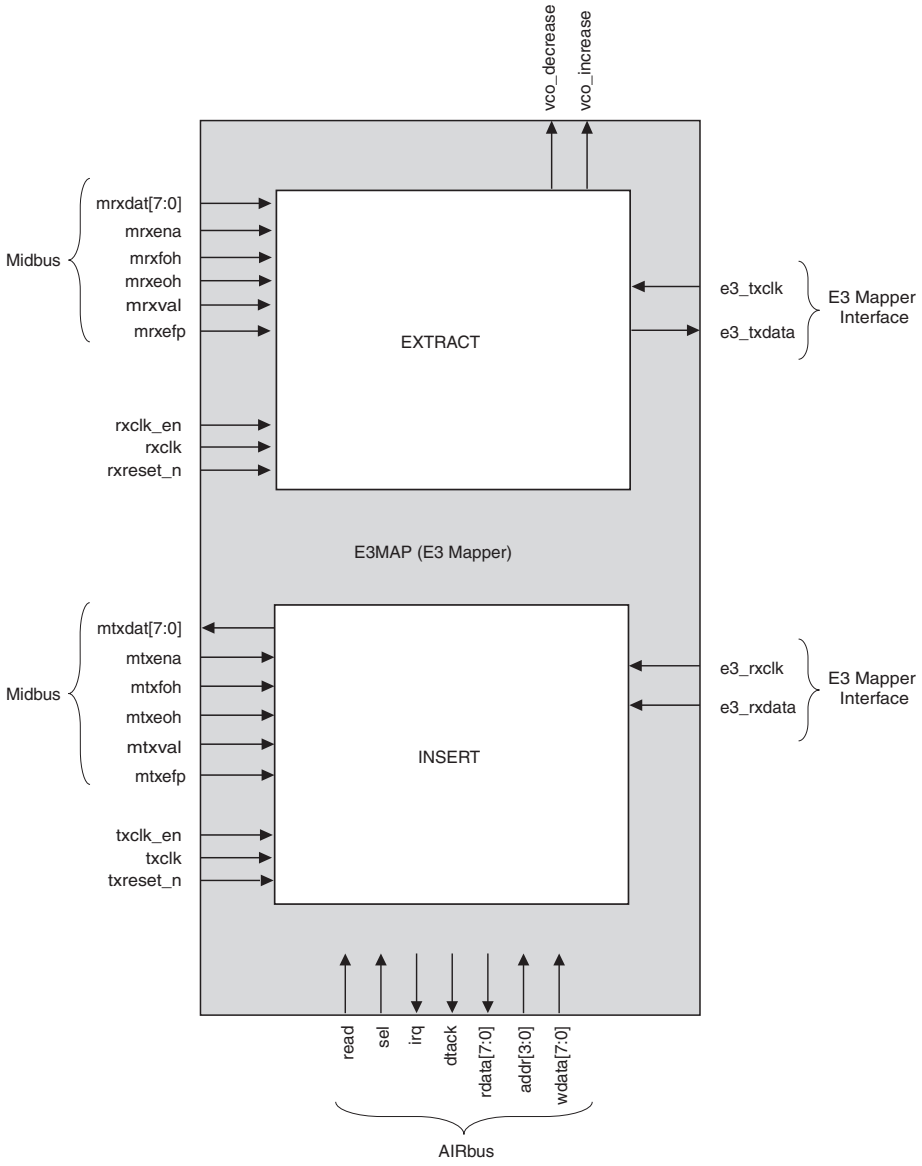
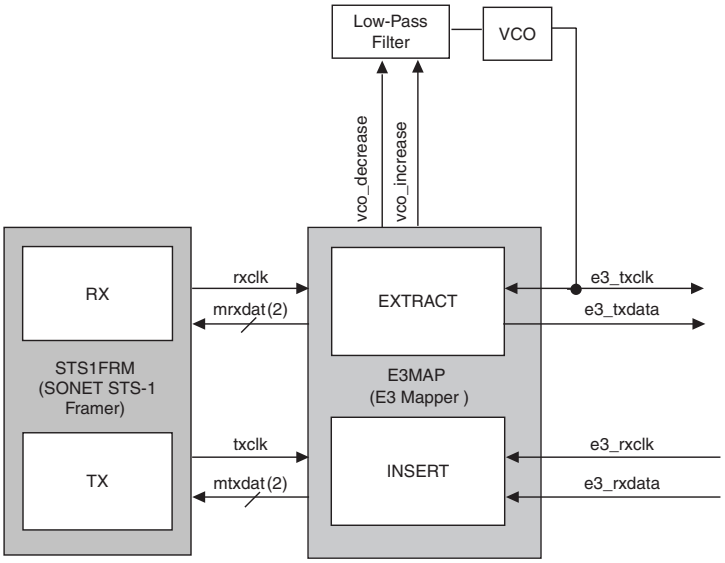


Figure 3 shows the E3MAP providing asynchronous mapping of E3 data over STS1FRM. It also depicts the interface to an external VCO, for the purpose of adjusting the `e3_txclk` clock.

Figure 3. Core Clocking



Note:
(1) For a more detailed view of the Midbus interface see Figure 2.

Performance

Table 1 shows the required speed and estimated gate count of the E3MAP in an APEX 20KE device.

Table 1. Performance ***Note (1)***

LEs	ESBs	f_{MAX} (MHz) *(2)*
950	2	34.392 required

Notes:
(1) All Logic Element (LE) and Embedded System Block (ESB) numbers are approximate as of March 9, 2001.
(2) If an E3MAP interfaces to an STS-12 line the f_{MAX} will be 77.76 MHz.

Licensing

No license is required to perform the following trial operations using your own custom logic:

- Instantiation
- Place-and-Route
- Static Timing Analysis
- Simulation on a third-party simulator

Only when you are ready to generate programming files, do you need to obtain licenses through your local Altera representative.

☞ All current variants use a single license with ordering code: PLSM-E3MAP.

Deliverables

The following elements are provided with the E3MAP package:

- Data Sheet
- User Guide
- Midbus and AIRbus Interface Functional Specifications
- MegaWizard Plug-In
  - Encrypted gate level netlist
  - Place-and-Route constraints (where necessary)
  - Secure RTL simulation model
- Sanity testbench

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