

Designers can use the Stratix GX Development Board to prototype and develop high-speed applications for Stratix™ GX and Stratix™ FPGAs. Use of this board can shorten the time to market for applicable designs. The board can demonstrate several IP cores, such as 10GE MAC, 10G Fibre Channel, SONET, POS-PHY Level 4, PCI, double data rate (DDR) SDRAM, RS-232, and NIOS® microprocessors. It can also demonstrate other high-speed buses using differential signaling standards, such as RapidIO, and other standards using LVDS signaling.

Designers can use the Stratix GX Development Board to prototype and verify high-speed designs that use Altera® devices. The high-speed transceivers are divided up and routed to different I/O connectors for high-speed interfaces. The board can be used stand-alone or plugged into a connector compatible backplane.

Features

The Stratix GX Development Board is a test and demonstration platform for high-speed analysis and applications targeted to the Stratix GX device family. The Stratix GX Development Board is the hardware portion of a Development Kit. This section lists the elements included on the board.

Devices

The Stratix GX Development Board contains one Stratix GX device and one Stratix device.

One Stratix GX Device (EP1SGX25FF1020 or EP1SGX40GF1020)

- Four or five transceiver blocks with four full duplex, 3.125-Gbps transceiver channels per block. (16 or 20 high-speed transceivers, respectively, for the EP1SGX25 or EP1SGX40 devices).
- 39 or 45 source synchronous channels
 - 20 full-duplex channels to HM-Zd connector
 - Channels connected to SMAs for DPA analysis
- Four transceivers interface to 16 SMA connectors for high-speed connections to test equipment or other boards.
- Four transceivers interface to HM-Zd high-speed connector for interfacing and running applications across a backplane.

- Four transceivers interface to four high-speed serial data connectors (HSSDC2) connectors or same HM-Zd. When using the EP1SGX40 device, an additional four transceivers connect either to the HM-Zd connector for a total of eight or four HSSDC2 connectors.
- Four transceivers interface to 10 Gigabit Ethernet network physical access (XPAK) optical transceiver module, which has four full-duplex channels for a 10 Gigabyte attachment unit interface (XAUI) interface at 3.125 Gbps per channel.
- Four transceivers interface to four small form-factor pluggable (SFP) optical transceiver connectors. Each SFP module is capable of interfacing with different standards from Fibre Channel OC-3 to OC-48 including SONET using the same footprint.
- SMA interfaces for external I/O
- 1,020-pin FineLine BGA® package

One Stratix Device (EP1S25F1020 or EP1S40F1020)

- 78 or 80 source synchronous channels
- Bus interface between Stratix GX and Stratix devices
- 1,020-pin FineLine BGA package
- SMA interfaces for external I/O

Table 1 shows the I/O pins that do not migrate between Stratix GX devices.

Table 1. Stratix GX I/O Pins that Do Not Migrate		
Package	Devices	I/O Pins
1,020-pin FineLine BGA	EP1SGX40, EP1SGX25	D29, D30, E29, E30, F27, F28, F29, F30, J23, K23, L23, M23, AA23, AB23, AC23, AD23, AG25, AG26, AH27, AH28, AH29, AH30, AJ29, AJ30
672-pin FineLine BGA	EP1SGX25, EP1SGX10	E10, E11, G16, H16, Y15, Y16, AA11, AA16

Configuration

Configuration of the board includes multiple modes for configuring the Stratix GX, Stratix, and two EPC16 devices on the board.

- Two EPC16 devices store configuration files for programming upon power-up.
- Configuration interfaces include fast passive parallel/passive serial, JTAG, and MDIO header connectors for configuration using the ByteBlaster™ II cable.
- Switches to select different configuration modes

- 10/100 Ethernet connection for remote/local updates for configuration purposes through the RJ-45 connector.

Clocks

Clocks are generated using on-board crystal oscillators and clock drivers or external clocks can be provided through SMA connectors. Each board contains up to four crystal oscillators.

- External clocks via SMA
- Clocks via on-board crystals (up to four) and clock drivers
- Clock outputs to SMAs for test/trigger
- A divide-by-20 circuit uses a high-speed external clock as input through an SMA.
- A divide-by-2 circuit is useful in SFI-5 applications.

Interfaces

- An interface between the Stratix device and external memory in the form of a DIMM socket using DDR SDRAM running at 166 or 200 MHz.
- 10/100 Ethernet media access control physical interface (MAC PHY) using an RJ-45 connector for the cable connection.

Digital Analysis/Instrumentation Connections

In addition, the Stratix GX and Stratix devices have source synchronous connections to connectors such as HM-Zd and SMAs for dynamic phase alignment (DPA) analysis and high-speed interfaces.

- RS-232 Interface for debug and register access
- Matched impedance connector (MICTOR) logic analyzer connectors
- High- and low-speed logic analyzer connectors
- Unused I/O test points
- Tektronix and Agilent logic analyzer connectors

Power

- ATX connector and power supply
- Regulators
- Banana jacks for the unregulated power sources
- A -48V power supply on the board provides for telecommunication applications.
- Socketed fuses switch between banana jacks and regulated power coming from on-board regulators

User I/O Formats

- LEDs
- Two dual seven-segment displays
- Switches for user logic functions
- Push buttons for user logic functions

Other

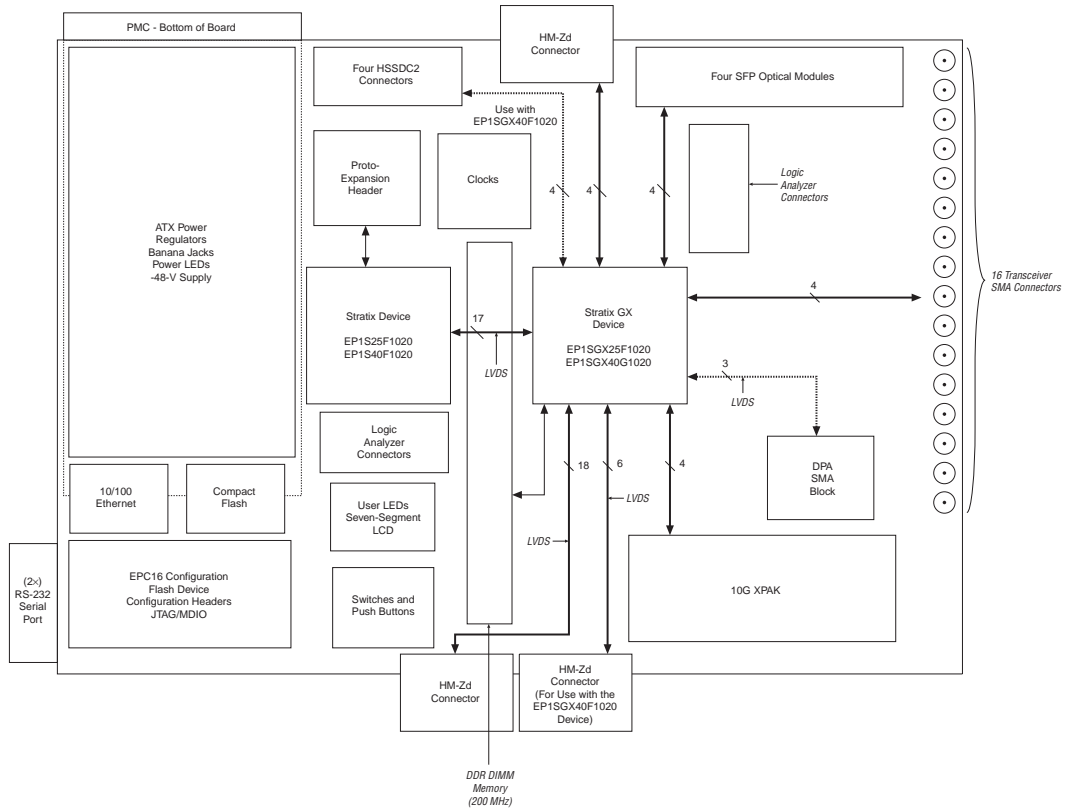
Other board capabilities include:

- Performance monitoring
- Error detection
- Phase-locked loop (PLL)
- Bus between the Stratix GX and Stratix devices
- PCI Mezzanine card interface on the bottom of the board interfaces to processor boards or other applications

Block Diagram

Figure 1 shows a block diagram of the Stratix GX Development Board.

Figure 1. Stratix GX Development Board Block Diagram



Connector Function Summary

Table 2 shows the function of the connectors on the development board.

Table 2. Stratix GX Development Board Connectors (Part 1 of 2)

Connector	Stratix GX Device	Stratix Device	Not Device Specific
FPGA device	U7	U15	
20-pin header (see the “20-Pin Headers” section)	J53	J68	
LED display (see the “Seven-Segment Displays” section)	D9	D8	

Table 2. Stratix GX Development Board Connectors (Part 2 of 2)

Connector	Stratix GX Device	Stratix Device	Not Device Specific
MICTOR (see the “Agilent Logic Analyzer Connectors” section)	J34	J75	
HM-Zd (see the “Stratix GX & HM-Zd Interface (J1)” section)			J108, J109
Logic analyzer (see the “Agilent Logic Analyzer Connectors” section)	J57	J58	
RS232			J124
HSSDC2 (see the “High-speed Connectors” section)			J1
Compact flash (see the “Compact Flash Connector Pinout” section)			CON3

Switch & Jumper Functions

Table 3 summarizes the function of each switch, quick switch, and jumper on the development board.

Table 3. Stratix GX Development Board I/O Parts (Part 1 of 2)

I/O Function	Stratix GX Device	Stratix Device	Not Device Specific
Device bypass switch	SW2	SW1	
Power switch			SW3
Passive header or EPC16 device switch			SW4
Remote or standard configuration switch			SW5
156.25-MHz crystal/SMA switch			SW6
155.52-Mhz crystal/SMA switch			SW9
In standard configuration mode, DIP switch to choose page to load in target device. In remote configuration mode, the target device selects the page to load.	SW7	SW8	
DIP switch for selecting options (see the “Octal Dual-in Line Package (DIP) Switches” section)	S11	S6	
Serial or parallel mode jumper			J48
Local or remote update jumper			J90

Table 3. Stratix GX Development Board I/O Parts (Part 2 of 2)

I/O Function	Stratix GX Device	Stratix Device	Not Device Specific
Select passive header or EPC16 device to program Stratix and Stratix GX devices			Quick switch 1 Quick switch 2 Quick switch 3
Remote or standard configuration quick switches			Quick switch 4 Quick switch 5

Development Board Stratix & Stratix GX Devices

The Altera Stratix devices combine the latest in silicon features to achieve industry-leading performance in internal speed, I/O speeds, and internal memory density. The development board is designed for two 1,020-pin FineLine BGA packages, which are an EP1SGX25FF1020 or EP1SGX40GF1020 device and either an EP1S25F1020 or an EP1S40F1020 device. The EP1SGX40 and EP1S40 devices are the size options that allow additional high-speed differential logic (HSDI) interface capability, as well as additional PLLs, memory, and logic elements (LEs). Table 4 shows the devices' features.

Table 4. Development Board Stratix & Stratix GX Device Features

Feature	EP1S25	EP1S40	EP1SGX25	EP1SGX40
LEs	25,660	41,250	25,660	41,250
RAM bits	1,944,576 (237 KB)	3,423,744 (417 KB)	1,944,576 (237 KB)	3,423,744 (417 KB)
PLLs	6 (4 fast and 2 enhanced)	12 PLLs (8 fast and 4 enhanced)	4	8
Transmitter and receiver source synchronous channels	78	80	39	45
Transceiver channels			16	20
Medium speed channels		10 receivers 10 transmitters		
User I/O pins	706	773	542	548
DSP blocks			10	14
Embedded multipliers			80	112

Board Layer Stack-Up

The Stratix GX Development Board consists of 18 layers of FR4 material for a combined width of 0.093 inches. The board layer stack-up is shown in Table 5.

Table 5. Stratix GX Development Board Layer Stack-Up *Note (1)*

Layer Number	Layer Type	Description	Thickness & Tolerances	
			Copper Thickness (Mils)	Laminate (Mils)
1	Mix	Foil	0.00035	
		Pre-pregate		0.0030 ±0.0003
2	Plain	Core 0.0040 1/H	0.0012	0.0040
3	Signal		0.00060	
		Pre-pregate		0.0050 ±0.0005
		Pre-pregate		
4	Mix	Core 0.0040 H/1	0.00060	0.0040
5	Plain		0.00120	
		Pre-pregate		0.0040 ±0.0004
6	Mix	Core 0.0060 H/H	0.00060	0.0060
7	Mix		0.00060	
		Pre-pregate		0.0040 ±0.0004
8	Plain	Core 0.0040 1/H	0.00120	0.0040
9	Signal		0.00060	
		Pre-pregate		0.0050 ±0.0005
10	Mix	Core 0.0040 H/1	0.00060	0.0040
11	Plain		0.00120	
		Pre-pregate		0.0040 ±0.0004
12	Signal	Core 0.0060 H/H	0.00060	0.0060
13	Signal		0.00060	
		Pre-pregate		0.0040 ±0.0004
14	Plain	Core 0.0040 1/H	0.00120	0.0040
15	Signal		0.00060	
		Pre-pregate		0.0050 ±0.0005
16	Signal	Core 0.0040 H/1	0.00060	0.0040
17	Plain		0.00120	
		Pre-pregate		0.0030 ±0.0003
18	Mix	Foil	0.00035	

Note to Table 5:

(1) 0.5 oz of copper is equivalent to a 0.6-mils trace width.

Power Sources

The Stratix GX Development Board has seven regulators:

- Two DC-DC converters
- Two switching regulators
- Six linear regulators

For this document, “DC-DC converters” implies DC isolation between the input and outputs, while “switching regulator” does not. Table 6 lists the power sources used on the Stratix GX Development Board.

Table 6. Stratix GX Development Board Regulators & DC-DC Converters

Reference Designator	Type	Voltage Output (V)	Description	Manufacturer	Part Number
U2	Linear regulator	1.5	Stratix GX transceivers and PLLs	National	LMS1585ACS-ADJ
U1	Linear regulator	2.5	Stratix GX I/O (banks 7 & 8), DDR	Micrel	MIC29502BU
U38	Linear regulator	3.3	V_{REF} for U37	Micrel	MIC5209BM
U42	Linear regulator	3.3	Powers clock circuitry	Micrel	MIC29502BU
U36	Switching regulator	1.5	Stratix V_{CCINT} , Stratix GX V_{CCINT} , XPAK signal bias	Fairchild	FAN5066
U53	Linear regulator	1.25	SSTL-2 class II terminations, DDR, Stratix GX V_{REF}	National	LP2995M
U37	Switching regulator	3.3	Stratix GX V_{CCA} , V_{CCIO} , Stratix V_{CCIO} , PLL, SFP modules, XPAK connector, adjustable power supply (APS), PMC, 10/100 Ethernet components, proto-expansion header, RS232 components, flash memory, FPGA configuration components, user switches, seven-segment LCDs, LEDs, and MDIO	Fairchild	FAN5066
U45	DC-DC converter	12	Used with a -48V input supply	DI DT	SQ48T04120-NBC0
U8	DC-DC converter	5, 3.3	Used with a -48V input supply	DI DT	QD48T033050-NBC0
U60	Linear regulator	3.8	Used with divide-by-20 clock output buffer	Micrel	MIC5219BM5

The board can be powered in three different ways:

1. ATX power supply (J31)
2. -48-V input (J8, J9)
3. Bench power supplies (various connectors)

ATX Power Supply


In normal operation, the ATX power supply is used. The ATX power supply is a 250-Watt unit and provides 3.3, 5, 12, -5, and -12 V.

Table 7 lists the characteristics of the ATX power supplies.


Mnemonic (V)	Description	Nominal Value (V)	Tolerance	Maximum Ripple (mV)
5	+5 V DC	5.0	±5%	50
3.3	+3.3 V DC	3.3	±5%	50
+12	+12 V DC	12	±5%	50
-12	-12 V DC	-12	±5%	50
GND	Ground			

ATX Power Supply Power Resistor

According to the manufacturer, the 5.0-V output of this unit requires a minimum current draw of 2.0 A, which implies that there needs to be a 2.5- Ω power resistor on the board to guarantee this. The power dissipation on this resistor is 10 Watts, making the resistor very hot.

 Altera does not populate this power resistor by default because lab experiments have shown that the ATX functions properly without this minimum current draw.

The ATX power supply also needs to guarantee 300 mA on the 3.3-V supply. This can be easily met by using a 9.0- Ω power resistor on the board. This resistor also gets hot, but not as hot as the load resistor on the 5.0-V supply.

 Altera does populate this resistor by default.

–48V input

A –48-V input is provided by banana jacks. Two DC-to-DC converters convert the –48 V to +12 V, +5 V, and +3 V. To use this option, supply –48 V and do not plug in the ATX power connector.

Bench Power Supplies

Socketed fuses are provided to bypass the ATX power supply and –48-V input in order to use bench supplies connected through banana jacks. The bench supply inputs are placed after the other power supplies (whether linear or switching supplies) on the board in order to allow current draw measurements.

Power Planes

Bench power supplies provide an easy way to measure the current draw on each power plane. When one plane is being powered by the bench supply, all other planes still draw current from the ATX power supply. Upon applying power to the board, the power LED should be on.

Table 8 shows the procedure for powering individual planes through bench power supplies. In the instructions in Table 8, only remove the fuse listed in the “Instructions” column. Leave the other fuses on the board.

Power Plane	Power Plane Using Bench Power Supplies(1)	Instructions
1.5V_PLL	Stratix GX PLL	Remove fuse F8. Apply (+1.5V, GND) to (J33, J35)
1.5V_XCVR	Stratix GX transceiver power	Remove fuse F5. Apply (+1.5V, GND) to (J12, J13)
2.5V_GX_IO	Stratix GX I/O power	Remove fuse F1. Apply (+2.5V, GND) to (J7, J21)
2.5V	DDR power	Remove fuse F2. Apply (+2.5V, GND) to (J10, J21)
1.5V_S_INT	Stratix VCCINT	Remove fuse F12. Apply (+1.5V, GND) to (J40, J22)
1.5V_GX_INT	Stratix GX VCCINT	Remove fuse F10. Apply (+1.5V, GND) to (J39, J22)
1.25V	SSTL2 Class II terminations, DDR, Stratix GX V_{REF}	Remove fuse F20. Apply (+1.25V, GND) to (J14, J22)
1.25V_GX_SSTL_VREF	SSTL2 Class II reference voltage	Remove fuse F21. Apply (+1.25V, GND) to (J125, J22)
3.3V_XCVR_CLK	Stratix GX VCCA	Remove fuse F13. Apply (+3.3V, GND) to (J51, J22)

Table 8. Procedure for Powering Individual Power Planes through Bench Power Supplies

Power Plane	Power Plane Using Bench Power Supplies(1)	Instructions
3.3V_S_IO	Stratix VCCIO	Remove fuse F14. Apply (+3.3V, GND) to (J65, J73)
3.3V	Stratix PLL, SFP modules, XPAK connector, APS, PMC, 10/100 Ethernet components, proto-expansion header, RS232 components, flash memory, FPGA configuration components, user switches, seven-segment LCDs, LEDs, and MDIO	Remove fuseF15. Apply (+3.3V, GND) to (J66, J73)
3.3V_GX_IO	Stratix GX VCCIO	Remove F16. Apply (+3.3V, GND) to (J67, J73)

Note to Table 8:

(1) Power plane which will use bench power supply rather than the ATX power supply.

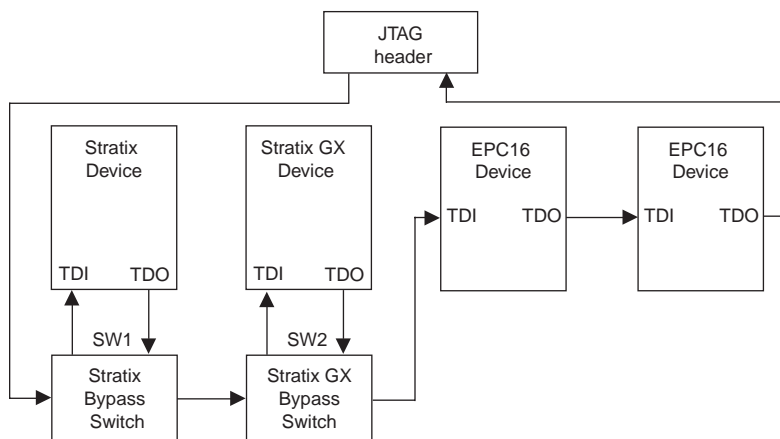
Configuration

The Stratix GX Development Board allows the user to configure the Stratix and Stratix GX devices individually or in a chain. The Stratix GX Development Board uses three different local configuration modes and one remote system configuration mode for configuring the Stratix and Stratix GX devices. The available configuration modes are:

- Passive serial mode using:
 - The passive serial header
 - The EPC16 devices
 - A remote RS-232 or Ethernet connection
- Fast passive parallel mode using:
 - The EPC16 devices
 - A remote RS-232 or Ethernet connection

JTAG Chain High-level Diagram

Figure 2 shows the JTAG chain used to program the Stratix GX Development Board.

Figure 2. JTAG Chain

The Stratix GX Development Board has Stratix and Stratix GX devices chained with two EPC16 devices. Bypass switches select whether or not a Stratix or Stratix GX device may be configured in the chain. The EPC16 devices are always in the chain. The ByteBlaster II cable is used to program this chain.

To configure the devices on the Stratix GX Development Board using the JTAG header, set the bypass switches (SW1, SW2) as described in Table 9.

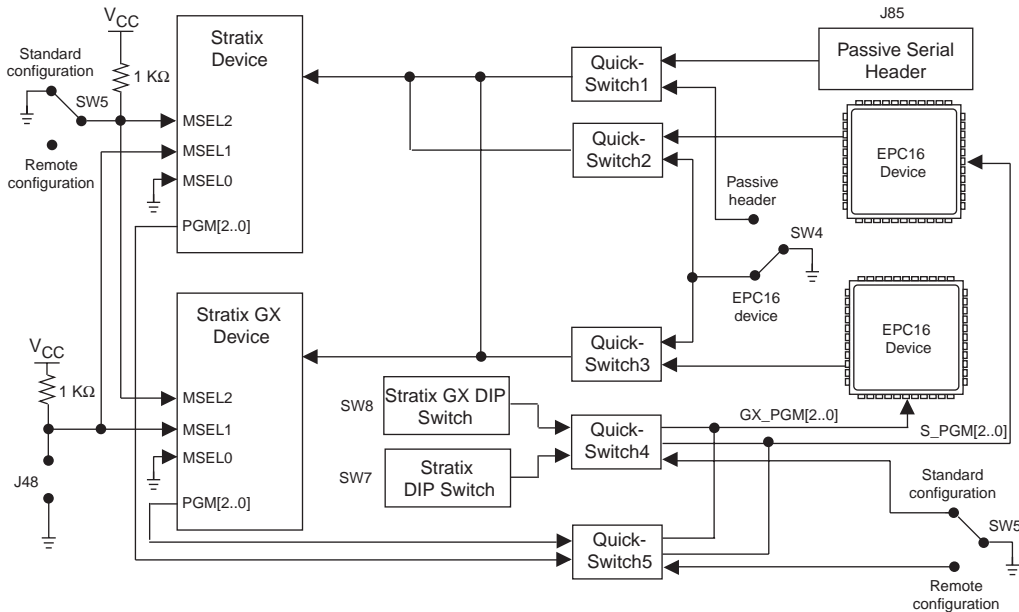
Table 9. JTAG Switch Setting for Device Chain

Devices in Chain	SW7[2..0]	SW8[2..0]	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Passive Header or EPC16 Device Switch (SW4)
Stratix, Stratix GX, EPC16A, and EPC16B	000	000	No	No	Shunt	PS_HDR
Stratix GX, EPC16A, and EPC16B	000	000	Yes	No	Shunt	PS_HDR
Stratix, EPC16A, and EPC16B	000	000	No	Yes	Shunt	PS_HDR
EPC16A and EPC16B	000	000	Yes	Yes	Shunt	PS_HDR

Passive Configuration High-level Diagram

Figure 3 shows the passive configuration used to program the Stratix GX Development Board.

Figure 3. Passive Configuration Note (1)



Note to Figure 3:

(1) Figure 3 only shows two of the four SW4 poles.

The Stratix and Stratix GX devices on the Stratix GX Development Board may be programmed in passive serial mode using the ByteBlaster II download cable either in a chain or individually.

- If using the EPC16 devices for configuration, to choose the mode to program the Stratix and/or Stratix GX devices configure the shunt jumper J48.
 - Do not install the J48 jumper for passive serial mode.
 - Install the J48 jumper for fast passive parallel mode.
- To choose the EPC16 devices or the passive serial header to program the Stratix and Stratix GX devices use the quadruple-pole double-throw switch SW4.
- To configure the Stratix and Stratix GX devices independently use the two bypass switches SW1 (Stratix device) and SW2 (Stratix GX device).

- When a bypass switch is set to YES that device is bypassed during programming.
- When a bypass switch is set to NO that device is not bypassed during programming.

Tables 10 through 12 show the passive configuration settings for the board.

- Table 10 shows the switch settings to configure the board devices using the passive serial header.
- Table 11 shows the switch settings to configure the Stratix and Stratix GX in passive serial mode using the EPC16
- Table 12 shows the switch settings to configure the Stratix and Stratix GX devices in fast passive parallel using the EPC16. .

Table 10. Switch Settings for Configuring Using The Passive Serial Header

Devices Configured	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Passive Header or EPC16 Device Switch (SW4)
Stratix and Stratix GX	No	No	Do not install	PS_HDR
Stratix GX	Yes	No	Do not install	PS_HDR
Stratix	No	Yes	Do not install	PS_HDR

Table 11. Switch Settings for Passive Serial Configuration Using the EPC16 Devices *Note (1)*

Devices Configured	SW7	SW8	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Local or Remote Update Jumper (J90)	Passive Header or EPC16 Device Switch (SW4)	Remote or Standard Configuration (SW5)
Stratix and Stratix GX	000	000	No	No	Open	Shunt	EPC_16	STD_CFG
Stratix GX	XXX	000	Yes	No	Open	Shunt	EPC_16	STD_CFG
Stratix	000	XXX	No	Yes	Open	Shunt	EPC_16	STD_CFG

Table 12. Switch Settings for Fast Passive Parallel Configuration Using the EPC16 Devices *Note (1)*

Devices Configured	SW7	SW8	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Local or Remote Update Jumper (J90)	Passive Header or EPC16 Device Switch (SW4)	Remote or Standard Configuration (SW5)
Stratix and Stratix GX	000	000	No	No	Shunt	Shunt	EPC_16	STD_CFG
Stratix GX	XXX	000	Yes	No	Shunt	Shunt	EPC_16	STD_CFG
Stratix	000	XXX	No	Yes	Shunt	Shunt	EPC_16	STD_CFG

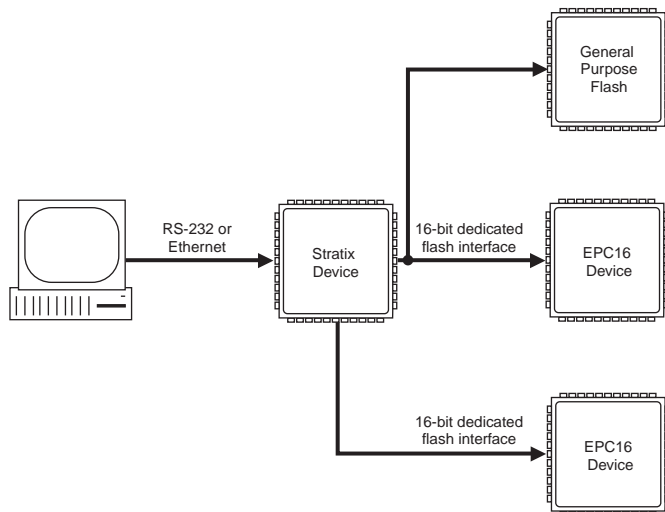
Note to Tables 11 and 12:

(1) X = Don't care.

Remote System Configuration High-level Diagram

The Stratix GX Development Board has the remote system configuration feature. This feature allows the Stratix and Stratix GX device to be updated and configured over an Ethernet or RS-232 connection. Figure 4 illustrates how the new configuration data is loaded in flash memory.

Figure 4. Remote System Configuration High-level Diagram



The following describes the process for remote system configuration using the RS-232 interface:

1. The remote system transfers the configuration data over an RS-232 interface to the Stratix device.
2. A UART on this device writes this configuration data to the Nios® processor.
3. The Nios processor writes the configuration data to the dedicated flash interface where the information is stored in the EPC16 devices.
4. Upon a successful transfer of the configuration data and re-initialization, the board is configured with the new data.

The following describes the process for remote system configuration using the Ethernet interface:

1. The remote system transfers the configuration data over an Ethernet interface to the Stratix device.
2. A UART on this device writes this configuration data to the Stratix Nios processor.
3. The Nios processor writes the configuration data to the dedicated flash interface where the information is stored in non-volatile RAM on the Stratix EPC16 device.
4. The configuration data for the Stratix GX device is transferred over the bridge to be written to the dedicated flash interface on the EPC16 for the Stratix GX device.
5. Upon a successful transfer of the configuration data and re-initialization, the board is configured with the new data.

Tables 13 through 16 show the remote and local configuration settings for the board devices. Before powering up the Stratix GX Development Board or resetting the board:

- Set the switches as described in Table 13 for the remote system configuration to do a **local update configuration in fast passive parallel** mode
- Set the switches as described in Table 14 for the remote system configuration to do a **remote update configuration in fast passive parallel** mode
- Set the switches as described in Table 15 for the remote system configuration to do a **local update configuration in passive serial** mode

- Set the switches as described in Table 16 for the remote system configuration to do a **remote update configuration in passive serial mode**.

Table 13. Local Update Configuration in Fast Passive Parallel Mode *Note (1)*

Devices Configured	SW7	SW8	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Local or Remote Update Jumper (J90)	Passive Header or EPC16 Device Switch (SW4)	Remote or Standard Configuration (SW5)
Stratix and Stratix GX	XXX	XXX	No	No	Shunt	Shunt	EPC_16	RMT_CFG
Stratix GX	XXX	XXX	Yes	No	Shunt	Shunt	EPC_16	RMT_CFG
Stratix	XXX	XXX	No	Yes	Shunt	Shunt	EPC_16	RMT_CFG

Table 14. Remote Update Configuration in Fast Passive Parallel Mode *Note (1)*

Devices Configured	SW7	SW8	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Local or Remote Update Jumper (J90)	Passive Header or EPC16 Device Switch (SW4)	Remote or Standard Configuration (SW5)
Stratix and Stratix GX	XXX	XXX	No	No	Shunt	Open	EPC_16	RMT_CFG
Stratix GX	XXX	XXX	Yes	No	Shunt	Open	EPC_16	RMT_CFG
Stratix	XXX	XXX	No	Yes	Shunt	Open	EPC_16	RMT_CFG

Table 15. Local Update Configuration in Passive Serial Mode *Note (1)*

Devices Configured	SW7	SW8	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Local or Remote Update Jumper (J90)	Passive Header or EPC16 Device Switch (SW4)	Remote or Standard Configuration (SW5)
Stratix and Stratix GX	XXX	XXX	NO	NO	OPEN	Shunt	EPC_16	RMT_CFG
Stratix GX	XXX	XXX	YES	NO	OPEN	Shunt	EPC_16	RMT_CFG
Stratix	XXX	XXX	NO	YES	OPEN	Shunt	EPC_16	RMT_CFG

Table 16. Remote Update Configuration in Passive Serial Mode *Note (1)*

Devices Configured	SW7	SW8	Stratix Bypass Switch (SW1)	Stratix GX Bypass Switch (SW2)	Serial or Parallel Mode Jumper (J48)	Local or Remote Update Jumper (J90)	Passive Header or EPC16 Device Switch (SW4)	Remote or Standard Configuration (SW5)
Stratix and Stratix GX	XXX	XXX	No	No	Open	Open	EPC_16	RMT_CFG
Stratix GX	XXX	XXX	Yes	No	Open	Open	EPC_16	RMT_CFG
Stratix	XXX	XXX	No	Yes	Open	Open	EPC_16	RMT_CFG

Note to Tables 13 – 16:

(1) X = Don't care bit.

Clocking

The clocking circuitry design of the Stratix GX Development Board has been designed with flexibility and user friendliness in mind. The clocks are passed through logic translators and routed to the appropriate destinations as shown in Figures 5 through 7. The board has the following three crystal oscillators:

- (Y4) is a 25-MHz crystal used in the MAC/PHY interface
- (Y3) is a 156.25-MHz crystal designed for XAUI applications
- (Y2) runs at 155.52-MHz and supports SONET OC-48 applications
- (Y1) runs at 33.33-MHz and is used for general purpose clocking needs on the board

In addition to the crystal inputs, there are SMA connectors to provide alternative ways to clock the board. Each crystal can be bypassed with an SMA input. Additionally, there are several differential clock inputs from SMA connectors.

The board also has dedicated circuitry that can take a differential clock input from SMA connectors and either pass it through unchanged or divide it by 2 and output to SMA connectors.

The board also has dedicated circuitry that can take a 3.125-GHz clock and divide it by 20. A cascade of two dividers implements this with the first one performing the divide-by-four function and the second performing the divide-by-five function.

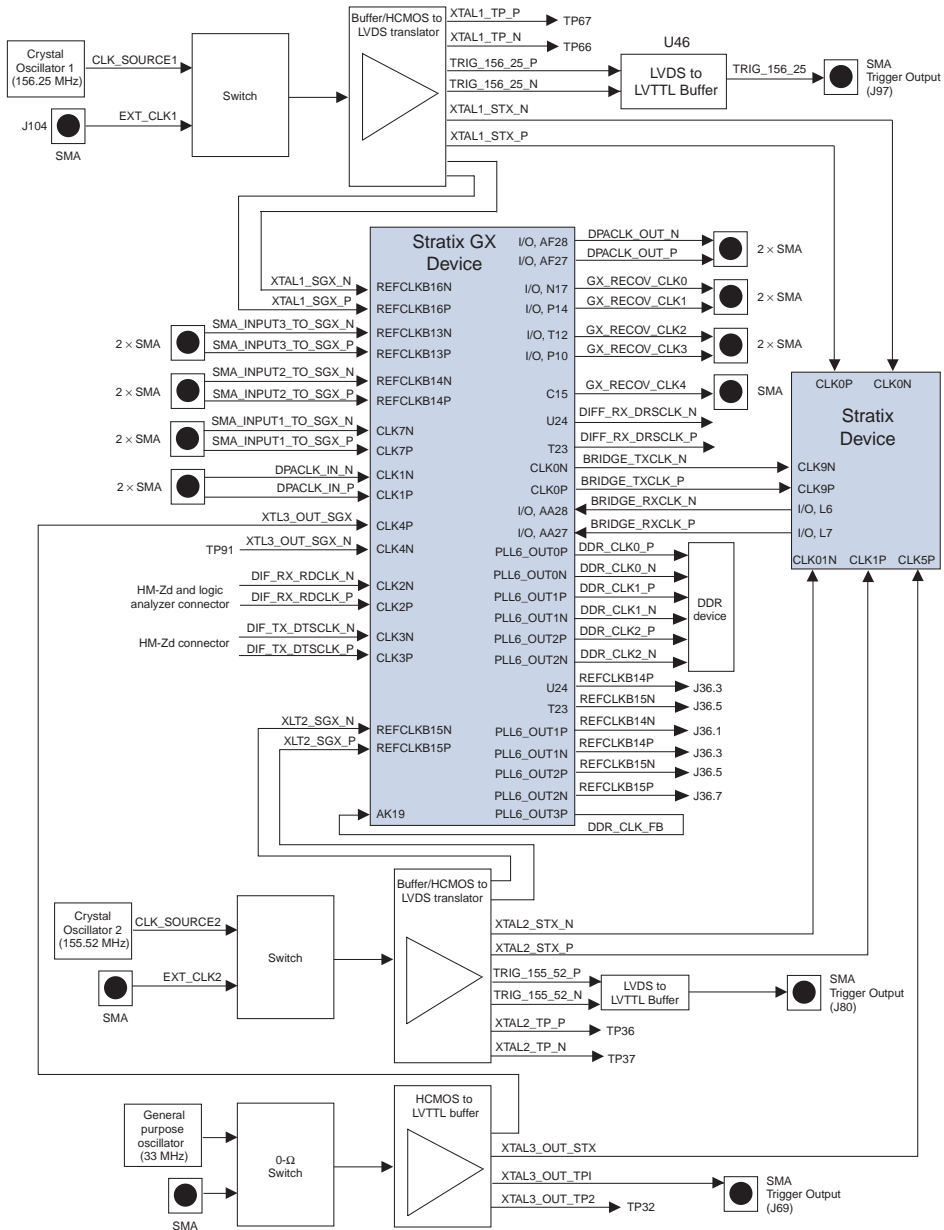
See Table 17 for the complete list of clock nets and their descriptions.

Clock Name	Origin	Destination	Description
XTAL1_TP_P XTAL1_TP_N	HCMOS to LVDS translator (U32)	Test points (TP66, TP67)	Test point clock outputs for monitoring.
TRIG_156.25	U46	SMA	SMA clock output for monitoring/triggering
XTAL1_STX_P XTAL1_STX_N	U32	Stratix device (U15)	156.25-MHz differential clock input to the Stratix device
XTAL1_SGX_P XTAL1_SGX_N	U32	Stratix GX device (U7)	156.25-MHz differential clock input to the Stratix GX device
SMA_INPUT1_TO_SGX_P SMA_INPUT1_TO_SGX_N	SMA	U7	Differential SMA input clock to the Stratix GX device
SMA_INPUT2_TO_SGX_P SMA_INPUT2_TO_SGX_N	SMA	U7	Differential SMA input clock to the Stratix GX device
DPACLK_IN_N DPACLK_IN_P	SMA	U7	Differential SMA input clock to the Stratix GX device (for DPA applications)
XTAL3_OUT_SGX	HCMOS to LVTTTL buffer (U13)	U7	33.33-MHz crystal output in LVTTTL standard
DIFF_RX_RDCLK_P DIFF_RX_RDCLK_N	HM-Zd Connector (J1)	U7	Clock from HM-Zd source synchronous link
DPACLK_OUT_P DPACLK_OUT_N	U7	SMA	Differential output clock from the Stratix GX device to SMA (DPA applications)
GX_RECOV_CLK[4..0]	U7	SMA	Recovered clock from the transceivers (one from each quad)
BRIDGE_TXCLK_P BRIDGE_TXCLK_N	U7	U15	Output clock from the Stratix GX device to the Stratix device for the bridge
BRIDGE_RXCLK_P BRIDGE_RXCLK_N	U15	U7	Output clock from the Stratix device to the Stratix GX device for the bridge
DDR_CLK[2..0]_P DDR_CLK[2..0]_N	U7	XU1	Three pairs of differential clocks required by DDR DIMM
XTAL2_TP_P XTAL2_TP_N	HCMOS to LVDS translator (U18)	Test points (TP36, TP37)	Test point clock outputs for monitoring
TRIG_155.52	U47	SMA	SMA clock output for monitoring/triggering
XTAL2_STX_P XTAL2_STX_N	U18	U15	155.52-MHz signal supplying the Stratix device

Table 17. Stratix GX Development Board Clock Nets (Part 2 of 2)

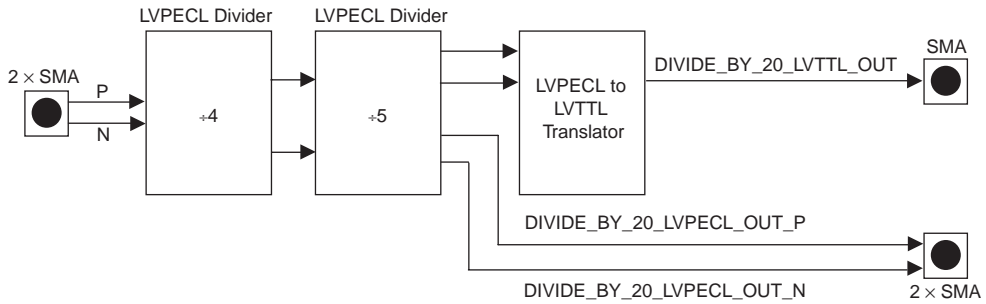
Clock Name	Origin	Destination	Description
XTAL2_SGX_P XTAL2_SGX_N	U18	U7	155.52-MHz signal supplying the Stratix GX device
XTAL3_OUT_STX	HCMOS to LVTTTL translator (U13)	U15	33.33-MHz crystal output supplying the Stratix device
XTAL3_OUT_TP1	U13	SMA	SMA test clock output for monitoring
XTAL3_OUT_TP2	U13	Test point (TP32)	Test point clock outputs for monitoring
DIVIDE_BY_20_LVTTTL_OUT	LVPECL to LVTTTL translator (U9)	SMA	LVTTTL version of signal divided by 20
DIVIDE_BY_20_LVPECL_OUT_P DIVIDE_BY_20_LVPECL_OUT_N	LVPECL divider (U6)	SMA	LVPECL version of signal divided by 20
CLK_OUT_A	U10	SMA	Output of divide by 1 or 2 circuitry
CLK_OUT_B	U10	SMA	Output of divide by 1 or 2 circuitry
EXT_CLK1	J104 SMA	U32	Input clock to Stratix GX device bank 16. Input clock to Stratix device PLL 1.
EXT_CLK2	J91 SMA	U18	Input clock to Stratix GX device bank 15. Input clock to Stratix device PLL 1.
DIFF_TX_DTSCCLK_N DIFF_TX_DTSCCLK_P	SPI 4.2 U7	J109 SPI 4.2	Transmit status clock for the SPI 4.2 interface.
REFCLKB[15..14]N REFCLKB[15..14]P	U7	J36	Spare clocks for future applications.
DIFF_RX_DRSCCLK_N	U7	J109 SPI 4.2	Receive status clock for the SPI 4.2 interface.
DATA_GEN_CLK_INN DATA_GEN_CLK_INP	J29 J30	U4	Input to divide-by-20 clock circuitry.
EXT_CLK_IN_N EXT_CLK_IN_P	J62 J61	U10	Input to divide-by-2 clock circuitry.

Figure 5. Stratix GX Development Board Clocking Circuitry Note (1)

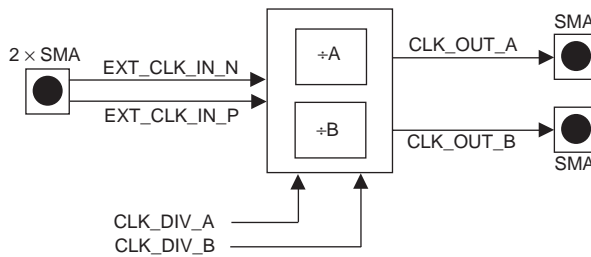


Note to Figure 5:

(1) Figure 5 only shows the important blocks of the clocking network. See the board schematics for details.

Figure 6. Divide-by-20 Clocking Circuitry Note (1)**Note to Figure 6:**

(1) Figure 6 only shows the important blocks of the clocking network. See the board schematics for details.

Figure 7. Divide-by-1 or -2 Clocking Circuitry Note (1)**Note to Figure 7:**

(1) Figure 7 only shows the important blocks of the clocking network. See the board schematics for details.

User I/O Standards

Octal Dual-in Line Package (DIP) Switches

Each Stratix and Stratix GX device is connected to a separate 8-position DIP switch (model 76SB08), allowing the user to configure several common options. These DIP switches are for reference design functions and general purpose use. Tables 18 and 19 list the pin assignment for each switch.

- When a switch is in the ON position a “0” is selected for the option.
- When the switch is in the OFF position, a “1” is selected for the option.

Table 18. Stratix GX DIP Switch Pinouts

Signal Name	DIP Switch (S11) Pin	Stratix GX (U7) Pin
GX_DIP0	16	F15
GX_DIP1	15	D15
GX_DIP2	14	E15
GX_DIP3	13	G8
GX_DIP4	12	H10
GX_DIP5	11	H12
GX_DIP6	10	G14
GX_DIP7	9	B14
GND	1	NA
GND	2	NA
GND	3	NA
GND	4	NA
GND	5	NA
GND	6	NA
GND	7	NA
GND	8	NA

Table 19. Stratix DIP Switch Pinouts (Part 1 of 2)

Signal Name	Dip Switch (S6) Pin	Stratix (U15) Pin
S_DIP0	16	AC23
S_DIP1	15	AD24
S_DIP2	14	AD23
S_DIP3	13	AG24
S_DIP4	12	AE24
S_DIP5	11	AE23
S_DIP6	10	AF24
S_DIP7	9	AC22
GND	1	NA
GND	2	NA
GND	3	NA

Table 19. Stratix DIP Switch Pinouts (Part 2 of 2)

Signal Name	Dip Switch (S6) Pin	Stratix (U15) Pin
GND	4	NA
GND	5	NA
GND	6	NA
GND	7	NA
GND	8	NA

Push Buttons

Push buttons (model EVQPAC07K) are provided for board-level reset, device-wide reset, and for user defined functions. LEDs are used to indicate the signal levels for the board and device level resets. Table 20 lists the assignment for each push button and LED.

Table 20. Push Button Pinout

Signal Name	Function	Push Button Number	FPGA Connection	Indicator LED
GLOBAL_RST_N	Global reset	S13	U29.16, U30.16, U7.K20, U15.J18	D17
GX_PB_DEV_CLR_N	Stratix GX device clear	S14	U7.AD14	D16
GX_PB0	Stratix GX device, user defined	S2	U7.G23	NA
GX_PB1	Stratix GX device, user defined	S3	U7.D28	NA
GX_PB2	Stratix GX device, user defined	S4	U7.E26	NA
GX_PB3	Stratix GX device, user defined	S5	U7.G24	NA
S_PB_DEV_CLR_N	Stratix device clear	S12	U15.AH14	D14
S_PB0	Stratix device, user defined	S8	U15.AB20	NA
S_PB1	Stratix device, user defined	S9	U15.AG22	NA
S_PB2	Stratix device, user defined	S10	U15.AB24	NA
S_PB3	Stratix device, user defined	S7	U15.AC24	NA

General Purpose LEDs

Green, surface mount LEDs (SM1206) are provided for general purpose use. A buffer is used between the FPGA and diodes as the diodes have a forward voltage (V_{FD}) of 2.1 V and require a 20-mA current to output light at the recommended levels. Table 21 lists the assignment for each LED.

- A logic 0 is driven on the I/O port to turn the LED ON.
- A logic 1 is driven on the I/O port to turn the LED OFF.

Table 21. LED Pinout

Signal Name	Reference Description	FPGA Connection
GX_LED0	D10	U7.J22
GX_LED1	D11	U7.E27
GX_LED2	D12	U7.F26
GX_LED3	D13	U7.B30
GX_LED4	D14	U7.C30
GX_LED5	D15	U7.E28
S_LED0	D18	U15.AB22
S_LED1	D19	U15.AF23
S_LED2	D20	U15.AM29
S_LED3	D21	U15.AL29
S_LED4	D22	U15.AL30
S_LED5	D23	U15.AK29

Dedicated LEDs

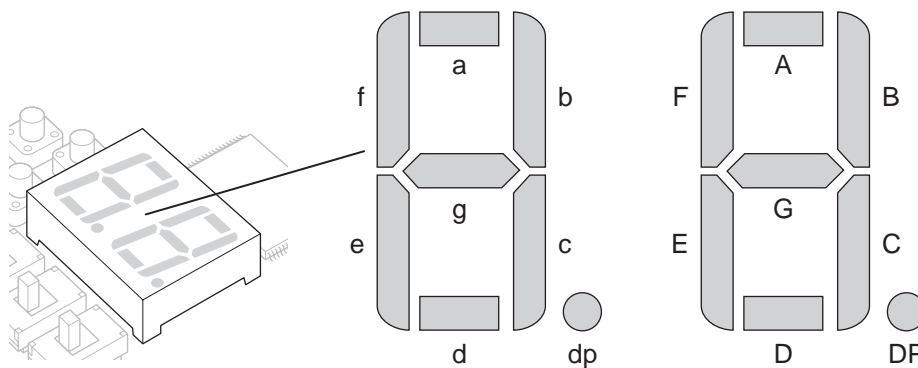
Green, surface mount LED's (model SM1206) indicate the status as shown in Table 22.

Table 22. Status LEDs

Signal Name	Description	Ref. Des.
3.3V	3.3-V power line	D1
GX_CDONE_BUF_N	Indicates Stratix GX configuration is finished.	D7
S_CDONE_BUF_N	Indicates Stratix configuration is finished.	D6

Seven-Segment Displays

Two dual-digit, seven-segment LED displays are provided for the user. Each display is controlled by either the Stratix device or the Stratix GX device. Each segment of the display can be illuminated by driving the connected device's I/O pin with a logic 0. Figure 8 shows the name of each segment.

Figure 8. Seven-Segment Displays

Tables 23 and 24 show the display segment (model LDD-A514RI) and assignments for the seven-segment displays.

Table 23. Stratix GX Dual-Digit Seven-Segment Display Pinouts

Display Segment	Display Connection	Signal Name	FPGA Connection
a	D9.16	GX_DIG_1_A	U7.C28
b	D9.15	GX_DIG_1_B	U7.B28
c	D9.3	GX_DIG_1_C	U7.C27
d	D9.2	GX_DIG_1_D	U7.B27
e	D9.1	GX_DIG_1_E	U7.A27
f	D9.18	GX_DIG_1_F	U7.D26
g	D9.17	GX_DIG_1_G	U7.C26
dp	D9.4	GX_DIG_1_DP	U7.B26
A	D9.11	GX_DIG_2_A	U7.A28
B	D9.10	GX_DIG_2_B	U7.D25
C	D9.8	GX_DIG_2_C	U7.D23
D	D9.6	GX_DIG_2_D	U7.B21
E	D9.5	GX_DIG_2_E	U7.F20
F	D9.12	GX_DIG_2_F	U7.C29
G	D9.7	GX_DIG_2_G	U7.B29
DP	D9.9	GX_DIG_2_DP	U7.A29

Table 24. Stratix Dual-Digit Seven-Segment Display Pinouts

Display Segment	Display Connection	Signal Name	FPGA Connection
a	D8.16	S_DIG_1_A	U15.AH18
b	D8.15	S_DIG_1_B	U15.AJ18
c	D8.3	S_DIG_1_C	U15.AD19
d	D8.2	S_DIG_1_D	U15.AE20
e	D8.1	S_DIG_1_E	U15.AG20
f	D8.18	S_DIG_1_F	U15.AG21
g	D8.17	S_DIG_1_G	U15.AD20
dp	D8.4	S_DIG_1_DP	U15.AB19
A	D8.11	S_DIG_2_A	U15.AD21
B	D8.10	S_DIG_2_B	U15.AG23
C	D8.8	S_DIG_2_C	U15.AC21
D	D8.6	S_DIG_2_D	U15.AF22
E	D8.5	S_DIG_2_E	U15.AD22
F	D8.12	S_DIG_2_F	U15.AB21
G	D8.7	S_DIG_2_G	U15.AA21
DP	D8.9	S_DIG_2_DP	U15.AK18

RS-232 Port

The board provides a standard RS-232 serial interface for both the Stratix and Stratix GX devices. Male DB9 connectors are used with standard PC serial port pin outs. A dedicated level-shifting buffer is used to translate between LVTTTL and RS-232 levels.

The signals listed in Tables 25 and 26 are relative to the RS-232/DB-9 specification and the “FPGA Type” should be considered relative to the Stratix or Stratix GX devices as far as the I/O setting and direction. .

Table 25. RS-232 Connector Pinout for the Stratix GX Device

Signal Name	Description	FPGA Type	FPGA Connection	Connector
GX_RS232_TXD	Transmit data	LVTTTL output	U7.H21	J124
GX_RS232_RTS	Request to send	LVTTTL output	U7.G21	J124
GX_RS232_RXD	Receive data	LVTTTL input	U7.F25	J124
GX_RS232_CTS	Clear to send	LVTTTL input	U7.H23	J124

Table 26. RS-232 Connector Pinout for the Stratix Device

Signal Name	Description	FPGA Type	FPGA Connection	Connector
S_RS232_TXD	Transmit data	LVTTL output	U15.W24	J124
S_RS232_RTS	Request to send	LVTTL output	U15.W23	J124
S_RS232_RXD	Receive data	LVTTL input	U15.Y27	J124
S_RS232_CTS	Clear to send	LVTTL input	U15.Y28	J124

Agilent Logic Analyzer Connectors

The evaluation board possesses two connectors (J57 and J58) for use with an Agilent E5387A logic analyzer probe. The Agilent probes provide less than 0.7-pF loading and claim to allow for signals with rise/fall times as short as 150 pS with minimal timing disturbances when routed in the manner suggest in “Soft Touch Connectorless Logic Analyzer Probes, Agilent models E5387A, E5390A.” Table 27 lists the signals provided to these logic analyzer connectors.

Table 27. Agilent Logic Analyzer Connector to Stratix GX Pinouts (Part 1 of 3)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector (J108)
DIFF_RX_RDCLK_N	U32	J57.A13	9B
DIFF_RX_RDCLK_P	U31	J57.B13	9A
DIFF_RX_N0	AH32	J57.A1	10D
DIFF_RX_P0	AH31	J57.B1	10C
DIFF_RX_N1	AG30	J57.A2	9H
DIFF_RX_P1	AG29	J57.B2	9G
DIFF_RX_N2	AG32	J57.A4	9D
DIFF_RX_P2	AG31	J57.B4	9C
DIFF_RX_N3	AF32	J57.A5	10F
DIFF_RX_P3	AF31	J57.B5	10E
DIFF_RX_N4	AF30	J57.A7	10B
DIFF_RX_P4	AF29	J57.B7	10A
DIFF_RX_N5	AD30	J57.A8	9F
DIFF_RX_P5	AD29	J57.B8	9E
DIFF_RX_N6	AE30	J57.A10	8F
DIFF_RX_P6	AE29	J57.B10	8E
DIFF_RX_N7	AE32	J57.A11	8D
DIFF_RX_P7	AE31	J57.B11	8C

Table 27. Agilent Logic Analyzer Connector to Stratix GX Pinouts (Part 2 of 3)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector (J108)
DIFF_RX_N8	AD32	J57.A15	7F
DIFF_RX_P8	AD31	J57.B15	7E
DIFF_RX_N9	AC30	J57.A16	8B
DIFF_RX_P9	AC29	J57.B16	8A
DIFF_RX_N10	AB30	J57.A18	7B
DIFF_RX_P10	AB29	J57.B18	7A
DIFF_RX_N11	AA30	J57.A19	7H
DIFF_RX_P11	AA29	J57.B19	7G
DIFF_RX_N12	AB32	J57.A21	6B
DIFF_RX_P12	AB31	J57.B21	6A
DIFF_RX_N13	Y30	J57.A22	6D
DIFF_RX_P13	Y29	J57.B22	6C
DIFF_RX_N14	AC32	J57.A24	7D
DIFF_RX_P14	AC31	J57.B24	7C
DIFF_RX_P15	AA32	J57.A25	6H
DIFF_RX_P15	AA31	J57.B25	6G
DIFF_TX_TDCLK_N	M26	J58.A13	3H
DIFF_TX_TDCLK_P	M25	J58.B13	3G
DIFF_TX_N0	R26	J58.A1	2H
DIFF_TX_P0	R25	J58.B1	2G
DIFF_TX_N1	R28	J58.A2	1D
DIFF_TX_P1	R27	J58.B2	1C
DIFF_TX_N2	P28	J58.A4	1B
DIFF_TX_P2	P27	J58.B4	1A
DIFF_TX_N3	R24	J58.A5	1F
DIFF_TX_P3	P24	J58.B5	1E
DIFF_TX_N4	P26	J58.A7	3F
DIFF_TX_P4	P25	J58.B7	3E
DIFF_TX_N5	N28	J58.A8	1H
DIFF_TX_P5	N27	J58.B8	1G
DIFF_TX_N6	N26	J58.A10	3B
DIFF_TX_P6	N25	J58.B10	3A
DIFF_TX_N7	M28	J58.A11	2B

Table 27. Agilent Logic Analyzer Connector to Stratix GX Pinouts (Part 3 of 3)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector (J108)
DIFF_TX_P7	M27	J58.B11	2A
DIFF_TX_N8	L27	J58.A15	4H
DIFF_TX_P8	L26	J58.B15	4G
DIFF_TX_N9	L25	J58.A16	2F
DIFF_TX_P9	L24	J58.B16	2E
DIFF_TX_N10	K25	J58.A18	4B
DIFF_TX_P10	K24	J58.B18	4A
DIFF_TX_N11	J25	J58.A19	4D
DIFF_TX_P11	J24	J58.B19	4C
DIFF_TX_N12	K28	J58.A21	4F
DIFF_TX_P12	L28	J58.B21	4E
DIFF_TX_N13	H25	J58.A22	5F
DIFF_TX_P13	H24	J58.B22	5E
DIFF_TX_N14	H27	J58.A24	3D
DIFF_TX_P14	H26	J58.B24	3C
DIFF_TX_N15	H28	J58.A25	5H
DIFF_TX_P15	J28	J58.B25	5G

MICTOR Connectors

The Stratix and Stratix GX devices connect to MICTOR connectors (model 2-767004-2_SMT38) for general use. Tables 28 and 29 list the applicable signals. Figure 9 shows the MICTOR connector on the Stratix GX Development Board.

Figure 9. MICTOR Connector**Table 28. MICTOR Connections for the Stratix GX Connector (Part 1 of 2)**

Signal Name	Stratix GX (U7)	MICTOR Connector (J34)
GX_MICTOR_EP_CLK	H9	5
GX_MICTOR_EP_15	J12	7
GX_MICTOR_EP_14	G11	9
GX_MICTOR_EP_13	L11	11
GX_MICTOR_EP_12	J11	13
GX_MICTOR_EP_11	H11	15
GX_MICTOR_EP_10	K11	17
GX_MICTOR_EP_9	G10	19
GX_MICTOR_EP_8	K10	21
GX_MICTOR_EP_7	J10	23
GX_MICTOR_EP_6	L9	25
GX_MICTOR_EP_5	H8	27
GX_MICTOR_EP_4	G9	29
GX_MICTOR_EP_3	K9	31
GX_MICTOR_EP_2	J9	33
GX_MICTOR_EP_1	K8	35
GX_MICTOR_EP_0	J8	37
GX_MICTOR_OP_CLK	G12	6
GX_MICTOR_OP_15	A14	8
GX_MICTOR_OP_14	A15	10
GX_MICTOR_OP_13	C14	12
GX_MICTOR_OP_12	H15	14
GX_MICTOR_OP_11	G15	16
GX_MICTOR_OP_10	J14	18
GX_MICTOR_OP_9	H14	20
GX_MICTOR_OP_8	E14	22
GX_MICTOR_OP_7	F14	24
GX_MICTOR_OP_6	D14	26

Table 28. MICTOR Connections for the Stratix GX Connector (Part 2 of 2)

Signal Name	Stratix GX (U7)	MICTOR Connector (J34)
GX_MICTOR_OP_5	G13	28
GX_MICTOR_OP_4	K13	30
GX_MICTOR_OP_3	L13	32
GX_MICTOR_OP_2	J13	34
GX_MICTOR_OP_1	H13	36
GX_MICTOR_OP_0	L12	38

Table 29. MICTOR Connections for the Stratix Connector (Part 1 of 2)

Signal Name	Stratix (U15)	Connector (J75)
S_MICTOR_EP_CLK	F5	5
S_MICTOR_EP_15	J3	7
S_MICTOR_EP_14	H2	9
S_MICTOR_EP_13	H1	11
S_MICTOR_EP_12	G2	13
S_MICTOR_EP_11	G1	15
S_MICTOR_EP_10	H4	17
S_MICTOR_EP_9	H3	19
S_MICTOR_EP_8	F2	21
S_MICTOR_EP_7	F1	23
S_MICTOR_EP_6	G4	25
S_MICTOR_EP_5	G3	27
S_MICTOR_EP_4	F4	29
S_MICTOR_EP_3	F3	31
S_MICTOR_EP_2	E1	33
S_MICTOR_EP_1	E2	35
S_MICTOR_EP_0	E4	37
S_MICTOR_OP_CLK	J4	6
S_MICTOR_OP_15	N2	8
S_MICTOR_OP_14	N1	10
S_MICTOR_OP_13	N4	12
S_MICTOR_OP_12	N3	14
S_MICTOR_OP_11	M3	16
S_MICTOR_OP_10	M2	18

Table 29. MICTOR Connections for the Stratix Connector (Part 2 of 2)

Signal Name	Stratix (U15)	Connector (J75)
S_MICTOR_OP_9	L3	20
S_MICTOR_OP_8	L2	22
S_MICTOR_OP_7	P4	24
S_MICTOR_OP_6	P3	26
S_MICTOR_OP_5	K2	28
S_MICTOR_OP_4	L1	30
S_MICTOR_OP_3	J1	32
S_MICTOR_OP_2	J2	34
S_MICTOR_OP_1	K3	36
S_MICTOR_OP_0	K4	38

20-Pin Headers

Two 20-pin header connectors provide test connections for both the Stratix and Stratix GX devices. The 20-pin connector connected to the Stratix U15 is J68. The 20-pin connector connected to the Stratix GX U7 is J53. See Tables 30 and 31. Figure 10 shows the 20-pin header.

Figure 10. 20-Pin Header**Table 30. 20-Pin Connections for the Stratix GX Connector**

Signal Name	Stratix GX (U7)	Connector (J53)
GX_HEADER0	D21	1
GX_HEADER1	A21	3
GX_HEADER2	A22	5
GX_HEADER3	C22	7
GX_HEADER4	D22	9
GX_HEADER5	B22	11
GX_HEADER6	E22	13
GX_HEADER7	A23	15
GX_HEADER8	B23	17
GX_HEADER9	C23	19

Table 30. 20-Pin Connections for the Stratix GX Connector

Signal Name	Stratix GX (U7)	Connector (J53)
GX_HEADER10	E23	20
GX_HEADER11	A24	18
GX_HEADER12	B24	16
GX_HEADER13	C24	14
GX_HEADER14	D24	12
GX_HEADER15	A25	10
GX_HEADER16	B25	8
GX_HEADER17	C25	6
GX_HEADER18	A26	4
GX_HEADER19	E25	2

Table 31. 20-Pin Connections for the Stratix Connector

Signal Name	Stratix (U15)	Connector (J68)
S_HEADER0	AA29	1
S_HEADER1	AA28	3
S_HEADER2	AB30	5
S_HEADER3	AB31	7
S_HEADER4	AA30	9
S_HEADER5	AA31	11
S_HEADER6	Y29	13
S_HEADER7	Y30	15
S_HEADER8	Y31	17
S_HEADER9	Y32	19
S_HEADER10	W29	20
S_HEADER11	W30	18
S_HEADER12	W31	16
S_HEADER13	W32	14
S_HEADER14	V29	12
S_HEADER15	V30	10
S_HEADER16	V31	8
S_HEADER17	V32	6
S_HEADER18	Y23	4
S_HEADER19	Y25	2

High-speed Connectors

The Stratix GX Development Board offers the following high-speed connectors:

- Four or five transceiver blocks with four full duplex 3.125-Gbps transceiver channels per block
- 39 or 45 source synchronous channels
- 20 full-duplex channels to HM-Zd connector
- Channels connected to SMAs for DPA analysis
- Four transceivers interface to 10GE XPAK module
- Same HM-Zd connector

Stratix GX & HM-Zd Interface (J1)

The HM-Zd connector J1 conforms to the XAUI standard to allow communication over the Tyco backplane.

The receiver and transmitter traces going to J1 (XCVR_RX_N[8..11], XCVR_RX_P[8..11], XCVR_TX_N[8..11], and XCVR_TX_P[8..11]) are routed with 100- Ω differential impedance transmission lines and are 4,822 mils \pm 50 mils in length. The receiver lines are expected to have an impedance drop due to the pad widths of the 0402 size, AC-coupling capacitors. The transmitter lines are DC-coupled. Table 32 lists the high-speed signals connected to J1 and the pin number on the Stratix GX device. Figure 11 shows the HM-Zd connector on the Stratix GX Development Board.

Figure 11. HM-Zd Connector

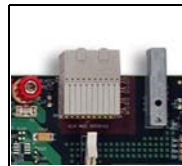


Table 32. HM-Zd to Stratix GX Connection (Part 1 of 2)

Signal Name (HM-Zd J1)	Stratix GX Pin	HM-Zd (J1)
XCVR_RX_N8	AD2	6A
XCVR_RX_P8	AD1	6B
XCVR_RX_N9	AB2	6C
XCVR_RX_P9	AB1	6D

Table 32. HM-Zd to Stratix GX Connection (Part 2 of 2)

Signal Name (HM-Zd J1)	Stratix GX Pin	HM-Zd (J1)
XCVR_RX_N10	AH2	6E
XCVR_RX_P10	AH1	6F
XCVR_RX_N11	AK2	6G
XCVR_RX_P11	AK1	6H
XCVR_TX_N8	AC5	5B
XCVR_TX_P8	AC4	5A
XCVR_TX_N9	AA5	5D
XCVR_TX_P9	AA4	5C
XCVR_TX_N10	AE5	5F
XCVR_TX_P10	AE4	5E
XCVR_TX_N11	AG5	5H
XCVR_TX_P11	AG4	5G

Stratix GX SMA Interface

The SMA signals (XCVR_RX_P[2..3], XCVR_RX_N[2..3], XCVR_TX_P[2..3], XCVR_TX_N[2..3]) are routed using surface mount (center pin), through-hole (ground pins) SMA connectors and 100- Ω differential impedance transmission lines with a length of 2,732 mils \pm 50 mils. The receiver lines are AC-coupled, the transmitter lines are DC-coupled. Table 33 lists the connector and Stratix GX device assignments for the SMA interface. Figure 12 shows the SMA interface on the Stratix GX Development Board.

Figure 12. SMA Interface**Table 33. Stratix GX SMA Interface (Part 1 of 2)**

Signal Name	SMA Connector	Stratix GX Pin
XCVR_RX_N2	J27	H2
XCVR_RX_P2	J19	H1

Table 33. Stratix GX SMA Interface (Part 2 of 2)

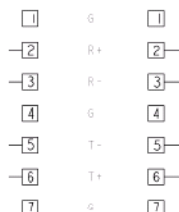
Signal Name	SMA Connector	Stratix GX Pin
XCVR_RX_N3	J26	K2
XCVR_RX_P3	J18	K1
XCVR_TX_N2	J28	J5
XCVR_TX_P2	J20	J4
XCVR_TX_N3	J25	L5
XCVR_TX_P3	J17	L4

High-Speed Serial Data Connector

High-speed serial data connector (HSSDC2) interface is provided for use with the EP1SGX40 device (see Figure 13). The HSSDC2 interface is designed to facilitate data transfer rates up to 5.0 Gbps. The connector uses a smaller form factor than previous HSSDC products. Plugs are die cast with a stamped latch/ground spring, impedance controlled PCB and seven high-speed contact pads. The receptacles have six chassis ground locations, six PCB grounding/retention contacts, four grounding contacts for the plug-in cable, and a metal EMI/RFI shield. The plug and receptacle have polarization and keying.

Figure 13. HSSDC2 Interface

The connector can accept cable from 22 to 30 AWG and uses an overmolded strain relief. The connector provides for positive latching and maintains 2.5 Gbps rates up to 15 meters. Some of the applications the connector can be used for include InfiniBand 1× Server I/O 2.5 Gbps, Fibre Channel small form-factor (SFF) Copper 2.1-, 3.125-, and 5.0-Gbps applications, and small form-factor pluggable (SFP) Copper Module I/O standard. Figure 14 shows the HSSDC2 interface pinout.

Figure 14. HSSDC2 Interface Pinout

All receiver and transmitter data lines to the HSSDC2 connectors (XCVR_RX_N[16..19], XCVR_RX_P[16..19], XCVR_TX_N[16..19], and XCVR_TX_P[16..19]) are routed with 100-Ω differential impedance lines and are 5,398 mils ±50 mils in length. The receiver lines are AC-coupled, and the transmitter lines are DC-coupled. Table 34 lists the connector and pin assignments.

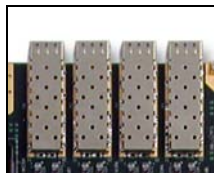
Table 34. HSSDC2 Connector to Stratix GX Pinout

Signal Name	Connector	Stratix GX
XCVR_RX_N16	J23.2	P2
XCVR_RX_P16	J23.3	P1
XCVR_TX_N16	J23.6	R5
XCVR_TX_P16	J23.5	R4
XCVR_RX_N17	J32.2	M2
XCVR_RX_P17	J32.3	M1
XCVR_TX_N17	J32.6	N5
XCVR_TX_P17	J32.5	N4
XCVR_RX_N18	J15.2	V2
XCVR_RX_P18	J15.3	V1
XCVR_TX_N18	J15.6	U5
XCVR_TX_P18	J15.5	U4
XCVR_RX_N19	J11.2	Y2
XCVR_RX_P19	J11.3	Y1
XCVR_TX_N19	J11.6	W5
XCVR_TX_P19	J11.5	W4

Small Form-Factor Pluggable (SFP) Transceiver

The board has a 20-contact, right angle surface mount SFP transceiver connector (see Figure 15).

Figure 15. SFP Transceiver Connector



The SFP transceiver contains a printed circuit board that mates with the SFP electrical connector. Figure 16 shows the electrical pad layout. The pads are designed for sequenced mating as shown in Table 35.

Table 35. Pad-Contact Mating	
Mate	Contact
First mate	Ground contacts
Second mate	Power contacts
Third mate	Signal contacts

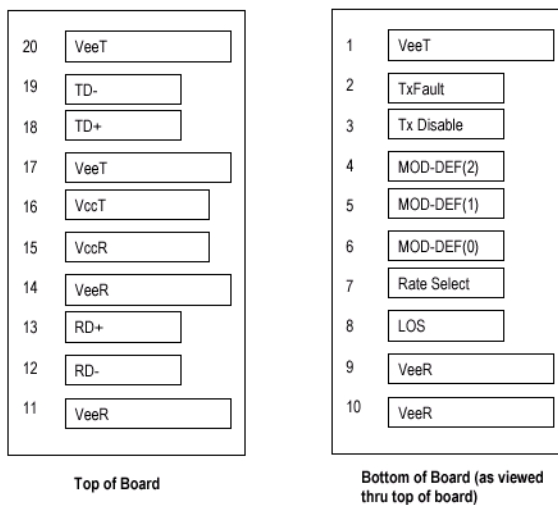
Figure 16. SFP Transceiver Electrical Pad Layout

Table 36 defines the pin functions. Figure 17 shows the interface of the SFP connector to the Stratix GX device. Standard board layout uses practices, such as connections to V_{CC} and ground with vias, use of short- and equal-length differential signal lines, use of microstrip-lines and 50- Ω terminations.

The SFP data signals are with 100- Ω differential transmission lines with a length of 3,491 mils \pm 50 mils. Both the receiver and transmitter lines are DC-coupled.

Table 37 shows the connector and Stratix GX device assignments



For electromagnetic interference (EMI) protection the signals to the 20-pin connector should be shut off when the transceiver is removed.

Table 36. Plug Sequence: Pin Engagement Sequence During Hot-plugging

Pin Number	Name	Function	Plug Sequence	Comment
1	VeeT	Transmitter ground	1	
2	TX fault	Transmitter fault indication	3	(1)
3	TX disable	Transmitter disable	3	Module disables on high or open (2)
4	MOD_DEF2	Module definition 2	3	Two-wire serial ID interface (3)
5	MOD_DEF1	Module definition 1	3	Two-wire serial ID interface (3)
6	MOD_DEF0	Module definition 0	3	Grounded in module (3)
7	Rate select	Select between full or reduced receiver bandwidth	3	Low or open - reduced bandwidth High - full bandwidth (4)
8	LOS	Loss of signal	3	(5)
9	VeeR	Receiver ground	1	(6)
10	VeeR	Receiver ground	1	(6)
11	VeeR	Receiver ground	1	(6)
12	RD-	Invert received data out	3	(7)
13	RD+	Received data out	3	(7)
14	VeeR	Receiver ground	1	(6)
15	VccR	Receiver power	2	3.3 V \pm 5% (8)
16	VccT	Transmitter power	2	3.3 V \pm 5% (8)
17	VeeT	Transmitter ground	1	(6)
18	TD+	Transmit data in	3	(9)
19	TD-	Invert transmit data in	3	(9)

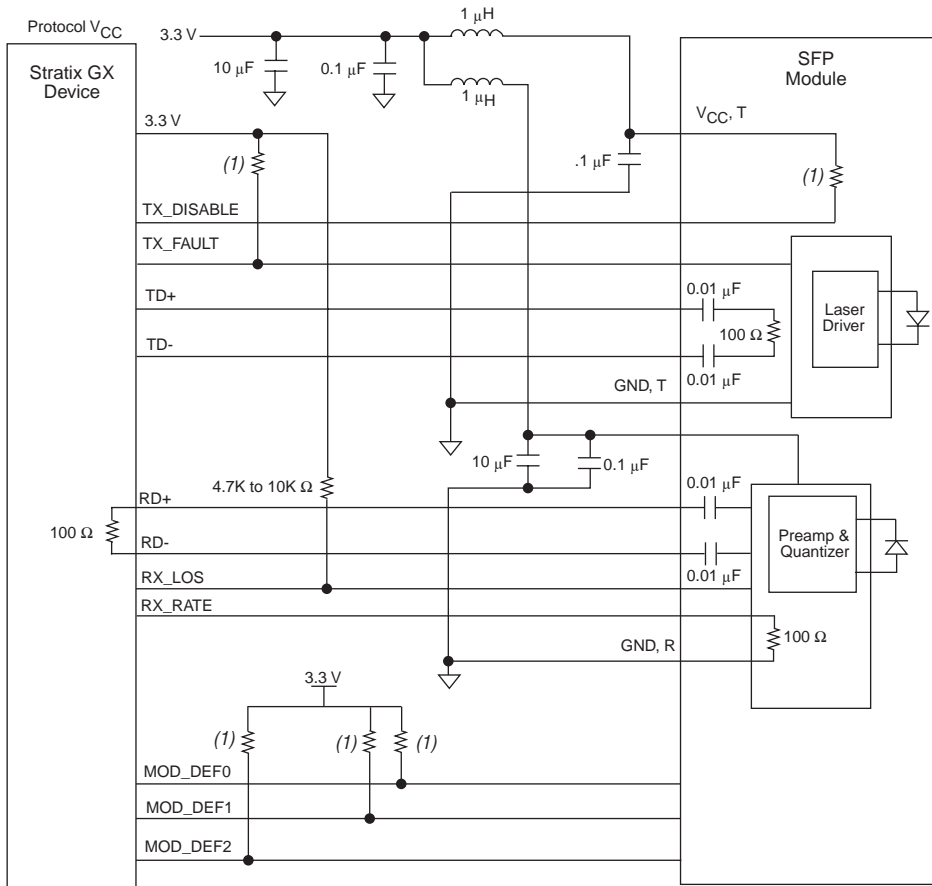
Table 36. Plug Sequence: Pin Engagement Sequence During Hot-plugging

Pin Number	Name	Function	Plug Sequence	Comment
20	VeeT	Transmitter ground	1	(6)

Notes for Table 36:

- (1) TX fault is an open collector/drain output, which should be pulled up with a 4.7 K to 10-K Ω resistor on the host board. The pull-up voltage is between 2.0 V and $V_{CCT} + 0.3$ V and $V_{CCR} + 0.3$ V.
High output indicates a laser fault of some kind.
Low output indicates normal operation. In the low state, the output is pulled to < 0.8 V.
- (2) TX disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7 K to 10-K Ω resistor. The input states are:
Low (0 to 0.8V): Transmitter on
(>0.8, < 2.0V): Undefined
High (2.0 to 3.465V): Transmitter Disabled
Open: Transmitter Disabled
- (3) MOD_DEF0, MOD_DEF1, and MOD_DEF2 are the module definition pins. They should be pulled up with a 4.7 K to 10-K Ω resistor on the host board. The pull-up voltage shall be V_{CCT} or V_{CCR} .
MOD_DEF 0 is grounded by the module to indicate that the module is present.
MOD_DEF1 is the clock line of the two wire serial interface for serial ID.
MOD_DEF2 is the data line of the two wire serial interface for serial ID.
- (4) This is an optional input used to control the receiver bandwidth for compatibility with multiple data rates (most likely Fibre Channel 1 \times and 2 \times Rates). If implemented, the input is internally pulled down with > 30-K Ω resistor. The input states are:
Low (0 to 0.8 V): reduced bandwidth
(>0.8, < 2.0 V): undefined
High (2.0 to 3.465 V): full bandwidth
Open: reduced bandwidth
- (5) LOS (loss of signal) is an open collector/drain output, which should be pulled up with a 4.7 K to 10-K Ω resistor. Pull up voltage between 2.0 V and $V_{CCT} + 0.3$ V and $V_{CCR} + 0.3$ V.
When high, this output indicates the received optical power is below the worst-case receiver sensitivity (as defined by the standard in use).
Low indicates normal operation. In the low state, the output is pulled to < 0.8 V.
- (6) VeeR and VeeT may be internally connected within the SFP module.
- (7) RD- and RD+ are the differential receiver outputs. They are AC coupled 100- Ω differential lines which should be terminated with a 100- Ω (differential) resistor at the Stratix GX device. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines is between 370 and 2,000 mV differential (185 to 1,000 mV single ended) when properly terminated.
- (8) V_{CCR} and V_{CCT} are the receiver and transmitter power supplies, respectively. They are defined as 3.3 V \pm 5% at the SFP connector pin. Maximum supply current is 300 mA. Recommended host board power supply filtering is shown *Note (9)*. Inductors with DC resistance of less than specific values should be used in order to maintain the required voltage at the SFP input pin with 3.3-V supply voltage. When the recommended supply filtering network is used, hot plugging of the SFP transceiver module results in an inrush current of no more than 30 mA greater than the steady state value. V_{CCR} and V_{CCT} may be internally connected within the SFP transceiver module.
- (9) TD- and TD+ are the differential transmitter inputs. They are AC-coupled, differential lines with 100- Ω differential termination inside the module. The AC-coupling is done inside the module and is thus not required on the host board. The inputs accept differential swings of 500 to 2,400 mV (250 to 1,200 mV single-ended), though it is recommended that values between 500 and 1,200 mV differential (250 to 600 mV single-ended) be used for best EMI performance.

Figure 17. SFP Connector Interface to the Stratix GX Device



Note to Figure 17:

(1) This resistor is between 4.7 KΩ and 10 KΩ.

Table 37. SFP Connector Interface to the Stratix GX Device

Signal Name	SFP Module	Stratix GX
XCVR_RX_N4	J54.12	B10
XCVR_RX_P4	J54.13	A10
XCVR_TX_N4	J54.19	E10
XCVR_TX_P4	J54.18	D10

Table 37. SFP Connector Interface to the Stratix GX Device

Signal Name	SFP Module	Stratix GX
XCVR_RX_N5	J64.12	B12
XCVR_RX_P5	J64.13	A12
XCVR_TX_N5	J64.19	E12
XCVR_TX_P5	J64.18	D12
XCVR_RX_N6	J45.12	B6
XCVR_RX_P6	J45.13	A6
XCVR_TX_N6	J45.19	E8
XCVR_TX_P6	J45.18	D8
XCVR_RX_N7	J38.12	B4
XCVR_RX_P7	J38.13	A4
XCVR_TX_N7	J38.19	E6
XCVR_TX_P7	J38.18	D6

XPAK Transceiver Connector

The Stratix GX Development Board has a 10G XPAK transceiver connector. The XPAK connector is a 70-way two-row connector, similar in style to the 20-way SFP connector. The electrical pad layout is illustrated in Figure 18.

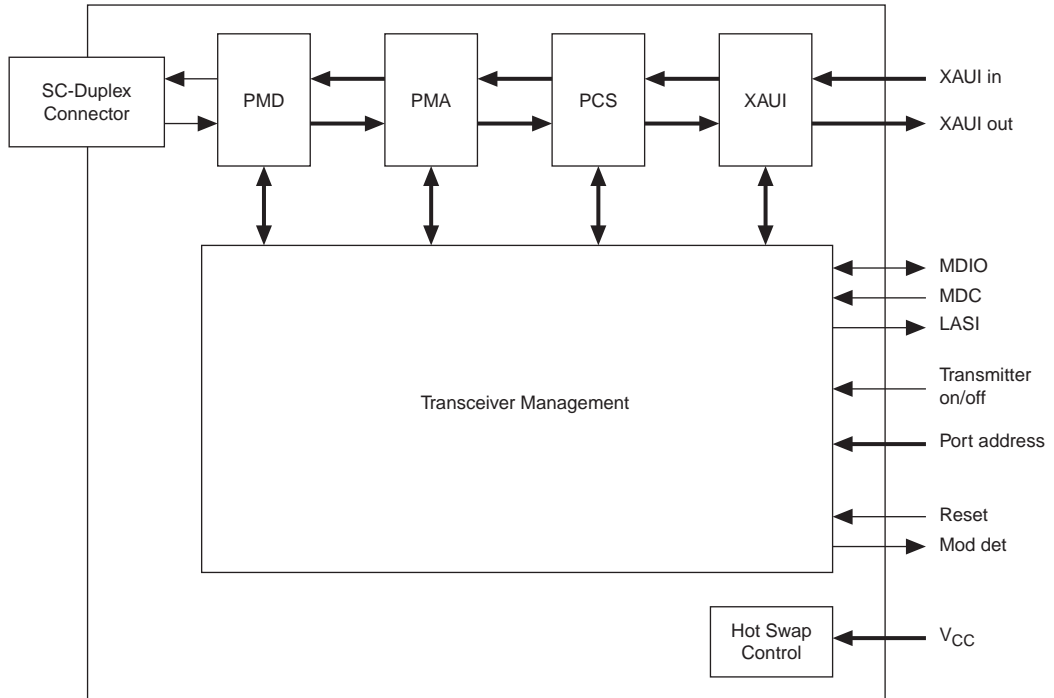
Figure 18. XPAK Transceiver Electrical Pad Layout

1	GND	GND	70
2	GND	GND	69
3	GND	RESERVED	68
4	5.0V	RESERVED	67
5	3.3V	GND	66
6	3.3V	TX LANE3-	65
7	APS	TX LANE3+	64
8	APS	GND	63
9	LAS1	TX LANE2-	62
10	RESET	TX LANE2+	61
11	VEND SPECIFIC	GND	60
12	TX ON/OFF	TX LANE1-	59
13	RESERVED	TX LANE1+	58
14	MOD DETECT	GND	57
15	VEND SPECIFIC	TX LANE0-	56
16	VEND SPECIFIC	TX LANE0+	55
17	MDIO	GND	54
18	MDC	GND	53
19	PRTAD4	GND	52
20	PRTAD3	RX LANE3-	51
21	PRTAD2	RX LANE3+	50
22	PRTAD1	GND	49
23	PRTAD0	RX LANE2-	48
24	VEND SPECIFIC	RX LANE2+	47
25	APS SET	GND	46
26	RESERVED	RX LANE1-	45
27	APS SENSE	RX LANE1+	44
28	APS	GND	43
29	APS	RX LANE0-	42
30	3.3V	RX LANE0+	41
31	3.3V	GND	40
32	5.0V	RESERVED	39
33	GND	RESERVED	38
34	GND	GND	37
35	GND	GND	36

A typical contact pad plating for the printed circuit board is 0.38- μm minimum hard gold over 1.27- μm minimum thick nickel. Other plating options that meet the performance requirements are acceptable. The XPAK module will be functionally operational within five seconds of insertion. 5.0-V and 3.3-V power supplies and an APS rail are supplied to the XPAK transceiver connector.

Figure 19 illustrates a typical functional diagram of a XPAK transceiver.

Figure 19. Functional Diagram of Typical XPAK Style Transceiver



The XPAK receiver and transmitter traces (XCVR_TX_N[12..15], XCVR_TX_P[12..15], XCVR_RX_N[12..15], XCVR_RX_P[12..15]) are routed with 100-Ω differential impedance transmission lines and are 5,411 mils ±50 mils in length.

Table 38 lists the Stratix GX device assignments for the XPAK data signals. The XPAK pin functions are also defined in Table 38.

Table 38. XPAK Pin Definitions & Stratix GX Pinout (Part 1 of 4)

Pin Number	XPAK Name	I/O Direction	Stratix GX Signal Name	Stratix GX Pin Number (U7)	Function
1	GND		HSSI_GND		Electrical ground (1)
2	GND		HSSI_GND		Electrical ground (1)
3	GND		HSSI_GND		Electrical ground (1)

Table 38. XPAK Pin Definitions & Stratix GX Pinout (Part 2 of 4)

Pin Number	XPAK Name	I/O Direction	Stratix GX Signal Name	Stratix GX Pin Number (U7)	Function
4	5.0V		5.0V		Power (2)
5	3.3V		3.3V		Power (2)
6	3.3V		3.3V		Power (2)
7	APS		APS		Adaptive power supply (2)
8	APS		APS		Adaptive power supply (2)
9	LASI		XPAK_LASI	AH26	Open drain compatible 10K-22K pull up on host Logic high - normal operation Logic low - LASI asserted (3)
10	RESET	I	XPAK_X_RST	AE23	Logic high - normal operation Logic low - reset (3)
11	VEND SPECIFIC		XPAK_VEND0	AJ28	Vendor specific pin. Leave unconnected when not in use. (6)
12	TX ON/OFF	I	XPAK_TX_ON	AF23	Open drain compatible 10K-22K pull-up on transceiver Logic high - transmitter on (capable) Logic low - transmitter off (always) (3)
13	RESERVED		RESERVED		Reserved (3)
14	MOD DETECT	O	XPAK_MOD_DET	AE21	Pulled low inside module through 1K
15	VEND SPECIFIC		XPAK_VEND1	AF24	Vendor specific pin. Leave unconnected when not in use. (6)
16	VEND SPECIFIC		XPAK_VEND2	AC22	Vendor specific pin. Leave unconnected when not in use. (6)
17	MDIO	I/O	XPAK_MDIO		Management data I/O (3), (4)
18	MDC	I	XPAK_MDC		Management data clock (3), (4)
19	PRTAD4	I	XPAK_PRTAD[4]	AB22	Port address bit 4 (low = 0) (3)
20	PRTAD3	I	XPAK_PRTAD[3]	AL30	Port address bit 4 (low = 0) (3)
21	PRTAD2	I	XPAK_PRTAD[2]	AL31	Port address bit 4 (low = 0) (3)
22	PRTAD1	I	XPAK_PRTAD[1]	AK30	Port address bit 4 (low = 0) (3)
23	PRTAD0	I	XPAK_PRTAD[0]	AK31	Port address bit 4 (low = 0) (3)

Table 38. XPAK Pin Definitions & Stratix GX Pinout (Part 3 of 4)

Pin Number	XPAK Name	I/O Direction	Stratix GX Signal Name	Stratix GX Pin Number (U7)	Function
24	VEND SPECIFIC		XPAK_VEND3	AD22	Vendor specific pin. Leave unconnected when not in use. (6)
25	APS SET		APS SET		Feedback input for APS
26	RESERVED		RESERVED		Reserved for avalanche photodiode use (6)
27	APS SENSE		APS SENSE		APS sense connection
28	APS		APS		Adaptive power supply (2)
29	APS		APS		Adaptive power supply (2)
30	3.3V		3.3V		Power (2)
31	3.3V		3.3V		Power (2)
32	5.0V		5.0V		Power (2)
33	GND		HSSI_GND		Electrical ground (1)
34	GND		HSSI_GND		Electrical ground (1)
35	GND		HSSI_GND		Electrical ground (1)
36	GND		HSSI_GND		Electrical ground (1)
37	GND		HSSI_GND		Electrical ground (1)
38	RESERVED		RESERVED		Reserved
39	RESERVED		RESERVED		Reserved
40	GND		HSSI_GND		Electrical ground (1)
41	RX LANE0+	O	XCVR_RX_P12	AM5	Module XAUI output lane 0+ (5)
42	RX LANE0-	O	XCVR_RX_N12	AL5	Module XAUI output lane 0- (5)
43	GND		HSSI_GND		Electrical ground (1)
44	RX LANE1-	O	XCVR_RX_P13	AM2	Module XAUI output lane 1+ (5)
45	RX LANE1-	O	XCVR_RX_N13	AM3	Module XAUI output lane 1- (5)
46	GND		HSSI_GND		Electrical ground (1)
47	RX LANE2+	O	XCVR_RX_P14	AM9	Module XAUI output lane 2+ (5)
48	RX LANE2-	O	XCVR_RX_N14	AL9	Module XAUI output lane 2- (5)
49	GND		HSSI_GND		Electrical ground (1)
50	RX LANE3+	O	XCVR_RX_P15	AM11	Module XAUI output lane 3+ (5)
51	RX LANE3-	O	XCVR_RX_N15	AL11	Module XAUI output lane 3- (5)
52	GND		HSSI_GND		Electrical ground (1)
53	GND		HSSI_GND		Electrical ground (1)

Table 38. XPAK Pin Definitions & Stratix GX Pinout (Part 4 of 4)

Pin Number	XPAK Name	I/O Direction	Stratix GX Signal Name	Stratix GX Pin Number (U7)	Function
54	GND		HSSI_GND		Electrical ground (1)
55	TX LANE0+	I	XCVR_TX_P12	AJ7	Module XAUI input lane 0+ (5)
56	TX LANE0-	I	XCVR_TX_N12	AH7	Module XAUI input lane 0- (5)
57	GND		HSSI_GND		Electrical ground (1)
58	TX LANE1+	I	XCVR_TX_P13	AJ4	Module XAUI input lane 1+ (5)
59	TX LANE1-	I	XCVR_TX_N13	AJ5	Module XAUI input lane 1- (5)
60	GND		HSSI_GND		Electrical ground (1)
61	TX LANE2+	I	XCVR_TX_P14	AJ9	Module XAUI input lane 2+ (5)
62	TX LANE2-	I	XCVR_TX_N14	AH9	Module XAUI input lane 2- (5)
63	GND		HSSI_GND		Electrical ground (1)
64	TX LANE3+	I	XCVR_TX_P15	AJ11	Module XAUI input lane 3+ (5)
65	TX LANE3-	I	XCVR_TX_N52	AH11	Module XAUI input lane 3- (5)
66	GND		HSSI_GND		Electrical ground (1)
67	RESERVED	I	RESERVED		Reserved
68	RESERVED	I	RESERVED		Reserved
69	GND		HSSI_GND		Electrical ground (1)
70	GND		HSSI_GND		Electrical ground (1)

Notes to Table 38:

- (1) Ground connections are common for transmitters and receivers.
- (2) All connector contacts are rated at 0.5 A nominal.
- (3) This pin is 1.2-V CMOS compatible.
- (4) MDIO and MDC timing must comply with IEEE802.3ae, Clause 45.3.
- (5) XAUI output characteristics should comply with IEEE802.3ae Clause 47.
- (6) Transceivers will be MSA compliant when no signals are present on the vendor specific pins.

Stratix GX Device & Intel Backplane (SPI-4.2) Interface

This interface conforms to the SPI-4.2 standard to allow communication with the Intel backplane. Access to the transmitter and receiver data and clock lines is provided as indicated in the “Agilent Logic Analyzer Connector” columns of Table 39.



“Report #20CG015-1, Rev. A, January 29” from Amp contains recommendations for plane keep outs around the receiver and transmitter differential pairs. The keep outs on the evaluation board conform to the document’s recommended dimensions.

The lines listed in Table 39 are routed with 100- Ω differential impedance transmission lines with a length of 11,633 mils \pm 50 mils.

Table 39. Stratix Device & Intel Backplane (SPI-4.2) Interface Transmission Line Length 11,633 mils \pm 50 mils (Part 1 of 2)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector
DIFF_RX_RDCLK_N	U32	J57.A13	J108.9B
DIFF_RX_RDCLK_P	U31	J57.B13	J108.9A
DIFF_RX_N0	AH32	J57.A1	J108.10D
DIFF_RX_P0	AH31	J57.B1	J108.10C
DIFF_RX_N1	AG30	J57.A2	J108.9H
DIFF_RX_P1	AG29	J57.B2	J108.9G
DIFF_RX_N2	AG32	J57.A4	J108.9D
DIFF_RX_P2	AG31	J57.B4	J108.9C
DIFF_RX_N3	AF32	J57.A5	J108.10F
DIFF_RX_P3	AF31	J57.B5	J108.10E
DIFF_RX_N4	AF30	J57.A7	J108.10B
DIFF_RX_P4	AF29	J57.B7	J108.10A
DIFF_RX_N5	AD30	J57.A8	J108.9F
DIFF_RX_P5	AD29	J57.B8	J108.9E
DIFF_RX_N6	AE30	J57.A10	J108.8F
DIFF_RX_P6	AE29	J57.B10	J108.8E
DIFF_RX_N7	AE32	J57.A11	J108.8D
DIFF_RX_P7	AE31	J57.B11	J108.8C
DIFF_RX_N8	AD32	J57.A15	J108.7F
DIFF_RX_P8	AD31	J57.B15	J108.7E
DIFF_RX_N9	AC30	J57.A16	J108.8B
DIFF_RX_P9	AC29	J57.B16	J108.8A
DIFF_RX_N10	AB30	J57.A18	J108.7B
DIFF_RX_P10	AB29	J57.B18	J108.7A
DIFF_RX_N11	AA30	J57.A19	J108.7H
DIFF_RX_P11	AA29	J57.B19	J108.7G
DIFF_RX_N12	AB32	J57.A21	J108.6B
DIFF_RX_P12	AB31	J57.B21	J108.6A
DIFF_RX_N13	Y30	J57.A22	J108.6D

Table 39. Stratix Device & Intel Backplane (SPI-4.2) Interface Transmission Line Length 11,633 mils \pm 50 mils (Part 2 of 2)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector
DIFF_RX_P13	Y29	J57.B22	J108.6C
DIFF_RX_N14	AC32	J57.A24	J108.7D
DIFF_RX_P14	AC31	J57.B24	J108.7C
DIFF_RX_P15	AA32	J57.A25	J108.6H
DIFF_RX_P15	AA31	J57.B25	J108.6G
DIFF_RX_RSCLK	F19	None	J108.8G
DIFF_RX_RSTAT0	E21	None	J108.10H
DIFF_RX_RSTAT1	C21	None	J108.10G
DIFF_RX_RCTL_N	W30	None	J108.6F
DIFF_RX_RCTL_P	W29	None	J108.6E
DIFF_RX_DRSTAT_N0	AB23	None	J109.10H
DIFF_RX_DRSTAT_P0	AA23	None	J109.10G
DIFF_RX_DRSTAT_N1	AD23	None	J109.9H
DIFF_RX_DRSTAT_P1	AC23	None	J109.9G
DIFF_RX_DRCLK_N	U24	None	J109.8H
DIFF_RX_DRCLK_P	T23	None	J109.8G

Table 40 shows the lines routed with 100- Ω differential impedance transmission lines with a length of 11,889 mils \pm 50 mils.

Table 40. Stratix Device & Intel Backplane (SPI-4.2) Interface Transmission Line Length 1,189 mils \pm 50 mils (Part 1 of 3)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector
DIFF_TX_TDCLK_N	M26	J58.A13	J108.3H
DIFF_TX_TDCLK_P	M25	J58.B13	J108.3G
DIFF_TX_N0	R26	J58.A1	J108.2H
DIFF_TX_P0	R25	J58.B1	J108.2G
DIFF_TX_N1	R28	J58.A2	J108.1D
DIFF_TX_P1	R27	J58.B2	J108.1C
DIFF_TX_N2	P28	J58.A4	J108.1B

Table 40. Stratix Device & Intel Backplane (SPI-4.2) Interface Transmission Line Length 1,189 mils \pm 50 mils (Part 2 of 3)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector
DIFF_TX_P2	P27	J58.B4	J108.1A
DIFF_TX_N3	R24	J58.A5	J108.3F
DIFF_TX_P3	P24	J58.B5	J108.3E
DIFF_TX_N4	P26	J58.A7	J108.3F
DIFF_TX_P4	P25	J58.B7	J108.3E
DIFF_TX_N5	N28	J58.A8	J108.1H
DIFF_TX_P5	N27	J58.B8	J108.1G
DIFF_TX_N6	N26	J58.A10	J108.3B
DIFF_TX_P6	N25	J58.B10	J108.3A
DIFF_TX_N7	M28	J58.A11	J108.2B
DIFF_TX_P7	M27	J58.B11	J108.2A
DIFF_TX_N8	L27	J58.A15	J108.4H
DIFF_TX_P8	L26	J58.B15	J108.4G
DIFF_TX_N9	L25	J58.A16	J108.2F
DIFF_TX_P9	L24	J58.B16	J108.2E
DIFF_TX_N10	K25	J58.A18	J108.4B
DIFF_TX_P10	K24	J58.B18	J108.4A
DIFF_TX_N11	J25	J58.A19	J108.4D
DIFF_TX_P11	J24	J58.B19	J108.4C
DIFF_TX_N12	K28	J58.A21	J108.4F
DIFF_TX_P12	L28	J58.B21	J108.4E
DIFF_TX_N13	H25	J58.A22	J108.5F
DIFF_TX_P13	H24	J58.B22	J108.5E
DIFF_TX_N14	H27	J58.A24	J108.3D
DIFF_TX_P14	H26	J58.B24	J108.3C
DIFF_TX_N15	H28	J58.A25	J108.5H
DIFF_TX_P15	J28	J58.B25	J108.5G
DIFF_TX_TSCLK	E19	None	J108.5A
DIFF_TX_TSTAT0	D27	None	J108.2D
DIFF_TX_TSTAT1	C31	None	J108.2C
DIFF_TX_TCTL_N	G26	None	J108.5D
DIFF_TX_TCTL_P	G25	None	J108.5C

Table 40. Stratix Device & Intel Backplane (SPI-4.2) Interface Transmission Line Length 1,189 mils \pm 50 mils (Part 3 of 3)

Signal Name	Stratix GX (U7)	Agilent Logic Analyzer Connector	HM-Zd Connector
DIFF_TX_DTSTAT_N0	Y32	None	J109.2D
DIFF_TX_DTSTAT_P0	Y31	None	J109.2C
DIFF_TX_DTSTAT_N1	W31	None	J109.1D
DIFF_TX_DTSTAT_P1	V31	None	J109.1C
DIFF_TX_TSCLK	E19	None	J109.5A

Stratix GX & DPA SMA Interface

SMA connectors are provided for use with the dynamic phase alignment (DPA) feature in the Stratix GX device.

The signals in Table 41 are routed using surface mount (center pin), through-hole (ground pins) SMA connectors, 100- Ω differential impedance transmission lines and are 8,912 mils \pm 50 mils in length:

Table 41. Stratix GX & DPA SMA Interface

Signal name	SMA Connector	Stratix GX Pin
DPA_RX_N0	J89	R30
DPA_RX_P0	J84	R29
DPACLK_IN_N	J107	T32
DPACLK_IN_P	J103	T31
DPA_TX_N0	J94	AG28
DPA_TX_P0	J99	AG27
DPA_TX_N1	J102	AF26
DPA_TX_P1	J106	AF25
DPACLK_OUT_N	J88	AF28
DPACLK_OUT_P	J83	AF27
DPA_RX_N1 (1)	J100	R31
DPA_RX_P1 (1)	J95	P31

Note to Table 41:

- (1) To show that the Stratix GX device can align a mis-aligned signal, these receiver signals have an additional 4.5 inches of length added to them

XPAK Connector Pinouts

Table 38 on page 47 shows the pinouts for the XPAK connector on the Stratix GX Development Board.

RS-232 Connector Pinouts

Tables 42 and 43 show the pinouts for the RS-232 connectors on the Stratix GX Development Board.

Table 42. RS-232 Connector to Stratix Device Pinout

Signal Name	U33 Pin Number	Pin J124A
S_TX1OUT1	14	2
S_RS232_CTS	9	N/A
S_RX1IN1	13	3
S_RS232_RTS	10	N/A
S_RS232_RXD	12	N/A
S_RS232_TXD	11	N/A
CAP1(0.1uF)	4	N/A
CAP1(0.1uF)	5	N/A
CAP2(0.1uF)	1	N/A
CAP2(0.1uF)	3	N/A
CAP3(0.1uF)	6	N/A
S_TX2OUT1	7	8
3.3V	16	N/A
S_RX2IN1	8	7
GND	15	N/A
CAP4(0.1uF)	2	N/A

Table 43. RS-232 Connector to Stratix GX Device Pinout (Part 1 of 2)

Signal Name	U28 Pin Number	Pin J124B
GX_TX1OUT1	14	11
GX_RS232_CTS	9	N/A
GX_RX1IN1	13	N/A
GX_RS232_RTS	10	N/A
GX_RS232_RXD	12	N/A
GX_RS232_TXD	11	N/A
CAP1(0.1uF)	4	N/A
CAP1(0.1uF)	5	N/A

Table 43. RS-232 Connector to Stratix GX Device Pinout (Part 2 of 2)

Signal Name	U28 Pin Number	Pin J124B
CAP2(0.1uF)	1	N/A
CAP2(0.1uF)	3	N/A
CAP3(0.1uF)	6	N/A
GX_TX2OUT1	7	17
3.3V	16	N/A
GX_RX2IN1	8	16
GND	15	N/A
CAP4(0.1uF)	2	N/A

ByteBlaster II Cable Connector Pinouts

Tables 44 and 45 shows the pinouts for the ByteBlaster II cable connectors on the Stratix GX Development Board

Table 44. ByteBlaster II Pinout for Serial Header

Signal Name	Pin Number
PS_DCLK	J85.1
GND	J85.10
GND	J85.2
VCC	J85.6
VCC	J85.4
PS_CDONE_n	J85.3
PS_CONFIG_n	J85.5
PS_STATUS_n	J85.7
PS_EPLD_D0	J85.9

Table 45. ByteBlaster II Pinout for JTAG Header (Part 1 of 2)

Signal Name	Pin Number
TCK	J87.1
GND	J87.2
3.3V	J87.4, J87.6
TDO	J87.3
TMS	J87.5
TDI	J87.9

Table 45. ByteBlaster II Pinout for JTAG Header (Part 2 of 2)

Signal Name	Pin Number
No Connect	J87.8, J87.7
GND	J87.10
VCC	J87.6

Flash Memory Pinouts

Table 46 shows the pinouts for the flash memory connector on the Stratix GX Development Board.

Table 46. Flash Memory Pinout (Part 1 of 2)

Signal Name	Pin Number (U31)	Stratix Pin Number (U15)
FLASH_A0	25	AD31
FLASH_A1	24	AD32
FLASH_A2	23	AC31
FLASH_A3	22	AB32
FLASH_A4	21	AB26
FLASH_A5	20	AA24
FLASH_A6	19	AG29
FLASH_A7	18	AG30
FLASH_A8	8	AG32
FLASH_A9	7	AG31
FLASH_A10	6	AF29
FLASH_A11	5	AF30
FLASH_A12	4	AF31
FLASH_A13	3	AF32
FLASH_A14	2	AE29
FLASH_A15	1	AE30
FLASH_A16	48	AE31
FLASH_A17	17	AE32
FLASH_A18	16	AD29
FLASH_A19	9	AD30
FLASH_RESETn	12	AA25
FLASH_BYTEn	47	Y24
FLASH_WPn	14	N/A
3.3V	37	N/A

Signal Name	Pin Number (U31)	Stratix Pin Number (U15)
FLASH_A20	10	AC30
FLASH_A21	13	AC29
FLASH_D0	29	AF25
FLASH_D1	31	AF26
FLASH_D2	33	AF28
FLASH_D3	35	AF27
FLASH_D4	38	AE26
FLASH_D5	40	AE25
FLASH_D6	42	AE27
FLASH_D7	44	AE28
FLASH_D8	30	AD25
FLASH_D9	32	AD26
FLASH_D10	34	AD27
FLASH_D11	36	AD28
FLASH_D12	39	AC28
FLASH_D13	41	AC27
FLASH_D14	43	AC26
FLASH_D15	45	AC25
FLASH_CEN	26	AA26
FLASH_OEN	28	AB27
FLASH_WEN	11	AA27
GND	27	N/A
GND	46	N/A
FLASH_RDY_BSYn	15	N/A

Compact Flash Connector Pinout

Table 47 shows the pinouts for the flash memory connector on the Stratix GX Development Board.

Signal Name	Pin Number (CON3)	U15 Stratix Pin Number
5V_CF	13	N/A
5V_CF	38	N/A

Table 47. Compact Flash Connector Pinout (Part 2 of 3)

Signal Name	Pin Number (CON3)	U15 Stratix Pin Number
GND	1	N/A
GND	25	N/A
GND	33	N/A
GND	39	N/A
GND	50	N/A
No connect	40	N/A
Q_CF_ATASEL_N	9	H11
Q_CF_CS_N	32	K12
Q_CF_PRESENT_N	26	J12
Q_CF_REG	44	K13
Q_CF_RESET_N	41	H12
Q_SCRUZ_IO[0]	6	A11
Q_SCRUZ_IO[10]	23	B9
Q_SCRUZ_IO[11]	29	D10
Q_SCRUZ_IO[12]	22	C10
Q_SCRUZ_IO[13]	30	A9
Q_SCRUZ_IO[14]	21	B11
Q_SCRUZ_IO[15]	31	C11
Q_SCRUZ_IO[17]	35	D11
Q_SCRUZ_IO[18]	34	B7
Q_SCRUZ_IO[19]	42	D8
Q_SCRUZ_IO[1]	47	B12
Q_SCRUZ_IO[22]	37	A8
Q_SCRUZ_IO[23]	24	C9
Q_SCRUZ_IO[24]	19	C8
Q_SCRUZ_IO[25]	20	D9
Q_SCRUZ_IO[26]	18	A7
Q_SCRUZ_IO[27]	7	D6
Q_SCRUZ_IO[28]	45	C6
Q_SCRUZ_IO[29]	8	B5
Q_SCRUZ_IO[2]	5	C12
Q_SCRUZ_IO[30]	46	C7
Q_SCRUZ_IO[31]	10	A5

Table 47. Compact Flash Connector Pinout (Part 3 of 3)

Signal Name	Pin Number (CON3)	U15 Stratix Pin Number
Q_SCRUZ_IO[32]	11	D7
Q_SCRUZ_IO[33]	12	A6
Q_SCRUZ_IO[34]	14	B6
Q_SCRUZ_IO[35]	15	E7
Q_SCRUZ_IO[36]	16	D5
Q_SCRUZ_IO[37]	17	C3
Q_SCRUZ_IO[38]	36	E5
Q_SCRUZ_IO[39]	43	C4
Q_SCRUZ_IO[3]	48	C13
Q_SCRUZ_IO[4]	4	D13
Q_SCRUZ_IO[5]	49	E13
Q_SCRUZ_IO[6]	3	A13
Q_SCRUZ_IO[7]	27	B13
Q_SCRUZ_IO[8]	2	D12
Q_SCRUZ_IO[9]	28	E11

DDR DIMM Memory Connector Pinout

Table 48 shows the pinouts for the DDR DIMM connector on the Stratix GX Development Board.

Table 48. DDR DIMM Pinout (Part 1 of 7)

Signal Name	Pin Number (XU1)	U7 Stratix GX Pin Number
DDR_CLK0_p	137	AL17
DDR_CLK0_n	138	AM17
DDR_CLK1_p	16	AJ17
DDR_CLK1_n	17	AK17
DDR_CLK2_p	76	AJ18
DDR_CLK2_n	75	AK18
DDR_CLK_EN0	21	U13
DDR_CLK_EN1	111	AA13
DDR_WE_N 11,39	63	W12
DDR_CAS_N 11,39	65	AA12
DDR_RAS_N 11,39	154	AF14

Table 48. DDR DIMM Pinout (Part 2 of 7)

Signal Name	Pin Number (XU1)	U7 Stratix GX Pin Number
DDR_CS0_N	157	V11
DDR_CS1_N	158	W11
DDR_BA0	59	W13
DDR_BA1	52	AE14
GND	181	N/A
GND	182	N/A
GND	183	N/A
DDR_A0	48	Y18
DDR_A1	43	AC19
DDR_A2	41	Y17
DDR_A3	130	V14
DDR_A4	37	AE19
DDR_A5	32	AE15
DDR_A6	125	AE18
DDR_A7	29	AF16
DDR_A8	122	W14
DDR_A9	27	Y14
DDR_A10	141	AD15
DDR_A11	118	AA14
DDR_A12	115	AB14
GND	90	N/A
GND	92	N/A
DDR_STROBE0	5	AM28
DDR_STROBE1	14	AJ25
DDR_STROBE2	25	AJ23
DDR_STROBE3	36	AL21
DDR_STROBE4	56	AL14
DDR_STROBE5	67	AH13
DDR_STROBE6	78	AE12
DDR_STROBE7	86	AD11
DDR_STROBE9	97	AL20
DDR_STROBE10	107	AK20
DDR_STROBE11	119	AJ20

Table 48. DDR DIMM Pinout (Part 3 of 7)

Signal Name	Pin Number (XU1)	U7 Stratix GX Pin Number
DDR_STROBE12	129	AH21
DDR_STROBE13	149	AC8
DDR_STROBE14	159	AF10
DDR_STROBE15	169	AF8
DDR_STROBE16	177	AF9
GND	91	
VREF	1	
N.C.	82	
N.C.	9	
N.C.	10	
N.C.	44	
N.C.	45	
N.C.	47	
N.C.	49	
N.C.	51	
N.C.	71	
N.C.	101	
N.C.	102	
N.C.	103	
N.C.	113	
N.C.	134	
N.C.	135	
N.C.	140	
N.C.	142	
N.C.	144	
N.C.	163	
N.C.	167	
N.C.	173	
VSS	3	
VSS	11	
VSS	18	
VSS	26	
VSS	34	

Table 48. DDR DIMM Pinout (Part 4 of 7)

Signal Name	Pin Number (XU1)	U7 Stratix GX Pin Number
VSS	42	
VSS	50	
VSS	58	
VSS	66	
VSS	74	
VSS	81	
VSS	89	
VSS	93	
VSS	100	
VSS	116	
VSS	124	
VSS	132	
VSS	139	
VSS	145	
VSS	152	
VSS	160	
VSS	176	
DDR_DATA0	2	AM27
DDR_DATA1	4	AL27
DDR_DATA2	6	AK27
DDR_DATA3	8	AL28
DDR_DATA4	94	AK28
DDR_DATA5	95	AM29
DDR_DATA6	98	AL29
DDR_DATA7	99	AK29
DDR_DATA8	12	AM25
DDR_DATA9	13	AL25
DDR_DATA10	19	AK25
DDR_DATA11	20	AM26
DDR_DATA12	105	AH25
DDR_DATA13	106	AL26
DDR_DATA14	109	AK26
DDR_DATA15	110	AJ26

Table 48. DDR DIMM Pinout (Part 5 of 7)

Signal Name	Pin Number (XU1)	U7 Stratix GX Pin Number
DDR_DATA16	23	AM23
DDR_DATA17	24	AL23
DDR_DATA18	28	AK23
DDR_DATA19	31	AH23
DDR_DATA20	114	AM24
DDR_DATA21	117	AL24
DDR_DATA22	121	AK24
DDR_DATA23	123	AJ24
DDR_DATA24	33	AK21
DDR_DATA25	35	AJ21
DDR_DATA26	39	AM21
DDR_DATA27	40	AM22
DDR_DATA28	126	AK22
DDR_DATA29	127	AJ22
DDR_DATA30	131	AL22
DDR_DATA31	133	AH22
DDR_DATA32	53	AK14
DDR_DATA33	55	AM15
DDR_DATA34	57	AM14
DDR_DATA35	60	AL15
DDR_DATA36	146	AK15
DDR_DATA37	147	AH15
DDR_DATA38	150	AJ15
DDR_DATA39	151	AG15
DDR_DATA40	61	AG13
DDR_DATA41	64	AK13
DDR_DATA42	68	AJ13
DDR_DATA43	69	AJ14
DDR_DATA44	153	AM13
DDR_DATA45	155	AL13
DDR_DATA46	161	AH14
DDR_DATA47	162	AG14
DDR_DATA48	72	AD12

Table 48. DDR DIMM Pinout (Part 6 of 7)

Signal Name	Pin Number (XU1)	U7 Stratix GX Pin Number
DDR_DATA49	73	AC12
DDR_DATA50	79	AF12
DDR_DATA51	80	AB13
DDR_DATA52	165	AF13
DDR_DATA53	166	AE13
DDR_DATA54	170	AC13
DDR_DATA55	171	AD13
DDR_DATA56	83	AD10
DDR_DATA57	84	AC10
DDR_DATA58	87	AE10
DDR_DATA59	88	AC11
DDR_DATA60	174	AE11
DDR_DATA61	175	AB12
DDR_DATA62	178	AB11
DDR_DATA63	179	AF11
VDD (2.5V)	7	
VDD (2.5V)	38	
VDD (2.5V)	46	
VDD (2.5V)	70	
VDD (2.5V)	85	
VDD (2.5V)	108	
VDD (2.5V)	120	
VDD (2.5V)	148	
VDD (2.5V)	168	
VDDQ (2.5V)	15	
VDDQ (2.5V)	22	
VDDQ (2.5V)	30	
VDDQ (2.5V)	54	
VDDQ (2.5V)	62	
VDDQ (2.5V)	77	
VDDQ (2.5V)	96	
VDDQ (2.5V)	104	
VDDQ (2.5V)	112	

Table 48. DDR DIMM Pinout (Part 7 of 7)

Signal Name	Pin Number (XU1)	U7 Stratix GX Pin Number
VDDQ (2.5V)	128	
VDDQ (2.5V)	136	
VDDQ (2.5V)	143	
VDDQ (2.5V)	156	
VDDQ (2.5V)	164	
VDDQ (2.5V)	172	
VDDQ (2.5V)	180	
GND	184	

Stratix GX Pinout

Table 49 shows the Stratix GX device pinouts both alphabetical by signal name and by pin number.

Table 49. Stratix GX Pinout (Part 1 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
1.25V_GX_SSTL_VREF	AA19	A2	GND_HSSI
1.25V_GX_SSTL_VREF	AA20	A3	GND_HSSI
1.25V_GX_SSTL_VREF	AA21	A4	XCVR_RX_P[7]
1.25V_GX_SSTL_VREF	AA22	A5	GND_HSSI
1.25V_GX_SSTL_VREF	Y12	A6	XCVR_RX_P[6]
1.25V_GX_SSTL_VREF	Y13	A7	GND_HSSI
1.25V_GX_SSTL_VREF	Y15	A8	SMA_INPUT3_TO_SGX_P
1.25V_GX_SSTL_VREF	Y16	A9	GND_HSSI
1.5V_GX_INT	AG10	A10	XCVR_RX_P[4]
1.5V_GX_INT	AG12	A11	GND_HSSI
1.5V_GX_INT	F9	A12	XCVR_RX_P[5]
1.5V_GX_INT	F11	A13	3.3V_GX_IO
1.5V_GX_INT	F13	A14	GX_MICTOR_OP_[15]
1.5V_GX_INT	P15	A15	GX_MICTOR_OP_[14]
1.5V_GX_INT	P17	A16	3.3V_GX_IO
1.5V_GX_INT	P19	A17	No connect

Table 49. Stratix GX Pinout (Part 2 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
1.5V_GX_INT	P20	A18	REFCLKB14N
1.5V_GX_INT	P21	A19	3.3V_GX_IO
1.5V_GX_INT	P22	A20	GND
1.5V_GX_INT	R15	A21	GX_HEADER[1]
1.5V_GX_INT	R16	A22	GX_HEADER[2]
1.5V_GX_INT	R18	A23	GX_HEADER[7]
1.5V_GX_INT	R20	A24	GX_HEADER[11]
1.5V_GX_INT	R21	A25	GX_HEADER[15]
1.5V_GX_INT	R22	A26	GX_HEADER[18]
1.5V_GX_INT	T9	A27	GX_DIG_1_E
1.5V_GX_INT	T15	A28	GX_DIG_2_A
1.5V_GX_INT	T17	A29	GX_DIG_2_DP
1.5V_GX_INT	T19	A30	3.3V_GX_IO
1.5V_GX_INT	T21	A31	GND
1.5V_GX_INT	U15	AA1	GND_HSSI
1.5V_GX_INT	U16	AA2	GND_HSSI
1.5V_GX_INT	U18	AA3	GND_HSSI
1.5V_GX_INT	U20	AA4	XCVR_TX_P[9]
1.5V_GX_INT	U21	AA5	XCVR_TX_N[9]
1.5V_GX_INT	V15	AA6	3.3V_XCVR_CLKS
1.5V_GX_INT	V17	AA7	1.5V_XCVR[4]
1.5V_GX_INT	V19	AA8	1.5V_XCVR[4]
1.5V_GX_INT	V21	AA9	1.5V_VCCP
1.5V_GX_INT	V22	AA10	No connect
1.5V_GX_INT	W15	AA11	No connect
1.5V_GX_INT	W16	AA12	DDR_CAS_N
1.5V_GX_INT	W18	AA13	DDR_CLK_EN[1]
1.5V_GX_INT	W20	AA14	DDR_A[11]
1.5V_GX_INT	W21	AA15	GX_VCCSEL
1.5V_GX_INT	W22	AA16	GND_PLL
1.5V_PLL	AC16	AA17	GND_PLL
1.5V_PLL	AC17	AA18	2.5V_GX_IO
1.5V_PLL	AC18	AA19	1.25V_GX_SSTL_VREF

Table 49. Stratix GX Pinout (Part 3 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
1.5V_PLL	AD17	AA20	1.25V_GX_SSTL_VREF
1.5V_PLL	AD26	AA21	1.25V_GX_SSTL_VREF
1.5V_PLL	AD27	AA22	1.25V_GX_SSTL_VREF
1.5V_PLL	J17	AA23	DIFF_RX_DRSTAT_P[0]
1.5V_PLL	J26	AA24	GND
1.5V_PLL	J27	AA25	BRIDGE_TX_P[8]
1.5V_PLL	K16	AA26	BRIDGE_TX_N[8]
1.5V_PLL	K17	AA27	BRIDGE_TXCLK_P
1.5V_PLL	L18	AA28	BRIDGE_TXCLK_N
1.5V_PLL	T25	AA29	DIFF_RX_P[11]
1.5V_PLL	T27	AA30	DIFF_RX_N[11]
1.5V_PLL	U25	AA31	DIFF_RX_P[15]
1.5V_PLL	U27	AA32	DIFF_RX_N[15]
1.5V_VCCG	AC6	AB1	XCVR_RX_P[9]
1.5V_VCCG	K6	AB2	XCVR_RX_N[9]
1.5V_VCCG	N6	AB3	GND_HSSI
1.5V_VCCG	T6	AB4	GND_HSSI
1.5V_VCCG	W6	AB5	GND_HSSI
1.5V_VCCP	AA9	AB6	GND
1.5V_VCCP	AB9	AB7	1.5V_XCVR[4]
1.5V_VCCP	M9	AB8	1.5V_XCVR[4]
1.5V_VCCP	N9	AB9	1.5V_VCCP
1.5V_VCCP	P9	AB10	No connect
1.5V_VCCP	R9	AB11	DDR_D[62]
1.5V_VCCP	U9	AB12	DDR_D[61]
1.5V_VCCP	V9	AB13	DDR_D[51]
1.5V_VCCP	W9	AB14	DDR_A[12]
1.5V_VCCP	Y9	AB15	NIO_PULLUP
1.5V_XCVR[1]	M7	AB16	GND_PLL
1.5V_XCVR[1]	M8	AB17	GND_PLL
1.5V_XCVR[1]	N7	AB18	2.5V_GX_IO
1.5V_XCVR[1]	N8	AB19	MSEL[2]
1.5V_XCVR[2]	P7	AB20	MSEL[1]

Table 49. Stratix GX Pinout (Part 4 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
1.5V_XCVR[2]	P8	AB21	No connect
1.5V_XCVR[2]	R7	AB22	XPAK_PRTAD[4]
1.5V_XCVR[2]	R8	AB23	DIFF_RX_DRSTAT_N[0]
1.5V_XCVR[3]	W7	AB24	BRIDGE_TX_P[6]
1.5V_XCVR[3]	W8	AB25	BRIDGE_TX_N[6]
1.5V_XCVR[3]	Y7	AB26	BRIDGE_TX_P[7]
1.5V_XCVR[3]	Y8	AB27	BRIDGE_TX_N[7]
1.5V_XCVR[4]	AA7	AB28	BRIDGE_TX_P[3]
1.5V_XCVR[4]	AA8	AB29	DIFF_RX_P[10]
1.5V_XCVR[4]	AB7	AB30	DIFF_RX_N[10]
1.5V_XCVR[4]	AB8	AB31	DIFF_RX_P[12]
1.5V_XCVR[5]	U7	AB32	DIFF_RX_N[12]
1.5V_XCVR[5]	U8	AC1	GND_HSSI
1.5V_XCVR[5]	V7	AC2	GND_HSSI
1.5V_XCVR[5]	V8	AC3	GND_HSSI
2.5V_GX_IO	AA18	AC4	XCVR_TX_P[8]
2.5V_GX_IO	AB18	AC5	XCVR_TX_N[8]
2.5V_GX_IO	AF7	AC6	1.5V_VCCG
2.5V_GX_IO	AM12	AC7	N20903449
2.5V_GX_IO	AM16	AC8	DDR_DS[13]
2.5V_GX_IO	AM19	AC9	DDR_DS[16]
2.5V_GX_IO	AM30	AC10	DDR_D[57]
2.5V_GX_IO	U11	AC11	DDR_D[59]
2.5V_GX_IO	Y19	AC12	DDR_D[49]
2.5V_GX_IO	Y21	AC13	DDR_D[54]
3.3V_GX_IO	A13	AC14	RDN[3]
3.3V_GX_IO	A16	AC15	PORSEL
3.3V_GX_IO	A19	AC16	1.5V_PLL
3.3V_GX_IO	A30	AC17	1.5V_PLL
3.3V_GX_IO	AK32	AC18	1.5V_PLL
3.3V_GX_IO	C32	AC19	DDR_A[1]
3.3V_GX_IO	G7	AC20	GX_PLL_ENA
3.3V_GX_IO	N19	AC21	No connect

Table 49. Stratix GX Pinout (Part 5 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
3.3V_GX_IO	N21	AC22	XPAK_VEND[2]
3.3V_GX_IO	N23	AC23	DIFF_RX_DRSTAT_P[1]
3.3V_GX_IO	R32	AC24	BRIDGE_TX_P[5]
3.3V_GX_IO	T11	AC25	BRIDGE_TX_N[5]
3.3V_GX_IO	T24	AC26	GND_PLL
3.3V_GX_IO	U23	AC27	GND_PLL
3.3V_GX_IO	V32	AC28	BRIDGE_TX_N[3]
3.3V_GX_IO	Y23	AC29	DIFF_RX_P[9]
3.3V_XCVR_CLKS	AA6	AC30	DIFF_RX_N[9]
3.3V_XCVR_CLKS	AD6	AC31	DIFF_RX_P[14]
3.3V_XCVR_CLKS	M6	AC32	DIFF_RX_N[14]
3.3V_XCVR_CLKS	R6	AD1	XCVR_RX_P[8]
3.3V_XCVR_CLKS	V6	AD10	DDR_D[56]
BRIDGE_RX_N[0]	N32	AD11	DDR_DS[7]
BRIDGE_RX_N[1]	P30	AD12	DDR_D[48]
BRIDGE_RX_N[10]	K30	AD13	DDR_D[55]
BRIDGE_RX_N[11]	H30	AD14	GX_PB_DEV_CLR_N
BRIDGE_RX_N[12]	G32	AD15	DDR_A[10]
BRIDGE_RX_N[13]	G30	AD16	CE_GX_N
BRIDGE_RX_N[14]	F32	AD17	1.5V_PLL
BRIDGE_RX_N[15]	E32	AD18	GX_PGM[0]
BRIDGE_RX_N[2]	M32	AD19	TP[8]
BRIDGE_RX_N[3]	K32	AD2	XCVR_RX_N[8]
BRIDGE_RX_N[4]	N30	AD20	MSEL[0]
BRIDGE_RX_N[5]	M30	AD21	RDN[4]
BRIDGE_RX_N[6]	L32	AD22	XPAK_VEND[3]
BRIDGE_RX_N[7]	L30	AD23	DIFF_RX_DRSTAT_N[1]
BRIDGE_RX_N[8]	J32	AD24	BRIDGE_TX_P[4]
BRIDGE_RX_N[9]	H32	AD25	BRIDGE_TX_N[4]
BRIDGE_RX_P[0]	N31	AD26	1.5V_PLL
BRIDGE_RX_P[1]	P29	AD27	1.5V_PLL
BRIDGE_RX_P[10]	K29	AD28	BRIDGE_TX_P[0]
BRIDGE_RX_P[11]	H29	AD29	DIFF_RX_P[5]

Table 49. Stratix GX Pinout (Part 6 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
BRIDGE_RX_P[12]	G31	AD3	GND_HSSI
BRIDGE_RX_P[13]	G29	AD30	DIFF_RX_N[5]
BRIDGE_RX_P[14]	F31	AD31	DIFF_RX_P[8]
BRIDGE_RX_P[15]	E31	AD32	DIFF_RX_N[8]
BRIDGE_RX_P[2]	M31	AD4	GND_HSSI
BRIDGE_RX_P[3]	K31	AD5	GND_HSSI
BRIDGE_RX_P[4]	N29	AD6	3.3V_XCVR_CLKS
BRIDGE_RX_P[5]	M29	AD7	No connect
BRIDGE_RX_P[6]	L31	AD8	No connect
BRIDGE_RX_P[7]	L29	AD9	No connect
BRIDGE_RX_P[8]	J31	AE1	GND_HSSI
BRIDGE_RX_P[9]	H31	AE2	GND_HSSI
BRIDGE_RXCLK_N	T32	AE3	GND_HSSI
BRIDGE_RXCLK_P	T31	AE4	XCVR_TX_P[10]
BRIDGE_TX_N[0]	AE28	AE5	XCVR_TX_N[10]
BRIDGE_TX_N[1]	AE27	AE6	GND_HSSI
BRIDGE_TX_N[10]	Y26	AE7	GND
BRIDGE_TX_N[11]	W26	AE8	No connect
BRIDGE_TX_N[12]	W28	AE9	No connect
BRIDGE_TX_N[13]	W24	AE10	DDR_D[58]
BRIDGE_TX_N[14]	V26	AE11	DDR_D[60]
BRIDGE_TX_N[15]	V28	AE12	DDR_DS[6]
BRIDGE_TX_N[2]	AE25	AE13	DDR_D[53]
BRIDGE_TX_N[3]	AC28	AE14	DDR_BA[1]
BRIDGE_TX_N[4]	AD25	AE15	DDR_A[5]
BRIDGE_TX_N[5]	AC25	AE16	No connect
BRIDGE_TX_N[6]	AB25	AE17	No connect
BRIDGE_TX_N[7]	AB27	AE18	DDR_A[6]
BRIDGE_TX_N[8]	AA26	AE19	DDR_A[4]
BRIDGE_TX_N[9]	Y28	AE20	No connect
BRIDGE_TX_P[0]	AD28	AE21	XPAK_MOD_DET
BRIDGE_TX_P[1]	AE26	AE22	GND_PLL
BRIDGE_TX_P[10]	Y25	AE23	XPAK_X_RST

Table 49. Stratix GX Pinout (Part 7 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
BRIDGE_TX_P[11]	W25	AE24	BRIDGE_TX_P[2]
BRIDGE_TX_P[12]	W27	AE25	BRIDGE_TX_N[2]
BRIDGE_TX_P[13]	V24	AE26	BRIDGE_TX_P[1]
BRIDGE_TX_P[14]	V25	AE27	BRIDGE_TX_N[1]
BRIDGE_TX_P[15]	V27	AE28	BRIDGE_TX_N[0]
BRIDGE_TX_P[2]	AE24	AE29	DIFF_RX_P[6]
BRIDGE_TX_P[3]	AB28	AE30	DIFF_RX_N[6]
BRIDGE_TX_P[4]	AD24	AE31	DIFF_RX_P[7]
BRIDGE_TX_P[5]	AC24	AE32	DIFF_RX_N[7]
BRIDGE_TX_P[6]	AB24	AF1	XTAL2_SGX_P
BRIDGE_TX_P[7]	AB26	AF2	XTAL2_SGX_N
BRIDGE_TX_P[8]	AA25	AF3	GND_HSSI
BRIDGE_TX_P[9]	Y27	AF4	GND_HSSI
BRIDGE_TXCLK_N	AA28	AF5	GND_HSSI
BRIDGE_TXCLK_P	AA27	AF6	GND
CE_GX_N	AD16	AF7	2.5V_GX_IO
DDR_A[0]	Y18	AF8	DDR_DS[15]
DDR_A[1]	AC19	AF9	No connect
DDR_A[10]	AD15	AF10	DDR_DS[14]
DDR_A[11]	AA14	AF11	DDR_D[63]
DDR_A[12]	AB14	AF12	DDR_D[50]
DDR_A[2]	Y17	AF13	DDR_D[52]
DDR_A[3]	V14	AF14	DDR_RAS_N
DDR_A[4]	AE19	AF15	GND_PLL
DDR_A[5]	AE15	AF16	DDR_A[7]
DDR_A[6]	AE18	AF17	GX_PGM[1]
DDR_A[7]	AF16	AF18	GX_RUNLU
DDR_A[8]	W14	AF19	RUP[3]
DDR_A[9]	Y14	AF20	RUP[4]
DDR_BA[0]	W13	AF21	GX_PGM[2]
DDR_BA[1]	AE14	AF22	GND_PLL
DDR_CAS_N	AA12	AF23	XPAK_TX_ON
DDR_CLK_EN[0]	U13	AF24	XPAK_VEND[1]

Table 49. Stratix GX Pinout (Part 8 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
DDR_CLK_EN[1]	AA13	AF25	DPA_TX_P[1]
DDR_CLK_FB	AG18	AF26	DPA_TX_N[1]
DDR_CLK_FB	AK19	AF27	DPACLK_OUT_P
DDR_CLK0_N	AM17	AF28	DPACLK_OUT_N
DDR_CLK0_P	AL17	AF29	DIFF_RX_P[4]
DDR_CLK1_N	AK17	AF30	DIFF_RX_N[4]
DDR_CLK1_P	AJ17	AF31	DIFF_RX_P[3]
DDR_CLK2_N	AK18	AF32	DIFF_RX_N[3]
DDR_CLK2_P	AJ18	AG1	GND_HSSI
DDR_CS0_N	V11	AG2	GND_HSSI
DDR_CS1_N	W11	AG3	GND_HSSI
DDR_D[0]	AM27	AG4	XCVR_TX_P[11]
DDR_D[1]	AL27	AG5	XCVR_TX_N[11]
DDR_D[10]	AK25	AG6	GND
DDR_D[11]	AM26	AG7	GND
DDR_D[12]	AH25	AG8	GND
DDR_D[13]	AL26	AG9	GND
DDR_D[14]	AK26	AG10	1.5V_GX_INT
DDR_D[15]	AJ26	AG11	GND
DDR_D[16]	AM23	AG12	1.5V_GX_INT
DDR_D[17]	AL23	AG13	DDR_D[40]
DDR_D[18]	AK23	AG14	DDR_D[47]
DDR_D[19]	AH23	AG15	DDR_D[39]
DDR_D[2]	AK27	AG16	SMA_INPUT1_TO_SGX_P
DDR_D[20]	AM24	AG17	GND_PLL
DDR_D[21]	AL24	AG18	DDR_CLK_FB
DDR_D[22]	AK24	AG19	No connect
DDR_D[23]	AJ24	AG20	No connect
DDR_D[24]	AK21	AG21	No connect
DDR_D[25]	AJ21	AG22	No connect
DDR_D[26]	AM21	AG23	TP[17]
DDR_D[27]	AM22	AG24	TP[13]
DDR_D[28]	AK22	AG25	No connect

Table 49. Stratix GX Pinout (Part 9 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
DDR_D[29]	AJ22	AG26	No connect
DDR_D[3]	AL28	AG27	DPA_TX_P[0]
DDR_D[30]	AL22	AG28	DPA_TX_N[0]
DDR_D[31]	AH22	AG29	DIFF_RX_P[1]
DDR_D[32]	AK14	AG30	DIFF_RX_N[1]
DDR_D[33]	AM15	AG31	DIFF_RX_P[2]
DDR_D[34]	AM14	AG32	DIFF_RX_N[2]
DDR_D[35]	AL15	AH1	XCVR_RX_P[10]
DDR_D[36]	AK15	AH2	XCVR_RX_N[10]
DDR_D[37]	AH15	AH3	GND_HSSI
DDR_D[38]	AJ15	AH4	GND_HSSI
DDR_D[39]	AG15	AH5	GND_HSSI
DDR_D[4]	AK28	AH6	GND_HSSI
DDR_D[40]	AG13	AH7	XCVR_TX_N[12]
DDR_D[41]	AK13	AH8	GND_HSSI
DDR_D[42]	AJ13	AH9	XCVR_TX_N[14]
DDR_D[43]	AJ14	AH10	GND_HSSI
DDR_D[44]	AM13	AH11	XCVR_TX_N[15]
DDR_D[45]	AL13	AH12	GND
DDR_D[46]	AH14	AH13	DDR_DS[5]
DDR_D[47]	AG14	AH14	DDR_D[46]
DDR_D[48]	AD12	AH15	DDR_D[37]
DDR_D[49]	AC12	AH16	SMA_INPUT1_TO_SGX_N
DDR_D[5]	AM29	AH17	GND_PLL
DDR_D[50]	AF12	AH18	No connect
DDR_D[51]	AB13	AH19	No connect
DDR_D[52]	AF13	AH20	No connect
DDR_D[53]	AE13	AH21	DDR_DS[12]
DDR_D[54]	AC13	AH22	DDR_D[31]
DDR_D[55]	AD13	AH23	DDR_D[19]
DDR_D[56]	AD10	AH24	No connect
DDR_D[57]	AC10	AH25	DDR_D[12]
DDR_D[58]	AE10	AH26	XPAK_LASI

Table 49. Stratix GX Pinout (Part 10 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
DDR_D[59]	AC11	AH27	No connect
DDR_D[6]	AL29	AH28	No connect
DDR_D[60]	AE11	AH29	No connect
DDR_D[61]	AB12	AH30	No connect
DDR_D[62]	AB11	AH31	DIFF_RX_P[0]
DDR_D[63]	AF11	AH32	DIFF_RX_N[0]
DDR_D[7]	AK29	AJ1	GND_HSSI
DDR_D[8]	AM25	AJ2	GND_HSSI
DDR_D[9]	AL25	AJ3	GND_HSSI
DDR_DS[0]	AM28	AJ4	XCVR_TX_P[13]
DDR_DS[1]	AJ25	AJ5	XCVR_TX_N[13]
DDR_DS[10]	AK20	AJ6	GND_HSSI
DDR_DS[11]	AJ20	AJ7	XCVR_TX_P[12]
DDR_DS[12]	AH21	AJ8	GND_HSSI
DDR_DS[13]	AC8	AJ9	XCVR_TX_P[14]
DDR_DS[14]	AF10	AJ10	GND_HSSI
DDR_DS[15]	AF8	AJ11	XCVR_TX_P[15]
DDR_DS[16]	AC9	AJ12	GND
DDR_DS[2]	AJ23	AJ13	DDR_D[42]
DDR_DS[3]	AL21	AJ14	DDR_D[43]
DDR_DS[4]	AL14	AJ15	DDR_D[38]
DDR_DS[5]	AH13	AJ16	GND_PLL
DDR_DS[6]	AE12	AJ17	DDR_CLK1_P
DDR_DS[7]	AD11	AJ18	DDR_CLK2_P
DDR_DS[9]	AL20	AJ19	No connect
DDR_RAS_N	AF14	AJ20	DDR_DS[11]
DDR_WE_N	W12	AJ21	DDR_D[25]
DIFF_RX_DRCLK_N	U24	AJ22	DDR_D[29]
DIFF_RX_DRCLK_P	T23	AJ23	DDR_DS[2]
DIFF_RX_DRSTAT_N[0]	AB23	AJ24	DDR_D[23]
DIFF_RX_DRSTAT_N[1]	AD23	AJ25	DDR_DS[1]
DIFF_RX_DRSTAT_P[0]	AA23	AJ26	DDR_D[15]
DIFF_RX_DRSTAT_P[1]	AC23	AJ27	TP[11]

Table 49. Stratix GX Pinout (Part 11 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
DIFF_RX_N[0]	AH32	AJ28	XPAK_VEND[0]
DIFF_RX_N[1]	AG30	AJ29	No connect
DIFF_RX_N[10]	AB30	AJ30	No connect
DIFF_RX_N[11]	AA30	AJ31	No connect
DIFF_RX_N[12]	AB32	AJ32	No connect
DIFF_RX_N[13]	Y30	AK1	XCVR_RX_P[11]
DIFF_RX_N[14]	AC32	AK2	XCVR_RX_N[11]
DIFF_RX_N[15]	AA32	AK3	GND_HSSI
DIFF_RX_N[2]	AG32	AK4	GND_HSSI
DIFF_RX_N[3]	AF32	AK5	GND_HSSI
DIFF_RX_N[4]	AF30	AK6	GND_HSSI
DIFF_RX_N[5]	AD30	AK7	GND_HSSI
DIFF_RX_N[6]	AE30	AK8	GND_HSSI
DIFF_RX_N[7]	AE32	AK9	GND_HSSI
DIFF_RX_N[8]	AD32	AK10	GND_HSSI
DIFF_RX_N[9]	AC30	AK11	GND_HSSI
DIFF_RX_P[0]	AH31	AK12	GND
DIFF_RX_P[1]	AG29	AK13	DDR_D[41]
DIFF_RX_P[10]	AB29	AK14	DDR_D[32]
DIFF_RX_P[11]	AA29	AK15	DDR_D[36]
DIFF_RX_P[12]	AB31	AK16	GND_PLL
DIFF_RX_P[13]	Y29	AK17	DDR_CLK1_N
DIFF_RX_P[14]	AC31	AK18	DDR_CLK2_N
DIFF_RX_P[15]	AA31	AK19	DDR_CLK_FB
DIFF_RX_P[2]	AG31	AK20	DDR_DS[10]
DIFF_RX_P[3]	AF31	AK21	DDR_D[24]
DIFF_RX_P[4]	AF29	AK22	DDR_D[28]
DIFF_RX_P[5]	AD29	AK23	DDR_D[18]
DIFF_RX_P[6]	AE29	AK24	DDR_D[22]
DIFF_RX_P[7]	AE31	AK25	DDR_D[10]
DIFF_RX_P[8]	AD31	AK26	DDR_D[14]
DIFF_RX_P[9]	AC29	AK27	DDR_D[2]
DIFF_RX_RCTL_N	W30	AK28	DDR_D[4]

Table 49. Stratix GX Pinout (Part 12 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
DIFF_RX_RCTL_P	W29	AK29	DDR_D[7]
DIFF_RX_RDCLK_N	U32	AK30	XPAK_PRTAD[1]
DIFF_RX_RDCLK_P	U31	AK31	XPAK_PRTAD[0]
DIFF_RX_RSCLK	F19	AK32	3.3V_GX_IO
DIFF_RX_RSTAT[0]	E21	AL1	GND_HSSI
DIFF_RX_RSTAT[1]	C21	AL2	GND_HSSI
DIFF_TX_DTSCLK_N	U30	AL3	GND_HSSI
DIFF_TX_DTSCLK_P	U29	AL4	GND_HSSI
DIFF_TX_DTSTAT_N[0]	D32	AL5	XCVR_RX_N[12]
DIFF_TX_DTSTAT_N[1]	D30	AL6	GND_HSSI
DIFF_TX_DTSTAT_P[0]	D31	AL7	XTAL1_SGX_N
DIFF_TX_DTSTAT_P[1]	D29	AL8	GND_HSSI
DIFF_TX_N[0]	R26	AL9	XCVR_RX_N[14]
DIFF_TX_N[1]	R28	AL10	GND_HSSI
DIFF_TX_N[10]	K25	AL11	XCVR_RX_N[15]
DIFF_TX_N[11]	J25	AL12	GND
DIFF_TX_N[12]	K28	AL13	DDR_D[45]
DIFF_TX_N[13]	H25	AL14	DDR_DS[4]
DIFF_TX_N[14]	H27	AL15	DDR_D[35]
DIFF_TX_N[15]	H28	AL16	GND
DIFF_TX_N[2]	P28	AL17	DDR_CLK0_P
DIFF_TX_N[3]	R24	AL18	XTAL3_OUT_SGX
DIFF_TX_N[4]	P26	AL19	GND_PLL
DIFF_TX_N[5]	N28	AL20	DDR_DS[9]
DIFF_TX_N[6]	N26	AL21	DDR_DS[3]
DIFF_TX_N[7]	M28	AL22	DDR_D[30]
DIFF_TX_N[8]	L27	AL23	DDR_D[17]
DIFF_TX_N[9]	L25	AL24	DDR_D[21]
DIFF_TX_P[0]	R25	AL25	DDR_D[9]
DIFF_TX_P[1]	R27	AL26	DDR_D[13]
DIFF_TX_P[10]	K24	AL27	DDR_D[1]
DIFF_TX_P[11]	J24	AL28	DDR_D[3]
DIFF_TX_P[12]	L28	AL29	DDR_D[6]

Table 49. Stratix GX Pinout (Part 13 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
DIFF_TX_P[13]	H24	AL30	XPAK_PRTAD[3]
DIFF_TX_P[14]	H26	AL31	XPAK_PRTAD[2]
DIFF_TX_P[15]	J28	AL32	GND
DIFF_TX_P[2]	P27	AM2	XCVR_RX_P[13]
DIFF_TX_P[3]	P24	AM3	XCVR_RX_N[13]
DIFF_TX_P[4]	P25	AM4	GND_HSSI
DIFF_TX_P[5]	N27	AM5	XCVR_RX_P[12]
DIFF_TX_P[6]	N25	AM6	GND_HSSI
DIFF_TX_P[7]	M27	AM7	XTAL1_SGX_P
DIFF_TX_P[8]	L26	AM8	GND_HSSI
DIFF_TX_P[9]	L24	AM9	XCVR_RX_P[14]
DIFF_TX_TCTL_N	G26	AM10	GND_HSSI
DIFF_TX_TCTL_P	G25	AM11	XCVR_RX_P[15]
DIFF_TX_TDCLK_N	M26	AM12	2.5V_GX_IO
DIFF_TX_TDCLK_P	M25	AM13	DDR_D[44]
DIFF_TX_TSCLK	E19	AM14	DDR_D[34]
DIFF_TX_TSTAT[0]	D27	AM15	DDR_D[33]
DIFF_TX_TSTAT[1]	C31	AM16	2.5V_GX_IO
DPA_RX_N[0]	R30	AM17	DDR_CLK0_N
DPA_RX_N[1]	R31	AM18	XTAL3_OUT_SGX_N
DPA_RX_P[0]	R29	AM19	2.5V_GX_IO
DPA_RX_P[1]	P31	AM20	GND
DPA_TX_N[0]	AG28	AM21	DDR_D[26]
DPA_TX_N[1]	AF26	AM22	DDR_D[27]
DPA_TX_P[0]	AG27	AM23	DDR_D[16]
DPA_TX_P[1]	AF25	AM24	DDR_D[20]
DPACLK_IN_N	T30	AM25	DDR_D[8]
DPACLK_IN_P	T29	AM26	DDR_D[11]
DPACLK_OUT_N	AF28	AM27	DDR_D[0]
DPACLK_OUT_P	AF27	AM28	DDR_DS[0]
GND	A20	AM29	DDR_D[5]
GND	A31	AM30	2.5V_GX_IO
GND	AA24	AM31	GND

Table 49. Stratix GX Pinout (Part 14 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND	AB6	B1	XCVR_RX_P[1]
GND	AE7	B2	XCVR_RX_N[1]
GND	AF6	B3	GND_HSSI
GND	AG6	B4	XCVR_RX_N[7]
GND	AG7	B5	GND_HSSI
GND	AG8	B6	XCVR_RX_N[6]
GND	AG9	B7	GND_HSSI
GND	AG11	B8	SMA_INPUT3_TO_SGX_N
GND	AH12	B9	GND_HSSI
GND	AJ12	B10	XCVR_RX_N[4]
GND	AK12	B11	GND_HSSI
GND	AL12	B12	XCVR_RX_N[5]
GND	AL16	B13	GND
GND	AL32	B14	GX_DIP[7]
GND	AM20	B15	No connect
GND	AM31	B16	GND
GND	B13	B17	No connect
GND	B16	B18	REFCLKB14P
GND	B32	B19	REFCLKB15N
GND	C13	B20	No connect
GND	D13	B21	GX_DIG_2_D
GND	E13	B22	GX_HEADER[5]
GND	F7	B23	GX_HEADER[8]
GND	F8	B24	GX_HEADER[12]
GND	F10	B25	GX_HEADER[16]
GND	F12	B26	GX_DIG_1_DP
GND	K22	B27	GX_DIG_1_D
GND	L6	B28	GX_DIG_1_B
GND	M19	B29	GX_DIG_2_G
GND	M20	B30	GX_LED[3]
GND	M21	B31	TP[12]
GND	M22	B32	GND
GND	M24	C1	GND_HSSI

Table 49. Stratix GX Pinout (Part 15 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND	N12	C2	GND_HSSI
GND	N13	C3	GND_HSSI
GND	N15	C4	GND_HSSI
GND	N16	C5	GND_HSSI
GND	N20	C6	GND_HSSI
GND	N22	C7	GND_HSSI
GND	N24	C8	GND_HSSI
GND	P6	C9	GND_HSSI
GND	P16	C10	GND_HSSI
GND	P18	C11	GND_HSSI
GND	P23	C12	GND_HSSI
GND	P32	C13	GND
GND	R17	C14	GX_MICTOR_OP_[13]
GND	R19	C15	GX_RECOV_CLK[4]
GND	R23	C16	GND_PLL
GND	T10	C17	No connect
GND	T16	C18	No connect
GND	T18	C19	REFCLKB15P
GND	T20	C20	No connect
GND	T22	C21	DIFF_RX_RSTAT[1]
GND	U6	C22	GX_HEADER[3]
GND	U10	C23	GX_HEADER[9]
GND	U17	C24	GX_HEADER[13]
GND	U19	C25	GX_HEADER[17]
GND	U22	C26	GX_DIG_1_G
GND	V16	C27	GX_DIG_1_C
GND	V18	C28	GX_DIG_1_A
GND	V20	C29	GX_DIG_2_F
GND	V23	C30	GX_LED[4]
GND	W17	C31	DIFF_TX_TSTAT[1]
GND	W19	C32	3.3V_GX_IO
GND	W23	D1	XCVR_RX_P[0]
GND	W32	D2	XCVR_RX_N[0]

Table 49. Stratix GX Pinout (Part 16 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND	Y6	D3	GND_HSSI
GND	Y20	D4	XCVR_TX_P[1]
GND	Y22	D5	GND_HSSI
GND	Y24	D6	XCVR_TX_P[7]
GND_HSSI	A2	D7	GND_HSSI
GND_HSSI	A3	D8	XCVR_TX_P[6]
GND_HSSI	A5	D9	GND_HSSI
GND_HSSI	A7	D10	XCVR_TX_P[4]
GND_HSSI	A9	D11	GND_HSSI
GND_HSSI	A11	D12	XCVR_TX_P[5]
GND_HSSI	AA1	D13	GND
GND_HSSI	AA2	D14	GX_MICTOR_OP_[6]
GND_HSSI	AA3	D15	GX_DIP[1]
GND_HSSI	AB3	D16	GND_PLL
GND_HSSI	AB4	D17	No connect
GND_HSSI	AB5	D18	No connect
GND_HSSI	AC1	D19	No connect
GND_HSSI	AC2	D20	No connect
GND_HSSI	AC3	D21	GX_HEADER[0]
GND_HSSI	AD3	D22	GX_HEADER[4]
GND_HSSI	AD4	D23	GX_DIG_2_C
GND_HSSI	AD5	D24	GX_HEADER[14]
GND_HSSI	AE1	D25	GX_DIG_2_B
GND_HSSI	AE2	D26	GX_DIG_1_F
GND_HSSI	AE3	D27	DIFF_TX_TSTAT[0]
GND_HSSI	AE6	D28	GX_PB[1]
GND_HSSI	AF3	D29	DIFF_TX_DTSTAT_P[1]
GND_HSSI	AF4	D30	DIFF_TX_DTSTAT_N[1]
GND_HSSI	AF5	D31	DIFF_TX_DTSTAT_P[0]
GND_HSSI	AG1	D32	DIFF_TX_DTSTAT_N[0]
GND_HSSI	AG2	E1	GND_HSSI
GND_HSSI	AG3	E2	GND_HSSI
GND_HSSI	AH3	E3	GND_HSSI

Table 49. Stratix GX Pinout (Part 17 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND_HSSI	AH4	E4	XCVR_TX_N[1]
GND_HSSI	AH5	E5	GND_HSSI
GND_HSSI	AH6	E6	XCVR_TX_N[7]
GND_HSSI	AH8	E7	GND_HSSI
GND_HSSI	AH10	E8	XCVR_TX_N[6]
GND_HSSI	AJ1	E9	GND_HSSI
GND_HSSI	AJ2	E10	XCVR_TX_N[4]
GND_HSSI	AJ3	E11	GND_HSSI
GND_HSSI	AJ6	E12	XCVR_TX_N[5]
GND_HSSI	AJ8	E13	GND
GND_HSSI	AJ10	E14	GX_MICTOR_OP_[8]
GND_HSSI	AK3	E15	GX_DIP[2]
GND_HSSI	AK4	E16	GND_PLL
GND_HSSI	AK5	E17	GND_PLL
GND_HSSI	AK6	E18	No connect
GND_HSSI	AK7	E19	DIFF_TX_TSCLK
GND_HSSI	AK8	E20	No connect
GND_HSSI	AK9	E21	DIFF_RX_RSTAT[0]
GND_HSSI	AK10	E22	GX_HEADER[6]
GND_HSSI	AK11	E23	GX_HEADER[10]
GND_HSSI	AL1	E24	No connect
GND_HSSI	AL2	E25	GX_HEADER[19]
GND_HSSI	AL3	E26	GX_PB[2]
GND_HSSI	AL4	E27	GX_LED[1]
GND_HSSI	AL6	E28	GX_LED[5]
GND_HSSI	AL8	E29	No connect
GND_HSSI	AL10	E30	No connect
GND_HSSI	AM4	E31	BRIDGE_RX_P[15]
GND_HSSI	AM6	E32	BRIDGE_RX_N[15]
GND_HSSI	AM8	F1	SMA_INPUT2_TO_SGX_P
GND_HSSI	AM10	F2	SMA_INPUT2_TO_SGX_N
GND_HSSI	B3	F3	GND_HSSI
GND_HSSI	B5	F4	GND_HSSI

Table 49. Stratix GX Pinout (Part 18 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND_HSSI	B7	F5	GND_HSSI
GND_HSSI	B9	F6	GND_HSSI
GND_HSSI	B11	F7	GND
GND_HSSI	C1	F8	GND
GND_HSSI	C2	F9	1.5V_GX_INT
GND_HSSI	C3	F10	GND
GND_HSSI	C4	F11	1.5V_GX_INT
GND_HSSI	C5	F12	GND
GND_HSSI	C6	F13	1.5V_GX_INT
GND_HSSI	C7	F14	GX_MICTOR_OP_[7]
GND_HSSI	C8	F15	GX_DIP[0]
GND_HSSI	C9	F16	GND_PLL
GND_HSSI	C10	F17	GND_PLL
GND_HSSI	C11	F18	No connect
GND_HSSI	C12	F19	DIFF_RX_RSCLK
GND_HSSI	D3	F20	GX_DIG_2_E
GND_HSSI	D5	F21	GX_DATA[7]
GND_HSSI	D7	F22	No connect
GND_HSSI	D9	F23	TP[10]
GND_HSSI	D11	F24	No connect
GND_HSSI	E1	F25	GX_RS232_RXD
GND_HSSI	E2	F26	GX_LED[2]
GND_HSSI	E3	F27	No connect
GND_HSSI	E5	F28	No connect
GND_HSSI	E7	F29	No connect
GND_HSSI	E9	F30	No connect
GND_HSSI	E11	F31	BRIDGE_RX_P[14]
GND_HSSI	F3	F32	BRIDGE_RX_N[14]
GND_HSSI	F4	G1	GND_HSSI
GND_HSSI	F5	G2	GND_HSSI
GND_HSSI	F6	G3	GND_HSSI
GND_HSSI	G1	G4	XCVR_TX_P[0]
GND_HSSI	G2	G5	XCVR_TX_N[0]

Table 49. Stratix GX Pinout (Part 19 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND_HSSI	G3	G6	GND_HSSI
GND_HSSI	G6	G7	3.3V_GX_IO
GND_HSSI	H3	G8	GX_DIP[3]
GND_HSSI	H4	G9	GX_MICTOR_EP_[4]
GND_HSSI	H5	G10	GX_MICTOR_EP_[9]
GND_HSSI	H6	G11	GX_MICTOR_EP_[14]
GND_HSSI	J1	G12	GX_MICTOR_OP_CLK
GND_HSSI	J2	G13	GX_MICTOR_OP_[5]
GND_HSSI	J3	G14	GX_DIP[6]
GND_HSSI	J6	G15	GX_MICTOR_OP_[11]
GND_HSSI	K3	G16	TMS
GND_HSSI	K4	G17	SFP2_TX_FAULT[6]
GND_HSSI	K5	G18	SFP3_MOD_DEF7_[0]
GND_HSSI	L1	G19	No connect
GND_HSSI	L2	G20	GX_DATA[4]
GND_HSSI	L3	G21	GX_RS232_RTS
GND_HSSI	M3	G22	GND_PLL
GND_HSSI	M4	G23	GX_PB[0]
GND_HSSI	M5	G24	GX_PB[3]
GND_HSSI	N1	G25	DIFF_TX_TCTL_P
GND_HSSI	N2	G26	DIFF_TX_TCTL_N
GND_HSSI	N3	G27	No connect
GND_HSSI	P3	G28	No connect
GND_HSSI	P4	G29	BRIDGE_RX_P[13]
GND_HSSI	P5	G30	BRIDGE_RX_N[13]
GND_HSSI	R1	G31	BRIDGE_RX_P[12]
GND_HSSI	R2	G32	BRIDGE_RX_N[12]
GND_HSSI	R3	H1	XCVR_RX_P[2]
GND_HSSI	T3	H2	XCVR_RX_N[2]
GND_HSSI	T4	H3	GND_HSSI
GND_HSSI	T5	H4	GND_HSSI
GND_HSSI	U1	H5	GND_HSSI
GND_HSSI	U2	H6	GND_HSSI

Table 49. Stratix GX Pinout (Part 20 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND_HSSI	U3	H7	SFP0_MOD_DEF4_[2]
GND_HSSI	V3	H8	GX_MICTOR_EP_[5]
GND_HSSI	V4	H9	GX_MICTOR_EP_CLK
GND_HSSI	V5	H10	GX_DIP[4]
GND_HSSI	W1	H11	GX_MICTOR_EP_[11]
GND_HSSI	W2	H12	GX_DIP[5]
GND_HSSI	W3	H13	GX_MICTOR_OP_[1]
GND_HSSI	Y3	H14	GX_MICTOR_OP_[9]
GND_HSSI	Y4	H15	GX_MICTOR_OP_[12]
GND_HSSI	Y5	H16	GX_TDI[2]
GND_PLL	AA16	H17	GX_DATA[0]
GND_PLL	AA17	H18	GX_DATA[1]
GND_PLL	AB16	H19	RUP_[4]
GND_PLL	AB17	H20	GX_DATA[5]
GND_PLL	AC26	H21	GX_RS232_TXD
GND_PLL	AC27	H22	GND_PLL
GND_PLL	AE22	H23	GX_RS232_CTS
GND_PLL	AF15	H24	DIFF_TX_P[13]
GND_PLL	AF22	H25	DIFF_TX_N[13]
GND_PLL	AG17	H26	DIFF_TX_P[14]
GND_PLL	AH17	H27	DIFF_TX_N[14]
GND_PLL	AJ16	H28	DIFF_TX_N[15]
GND_PLL	AK16	H29	BRIDGE_RX_P[11]
GND_PLL	AL19	H30	BRIDGE_RX_N[11]
GND_PLL	C16	H31	BRIDGE_RX_P[9]
GND_PLL	D16	H32	BRIDGE_RX_N[9]
GND_PLL	E16	J1	GND_HSSI
GND_PLL	E17	J2	GND_HSSI
GND_PLL	F16	J3	GND_HSSI
GND_PLL	F17	J4	XCVR_TX_P[2]
GND_PLL	G22	J5	XCVR_TX_N[2]
GND_PLL	H22	J6	GND_HSSI
GND_PLL	K26	J7	N20903841

Table 49. Stratix GX Pinout (Part 21 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GND_PLL	K27	J8	GX_MICTOR_EP_[0]
GND_PLL	L16	J9	GX_MICTOR_EP_[2]
GND_PLL	L17	J10	GX_MICTOR_EP_[7]
GND_PLL	M13	J11	GX_MICTOR_EP_[12]
GND_PLL	M16	J12	GX_MICTOR_EP_[15]
GND_PLL	M17	J13	GX_MICTOR_OP_[2]
GND_PLL	T14	J14	GX_MICTOR_OP_[10]
GND_PLL	T26	J15	TRSTN
GND_PLL	T28	J16	GX_TDO2_SW
GND_PLL	U14	J17	1.5V_PLL
GND_PLL	U26	J18	SFP3_MOD_DEF7_[1]
GND_PLL	U28	J19	GX_DATA[3]
GX_CDONE_BUF_N	K21	J20	GX_DCLK_BUF
GX_CONFIG_BUF_N	K20	J21	GX_DATA[6]
GX_DATA[0]	H17	J22	GX_LED[0]
GX_DATA[1]	H18	J23	No connect
GX_DATA[2]	L19	J24	DIFF_TX_P[11]
GX_DATA[3]	J19	J25	DIFF_TX_N[11]
GX_DATA[4]	G20	J26	1.5V_PLL
GX_DATA[5]	H20	J27	1.5V_PLL
GX_DATA[6]	J21	J28	DIFF_TX_P[15]
GX_DATA[7]	F21	J29	No connect
GX_DCLK_BUF	J20	J30	No connect
GX_DIG_1_A	C28	J31	BRIDGE_RX_P[8]
GX_DIG_1_B	B28	J32	BRIDGE_RX_N[8]
GX_DIG_1_C	C27	K1	XCVR_RX_P[3]
GX_DIG_1_D	B27	K2	XCVR_RX_N[3]
GX_DIG_1_DP	B26	K3	GND_HSSI
GX_DIG_1_E	A27	K4	GND_HSSI
GX_DIG_1_F	D26	K5	GND_HSSI
GX_DIG_1_G	C26	K6	1.5V_VCCG
GX_DIG_2_A	A28	K7	SFP0_MOD_DEF4_[0]
GX_DIG_2_B	D25	K8	GX_MICTOR_EP_[1]

Table 49. Stratix GX Pinout (Part 22 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GX_DIG_2_C	D23	K9	GX_MICTOR_EP_[3]
GX_DIG_2_D	B21	K10	GX_MICTOR_EP_[8]
GX_DIG_2_DP	A29	K11	GX_MICTOR_EP_[10]
GX_DIG_2_E	F20	K12	No connect
GX_DIG_2_F	C29	K13	GX_MICTOR_OP_[4]
GX_DIG_2_G	B29	K14	RDN_[4]
GX_DIP[0]	F15	K15	TCK
GX_DIP[1]	D15	K16	1.5V_PLL
GX_DIP[2]	E15	K17	1.5V_PLL
GX_DIP[3]	G8	K18	No connect
GX_DIP[4]	H10	K19	SFP3_RATE_SELECT[7]
GX_DIP[5]	H12	K20	GX_CONFIG_BUF_N
GX_DIP[6]	G14	K21	GX_CDONE_BUF_N
GX_DIP[7]	B14	K22	GND
GX_HEADER[0]	D21	K23	No connect
GX_HEADER[1]	A21	K24	DIFF_TX_P[10]
GX_HEADER[10]	E23	K25	DIFF_TX_N[10]
GX_HEADER[11]	A24	K26	GND_PLL
GX_HEADER[12]	B24	K27	GND_PLL
GX_HEADER[13]	C24	K28	DIFF_TX_N[12]
GX_HEADER[14]	D24	K29	BRIDGE_RX_P[10]
GX_HEADER[15]	A25	K30	BRIDGE_RX_N[10]
GX_HEADER[16]	B25	K31	BRIDGE_RX_P[3]
GX_HEADER[17]	C25	K32	BRIDGE_RX_N[3]
GX_HEADER[18]	A26	L1	GND_HSSI
GX_HEADER[19]	E25	L2	GND_HSSI
GX_HEADER[2]	A22	L3	GND_HSSI
GX_HEADER[3]	C22	L4	XCVR_TX_P[3]
GX_HEADER[4]	D22	L5	XCVR_TX_N[3]
GX_HEADER[5]	B22	L6	GND
GX_HEADER[6]	E22	L7	N20903737
GX_HEADER[7]	A23	L8	SFP0_MOD_DEF4_[1]
GX_HEADER[8]	B23	L9	GX_MICTOR_EP_[6]

Table 49. Stratix GX Pinout (Part 23 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GX_HEADER[9]	C23	L10	SFP0_RATE_SELECT[4]
GX_LED[0]	J22	L11	GX_MICTOR_EP_[13]
GX_LED[1]	E27	L12	GX_MICTOR_OP_[0]
GX_LED[2]	F26	L13	GX_MICTOR_OP_[3]
GX_LED[3]	B30	L14	SFP2_MOD_DEF6_[2]
GX_LED[4]	C30	L15	SFP3_MOD_DEF7_[2]
GX_LED[5]	E28	L16	GND_PLL
GX_MICTOR_EP_[0]	J8	L17	GND_PLL
GX_MICTOR_EP_[1]	K8	L18	1.5V_PLL
GX_MICTOR_EP_[10]	K11	L19	GX_DATA[2]
GX_MICTOR_EP_[11]	H11	L20	GX_TEMPDIODEN
GX_MICTOR_EP_[12]	J11	L21	GX_TEMPDIODEP
GX_MICTOR_EP_[13]	L11	L22	GX_STATUS_BUF_N
GX_MICTOR_EP_[14]	G11	L23	No connect
GX_MICTOR_EP_[15]	J12	L24	DIFF_TX_P[9]
GX_MICTOR_EP_[2]	J9	L25	DIFF_TX_N[9]
GX_MICTOR_EP_[3]	K9	L26	DIFF_TX_P[8]
GX_MICTOR_EP_[4]	G9	L27	DIFF_TX_N[8]
GX_MICTOR_EP_[5]	H8	L28	DIFF_TX_P[12]
GX_MICTOR_EP_[6]	L9	L29	BRIDGE_RX_P[7]
GX_MICTOR_EP_[7]	J10	L30	BRIDGE_RX_N[7]
GX_MICTOR_EP_[8]	K10	L31	BRIDGE_RX_P[6]
GX_MICTOR_EP_[9]	G10	L32	BRIDGE_RX_N[6]
GX_MICTOR_EP_CLK	H9	M1	XCVR_RX_P[17]
GX_MICTOR_OP_[0]	L12	M2	XCVR_RX_N[17]
GX_MICTOR_OP_[1]	H13	M3	GND_HSSI
GX_MICTOR_OP_[10]	J14	M4	GND_HSSI
GX_MICTOR_OP_[11]	G15	M5	GND_HSSI
GX_MICTOR_OP_[12]	H15	M6	3.3V_XCVR_CLKS
GX_MICTOR_OP_[13]	C14	M7	1.5V_XCVR[1]
GX_MICTOR_OP_[14]	A15	M8	1.5V_XCVR[1]
GX_MICTOR_OP_[15]	A14	M9	1.5V_VCCP
GX_MICTOR_OP_[2]	J13	M10	SFP0_TX_FAULT[4]

Table 49. Stratix GX Pinout (Part 24 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
GX_MICTOR_OP_[3]	L13	M11	SFP0_RX_LOS[4]
GX_MICTOR_OP_[4]	K13	M12	SFP1_TX_DISABLE[5]
GX_MICTOR_OP_[5]	G13	M13	GND_PLL
GX_MICTOR_OP_[6]	D14	M14	No connect
GX_MICTOR_OP_[7]	F14	M15	SFP3_TX_DISABLE[7]
GX_MICTOR_OP_[8]	E14	M16	GND_PLL
GX_MICTOR_OP_[9]	H14	M17	GND_PLL
GX_MICTOR_OP_CLK	G12	M18	No connect
GX_PB[0]	G23	M19	GND
GX_PB[1]	D28	M20	GND
GX_PB[2]	E26	M21	GND
GX_PB[3]	G24	M22	GND
GX_PB_DEV_CLR_N	AD14	M23	No connect
GX_PGM[0]	AD18	M24	GND
GX_PGM[1]	AF17	M25	DIFF_TX_TDCLK_P
GX_PGM[2]	AF21	M26	DIFF_TX_TDCLK_N
GX_PLL_ENA	AC20	M27	DIFF_TX_P[7]
GX_RECOV_CLK[0]	N17	M28	DIFF_TX_N[7]
GX_RECOV_CLK[1]	P14	M29	BRIDGE_RX_P[5]
GX_RECOV_CLK[2]	T12	M30	BRIDGE_RX_N[5]
GX_RECOV_CLK[3]	P10	M31	BRIDGE_RX_P[2]
GX_RECOV_CLK[4]	C15	M32	BRIDGE_RX_N[2]
GX_RS232_CTS	H23	N1	GND_HSSI
GX_RS232_RTS	G21	N2	GND_HSSI
GX_RS232_RXD	F25	N3	GND_HSSI
GX_RS232_TXD	H21	N4	XCVR_TX_P[17]
GX_RUNLU	AF18	N5	XCVR_TX_N[17]
GX_STATUS_BUF_N	L22	N6	1.5V_VCCG
GX_TDI[2]	H16	N7	1.5V_XCVR[1]
GX_TDO2_SW	J16	N8	1.5V_XCVR[1]
GX_TEMPDIODEN	L20	N9	1.5V_VCCP
GX_TEMPDIODEP	L21	N10	SFP0_TX_DISABLE[4]
GX_VCCSEL	AA15	N11	SFP1_MOD_DEF5_[1]

Table 49. Stratix GX Pinout (Part 25 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
MSEL[0]	AD20	N12	GND
MSEL[1]	AB20	N13	GND
MSEL[2]	AB19	N14	SFP2_TX_DISABLE[6]
N20903449	AC7	N15	GND
N20903653	T8	N16	GND
N20903737	L7	N17	GX_RECOV_CLK[0]
N20903841	J7	N18	SFP3_RX_LOS[7]
N33311607	T7	N19	3.3V_GX_IO
No connect	A17	N20	GND
No connect	AA10	N21	3.3V_GX_IO
No connect	AA11	N22	GND
No connect	AB10	N23	3.3V_GX_IO
No connect	AB21	N24	GND
No connect	AC21	N25	DIFF_TX_P[6]
No connect	AD7	N26	DIFF_TX_N[6]
No connect	AD8	N27	DIFF_TX_P[5]
No connect	AD9	N28	DIFF_TX_N[5]
No connect	AE8	N29	BRIDGE_RX_P[4]
No connect	AE9	N30	BRIDGE_RX_N[4]
No connect	AE16	N31	BRIDGE_RX_P[0]
No connect	AE17	N32	BRIDGE_RX_N[0]
No connect	AE20	P1	XCVR_RX_P[16]
No connect	AF9	P2	XCVR_RX_N[16]
No connect	AG19	P3	GND_HSSI
No connect	AG20	P4	GND_HSSI
No connect	AG21	P5	GND_HSSI
No connect	AG22	P6	GND
No connect	AG25	P7	1.5V_XCVR[2]
No connect	AG26	P8	1.5V_XCVR[2]
No connect	AH18	P9	1.5V_VCCP
No connect	AH19	P10	GX_RECOV_CLK[3]
No connect	AH20	P11	SFP1_MOD_DEF5_[2]
No connect	AH24	P12	SFP1_RX_LOS[5]

Table 49. Stratix GX Pinout (Part 26 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	AH27	P13	SFP2_MOD_DEF6_[0]
No connect	AH28	P14	GX_RECOV_CLK[1]
No connect	AH29	P15	1.5V_GX_INT
No connect	AH30	P16	GND
No connect	AJ19	P17	1.5V_GX_INT
No connect	AJ29	P18	GND
No connect	AJ30	P19	1.5V_GX_INT
No connect	AJ31	P20	1.5V_GX_INT
No connect	AJ32	P21	1.5V_GX_INT
No connect	B15	P22	1.5V_GX_INT
No connect	B17	P23	GND
No connect	B20	P24	DIFF_TX_P[3]
No connect	C17	P25	DIFF_TX_P[4]
No connect	C18	P26	DIFF_TX_N[4]
No connect	C20	P27	DIFF_TX_P[2]
No connect	D17	P28	DIFF_TX_N[2]
No connect	D18	P29	BRIDGE_RX_P[1]
No connect	D19	P30	BRIDGE_RX_N[1]
No connect	D20	P31	DPA_RX_P[1]
No connect	E18	P32	GND
No connect	E20	R1	GND_HSSI
No connect	E24	R2	GND_HSSI
No connect	E29	R3	GND_HSSI
No connect	E30	R4	XCVR_TX_P[16]
No connect	F18	R5	XCVR_TX_N[16]
No connect	F22	R6	3.3V_XCVR_CLKS
No connect	F24	R7	1.5V_XCVR[2]
No connect	F27	R8	1.5V_XCVR[2]
No connect	F28	R9	1.5V_VCCP
No connect	F29	R10	SFP1_MOD_DEF5_[0]
No connect	F30	R11	SFP1_RATE_SELECT[5]
No connect	G19	R12	SFP1_TX_FAULT[5]
No connect	G27	R13	SFP2_RATE_SELECT[6]

Table 49. Stratix GX Pinout (Part 27 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	G28	R14	SFP3_TX_FAULT[7]
No connect	J23	R15	1.5V_GX_INT
No connect	J29	R16	1.5V_GX_INT
No connect	J30	R17	GND
No connect	K12	R18	1.5V_GX_INT
No connect	K18	R19	GND
No connect	K23	R20	1.5V_GX_INT
No connect	L23	R21	1.5V_GX_INT
No connect	M14	R22	1.5V_GX_INT
No connect	M18	R23	GND
No connect	M23	R24	DIFF_TX_N[3]
No connect	V10	R25	DIFF_TX_P[0]
No connect	V12	R26	DIFF_TX_N[0]
No connect	V13	R27	DIFF_TX_P[1]
No connect	V29	R28	DIFF_TX_N[1]
No connect	V30	R29	DPA_RX_P[0]
No connect	V31	R30	DPA_RX_N[0]
No connect	W10	R31	DPA_RX_N[1]
No connect	W31	R32	3.3V_GX_IO
No connect	Y10	T1	SMA_INPUT4_TO_SGX_P
No connect	Y11	T2	SMA_INPUT4_TO_SGX_N
No connect	Y31	T3	GND_HSSI
No connect	Y32	T4	GND_HSSI
NIO_PULLUP	AB15	T5	GND_HSSI
PORSEL	AC15	T6	1.5V_VCCG
RDN[3]	AC14	T7	N33311607
RDN[4]	AD21	T8	N20903653
RDN_4]	K14	T9	1.5V_GX_INT
REFCLKB14N	A18	T10	GND
REFCLKB14P	B18	T11	3.3V_GX_IO
REFCLKB15N	B19	T12	GX_RECOV_CLK[2]
REFCLKB15P	C19	T13	SFP2_RX_LOS[6]
RUP[3]	AF19	T14	GND_PLL

Table 49. Stratix GX Pinout (Part 28 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
RUP[4]	AF20	T15	1.5V_GX_INT
RUP_[4]	H19	T16	GND
SFP0_MOD_DEF4_[0]	K7	T17	1.5V_GX_INT
SFP0_MOD_DEF4_[1]	L8	T18	GND
SFP0_MOD_DEF4_[2]	H7	T19	1.5V_GX_INT
SFP0_RATE_SELECT[4]	L10	T20	GND
SFP0_RX_LOS[4]	M11	T21	1.5V_GX_INT
SFP0_TX_DISABLE[4]	N10	T22	GND
SFP0_TX_FAULT[4]	M10	T23	DIFF_RX_DRSCCLK_P
SFP1_MOD_DEF5_[0]	R10	T24	3.3V_GX_IO
SFP1_MOD_DEF5_[1]	N11	T25	1.5V_PLL
SFP1_MOD_DEF5_[2]	P11	T26	GND_PLL
SFP1_RATE_SELECT[5]	R11	T27	1.5V_PLL
SFP1_RX_LOS[5]	P12	T28	GND_PLL
SFP1_TX_DISABLE[5]	M12	T29	DPACLK_IN_P
SFP1_TX_FAULT[5]	R12	T30	DPACLK_IN_N
SFP2_MOD_DEF6_[0]	P13	T31	BRIDGE_RXCLK_P
SFP2_MOD_DEF6_[1]	U12	T32	BRIDGE_RXCLK_N
SFP2_MOD_DEF6_[2]	L14	U1	GND_HSSI
SFP2_RATE_SELECT[6]	R13	U2	GND_HSSI
SFP2_RX_LOS[6]	T13	U3	GND_HSSI
SFP2_TX_DISABLE[6]	N14	U4	XCVR_TX_P[18]
SFP2_TX_FAULT[6]	G17	U5	XCVR_TX_N[18]
SFP3_MOD_DEF7_[0]	G18	U6	GND
SFP3_MOD_DEF7_[1]	J18	U7	1.5V_XCVR[5]
SFP3_MOD_DEF7_[2]	L15	U8	1.5V_XCVR[5]
SFP3_RATE_SELECT[7]	K19	U9	1.5V_VCCP
SFP3_RX_LOS[7]	N18	U10	GND
SFP3_TX_DISABLE[7]	M15	U11	2.5V_GX_IO
SFP3_TX_FAULT[7]	R14	U12	SFP2_MOD_DEF6_[1]
SMA_INPUT1_TO_SGX_N	AH16	U13	DDR_CLK_EN[0]
SMA_INPUT1_TO_SGX_P	AG16	U14	GND_PLL
SMA_INPUT2_TO_SGX_N	F2	U15	1.5V_GX_INT

Table 49. Stratix GX Pinout (Part 29 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
SMA_INPUT2_TO_SGX_P	F1	U16	1.5V_GX_INT
SMA_INPUT3_TO_SGX_N	B8	U17	GND
SMA_INPUT3_TO_SGX_P	A8	U18	1.5V_GX_INT
SMA_INPUT4_TO_SGX_N	T2	U19	GND
SMA_INPUT4_TO_SGX_P	T1	U20	1.5V_GX_INT
TCK	K15	U21	1.5V_GX_INT
TMS	G16	U22	GND
TP[10]	F23	U23	3.3V_GX_IO
TP[11]	AJ27	U24	DIFF_RX_DRCLK_N
TP[12]	B31	U25	1.5V_PLL
TP[13]	AG24	U26	GND_PLL
TP[17]	AG23	U27	1.5V_PLL
TP[8]	AD19	U28	GND_PLL
TRSTN	J15	U29	DIFF_TX_DTCLK_P
XCVR_RX_N[0]	D2	U30	DIFF_TX_DTCLK_N
XCVR_RX_N[1]	B2	U31	DIFF_RX_RDCLK_P
XCVR_RX_N[10]	AH2	U32	DIFF_RX_RDCLK_N
XCVR_RX_N[11]	AK2	V1	XCVR_RX_P[18]
XCVR_RX_N[12]	AL5	V2	XCVR_RX_N[18]
XCVR_RX_N[13]	AM3	V3	GND_HSSI
XCVR_RX_N[14]	AL9	V4	GND_HSSI
XCVR_RX_N[15]	AL11	V5	GND_HSSI
XCVR_RX_N[16]	P2	V6	3.3V_XCVR_CLKS
XCVR_RX_N[17]	M2	V7	1.5V_XCVR[5]
XCVR_RX_N[18]	V2	V8	1.5V_XCVR[5]
XCVR_RX_N[19]	Y2	V9	1.5V_VCCP
XCVR_RX_N[2]	H2	V10	No connect
XCVR_RX_N[3]	K2	V11	DDR_CS0_N
XCVR_RX_N[4]	B10	V12	No connect
XCVR_RX_N[5]	B12	V13	No connect
XCVR_RX_N[6]	B6	V14	DDR_A[3]
XCVR_RX_N[7]	B4	V15	1.5V_GX_INT
XCVR_RX_N[8]	AD2	V16	GND

Table 49. Stratix GX Pinout (Part 30 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
XCVR_RX_N[9]	AB2	V17	1.5V_GX_INT
XCVR_RX_P[0]	D1	V18	GND
XCVR_RX_P[1]	B1	V19	1.5V_GX_INT
XCVR_RX_P[10]	AH1	V20	GND
XCVR_RX_P[11]	AK1	V21	1.5V_GX_INT
XCVR_RX_P[12]	AM5	V22	1.5V_GX_INT
XCVR_RX_P[13]	AM2	V23	GND
XCVR_RX_P[14]	AM9	V24	BRIDGE_TX_P[13]
XCVR_RX_P[15]	AM11	V25	BRIDGE_TX_P[14]
XCVR_RX_P[16]	P1	V26	BRIDGE_TX_N[14]
XCVR_RX_P[17]	M1	V27	BRIDGE_TX_P[15]
XCVR_RX_P[18]	V1	V28	BRIDGE_TX_N[15]
XCVR_RX_P[19]	Y1	V29	No connect
XCVR_RX_P[2]	H1	V30	No connect
XCVR_RX_P[3]	K1	V31	No connect
XCVR_RX_P[4]	A10	V32	3.3V_GX_IO
XCVR_RX_P[5]	A12	W1	GND_HSSI
XCVR_RX_P[6]	A6	W2	GND_HSSI
XCVR_RX_P[7]	A4	W3	GND_HSSI
XCVR_RX_P[8]	AD1	W4	XCVR_TX_P[19]
XCVR_RX_P[9]	AB1	W5	XCVR_TX_N[19]
XCVR_TX_N[0]	G5	W6	1.5V_VCCG
XCVR_TX_N[1]	E4	W7	1.5V_XCVR[3]
XCVR_TX_N[10]	AE5	W8	1.5V_XCVR[3]
XCVR_TX_N[11]	AG5	W9	1.5V_VCCP
XCVR_TX_N[12]	AH7	W10	No connect
XCVR_TX_N[13]	AJ5	W11	DDR_CS1_N
XCVR_TX_N[14]	AH9	W12	DDR_WE_N
XCVR_TX_N[15]	AH11	W13	DDR_BA[0]
XCVR_TX_N[16]	R5	W14	DDR_A[8]
XCVR_TX_N[17]	N5	W15	1.5V_GX_INT
XCVR_TX_N[18]	U5	W16	1.5V_GX_INT
XCVR_TX_N[19]	W5	W17	GND

Table 49. Stratix GX Pinout (Part 31 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
XCVR_TX_N[2]	J5	W18	1.5V_GX_INT
XCVR_TX_N[3]	L5	W19	GND
XCVR_TX_N[4]	E10	W20	1.5V_GX_INT
XCVR_TX_N[5]	E12	W21	1.5V_GX_INT
XCVR_TX_N[6]	E8	W22	1.5V_GX_INT
XCVR_TX_N[7]	E6	W23	GND
XCVR_TX_N[8]	AC5	W24	BRIDGE_TX_N[13]
XCVR_TX_N[9]	AA5	W25	BRIDGE_TX_P[11]
XCVR_TX_P[0]	G4	W26	BRIDGE_TX_N[11]
XCVR_TX_P[1]	D4	W27	BRIDGE_TX_P[12]
XCVR_TX_P[10]	AE4	W28	BRIDGE_TX_N[12]
XCVR_TX_P[11]	AG4	W29	DIFF_RX_RCTL_P
XCVR_TX_P[12]	AJ7	W30	DIFF_RX_RCTL_N
XCVR_TX_P[13]	AJ4	W31	No connect
XCVR_TX_P[14]	AJ9	W32	GND
XCVR_TX_P[15]	AJ11	Y1	XCVR_RX_P[19]
XCVR_TX_P[16]	R4	Y2	XCVR_RX_N[19]
XCVR_TX_P[17]	N4	Y3	GND_HSSI
XCVR_TX_P[18]	U4	Y4	GND_HSSI
XCVR_TX_P[19]	W4	Y5	GND_HSSI
XCVR_TX_P[2]	J4	Y6	GND
XCVR_TX_P[3]	L4	Y7	1.5V_XCVR[3]
XCVR_TX_P[4]	D10	Y8	1.5V_XCVR[3]
XCVR_TX_P[5]	D12	Y9	1.5V_VCCP
XCVR_TX_P[6]	D8	Y10	No connect
XCVR_TX_P[7]	D6	Y11	No connect
XCVR_TX_P[8]	AC4	Y12	1.25V_GX_SSTL_VREF
XCVR_TX_P[9]	AA4	Y13	1.25V_GX_SSTL_VREF
XPAK_LASI	AH26	Y14	DDR_A[9]
XPAK_MOD_DET	AE21	Y15	1.25V_GX_SSTL_VREF
XPAK_PRTAD[0]	AK31	Y16	1.25V_GX_SSTL_VREF
XPAK_PRTAD[1]	AK30	Y17	DDR_A[2]
XPAK_PRTAD[2]	AL31	Y18	DDR_A[0]

Table 49. Stratix GX Pinout (Part 32 of 32)

Alphabetical Order by Signal Name		Alphabetical Order by Pin Number	
Signal Name	Pin Number	Pin Number	Signal Name
XPAK_PRTAD[3]	AL30	Y19	2.5V_GX_IO
XPAK_PRTAD[4]	AB22	Y20	GND
XPAK_TX_ON	AF23	Y21	2.5V_GX_IO
XPAK_VEND[0]	AJ28	Y22	GND
XPAK_VEND[1]	AF24	Y23	3.3V_GX_IO
XPAK_VEND[2]	AC22	Y24	GND
XPAK_VEND[3]	AD22	Y25	BRIDGE_TX_P[10]
XPAK_X_RST	AE23	Y26	BRIDGE_TX_N[10]
XTAL1_SGX_N	AL7	Y27	BRIDGE_TX_P[9]
XTAL1_SGX_P	AM7	Y28	BRIDGE_TX_N[9]
XTAL2_SGX_N	AF2	Y29	DIFF_RX_P[13]
XTAL2_SGX_P	AF1	Y30	DIFF_RX_N[13]
XTAL3_OUT_SGX	AL18	Y31	No connect
XTAL3_OUT_SGX_N	AM18	Y32	No connect

Stratix Pinout

Table 50 shows the Stratix device pinouts alphabetical by both signal name and pin number.

Table 50. Stratix Pinout (Part 1 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
1.5V_PLL	AG16	A2	GND
1.5V_PLL	AG17	A3	3.3V_S_IO
1.5V_PLL	AJ2	A4	No connect
1.5V_PLL	AJ31	A5	SCRUZ_IO[31]
1.5V_PLL	D2	A6	SCRUZ_IO[33]
1.5V_PLL	D31	A7	SCRUZ_IO[26]
1.5V_PLL	E16	A8	SCRUZ_IO[22]
1.5V_PLL	G17	A9	SCRUZ_IO[13]
1.5V_PLL	T8	A10	GND
1.5V_PLL	T25	A11	SCRUZ_IO[0]
1.5V_PLL	U8	A12	3.3V_S_IO

Table 50. Stratix Pinout (Part 2 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
1.5V_PLL	U25	A13	SCRUZ_IO[6]
1.5V_S_INT	AD16	A14	No connect
1.5V_S_INT	AF16	A15	GND_PLL
1.5V_S_INT	AJ3	A16	No connect
1.5V_S_INT	AJ30	A17	No connect
1.5V_S_INT	D3	A18	No connect
1.5V_S_INT	D30	A19	STX_PMC_CLK
1.5V_S_INT	H16	A20	PMC_REQN
1.5V_S_INT	J16	A21	3.3V_S_IO
1.5V_S_INT	M12	A22	PMC_AD[5]
1.5V_S_INT	M14	A23	GND
1.5V_S_INT	M19	A24	PMC_TRDYN
1.5V_S_INT	M21	A25	PMC_AD[16]
1.5V_S_INT	N13	A26	No connect
1.5V_S_INT	N15	A27	PMC_C_BEN[3]
1.5V_S_INT	N18	A28	PMC_AD[28]
1.5V_S_INT	N20	A29	PMC_INTAN
1.5V_S_INT	P12	A30	3.3V_S_IO
1.5V_S_INT	P14	A31	GND
1.5V_S_INT	P16	AA1	3.3V_S_IO
1.5V_S_INT	P17	AA2	BRIDGE_TX_P[4]
1.5V_S_INT	P19	AA3	BRIDGE_TX_N[4]
1.5V_S_INT	P21	AA4	BRIDGE_TX_N[6]
1.5V_S_INT	R13	AA5	BRIDGE_TX_P[6]
1.5V_S_INT	R15	AA6	No connect
1.5V_S_INT	R18	AA7	No connect
1.5V_S_INT	R20	AA8	No connect
1.5V_S_INT	R22	AA9	No connect
1.5V_S_INT	T9	AA10	GND
1.5V_S_INT	T14	AA11	No connect
1.5V_S_INT	T16	AA12	GX_FLASH_D[2]
1.5V_S_INT	T17	AA13	No connect
1.5V_S_INT	T19	AA14	No connect

Table 50. Stratix Pinout (Part 3 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
1.5V_S_INT	U14	AA15	No connect
1.5V_S_INT	U16	AA16	GND
1.5V_S_INT	U17	AA17	GND
1.5V_S_INT	U19	AA18	No connect
1.5V_S_INT	U24	AA19	No connect
1.5V_S_INT	V11	AA20	S_PGM[2]
1.5V_S_INT	V13	AA21	S_DIG_2_G
1.5V_S_INT	V15	AA22	No connect
1.5V_S_INT	V18	AA23	GND
1.5V_S_INT	V20	AA24	FLASH_A[5]
1.5V_S_INT	W14	AA25	FLASH_RESETN
1.5V_S_INT	W16	AA26	FLASH_CEN
1.5V_S_INT	W17	AA27	FLASH_WEN
1.5V_S_INT	W19	AA28	S_HEADER[1]
1.5V_S_INT	Y13	AA29	S_HEADER[0]
1.5V_S_INT	Y15	AA30	S_HEADER[4]
1.5V_S_INT	Y18	AA31	S_HEADER[5]
1.5V_S_INT	Y20	AA32	3.3V_S_IO
3.3V_PLL	AB17	AB1	BRIDGE_TX_P[7]
3.3V_PLL	AE17	AB2	BRIDGE_TX_P[5]
3.3V_PLL	H17	AB3	BRIDGE_TX_N[5]
3.3V_PLL	L17	AB4	GND_PLL
3.3V_S_IO	A3	AB5	GND_PLL
3.3V_S_IO	A12	AB6	No connect
3.3V_S_IO	A21	AB7	No connect
3.3V_S_IO	A30	AB8	GND
3.3V_S_IO	AA1	AB9	No connect
3.3V_S_IO	AA32	AB10	No connect
3.3V_S_IO	AC16	AB11	GX_FLASH_D[4]
3.3V_S_IO	AC17	AB12	No connect
3.3V_S_IO	AK1	AB13	GX_FLASH_D[15]
3.3V_S_IO	AK2	AB14	No connect
3.3V_S_IO	AK31	AB15	No connect

Table 50. Stratix Pinout (Part 4 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
3.3V_S_IO	AK32	AB16	GND_PLL
3.3V_S_IO	AM3	AB17	3.3V_PLL
3.3V_S_IO	AM12	AB18	No connect
3.3V_S_IO	AM21	AB19	S_DIG_1_DP
3.3V_S_IO	AM30	AB20	S_PB[0]
3.3V_S_IO	C1	AB21	S_DIG_2_F
3.3V_S_IO	C2	AB22	S_LED[0]
3.3V_S_IO	C31	AB23	No connect
3.3V_S_IO	C32	AB24	S_PB[2]
3.3V_S_IO	K16	AB25	GND
3.3V_S_IO	K17	AB26	FLASH_A[4]
3.3V_S_IO	M1	AB27	FLASH_OEN
3.3V_S_IO	M32	AB28	GND_PLL
3.3V_S_IO	T10	AB29	GND_PLL
3.3V_S_IO	T23	AB30	S_HEADER[2]
3.3V_S_IO	U10	AB31	S_HEADER[3]
3.3V_S_IO	U23	AB32	FLASH_A[3]
BRIDGE_RX_N[0]	R5	AC1	GND
BRIDGE_RX_N[1]	G6	AC2	BRIDGE_TX_N[7]
BRIDGE_RX_N[10]	N10	AC3	BRIDGE_TX_N[9]
BRIDGE_RX_N[11]	N5	AC4	BRIDGE_TX_P[9]
BRIDGE_RX_N[12]	P9	AC5	No connect
BRIDGE_RX_N[13]	N7	AC6	No connect
BRIDGE_RX_N[14]	P6	AC7	No connect
BRIDGE_RX_N[15]	R10	AC8	No connect
BRIDGE_RX_N[2]	H8	AC9	GX_FLASH_D[11]
BRIDGE_RX_N[3]	H5	AC10	No connect
BRIDGE_RX_N[4]	J7	AC11	No connect
BRIDGE_RX_N[5]	J5	AC12	GX_FLASH_D[1]
BRIDGE_RX_N[6]	K8	AC13	GX_EPC16_OEN
BRIDGE_RX_N[7]	K5	AC14	No connect
BRIDGE_RX_N[8]	M6	AC15	No connect
BRIDGE_RX_N[9]	M8	AC16	3.3V_S_IO

Table 50. Stratix Pinout (Part 5 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
BRIDGE_RX_P[0]	R6	AC17	3.3V_S_IO
BRIDGE_RX_P[1]	G5	AC18	No connect
BRIDGE_RX_P[10]	N9	AC19	No connect
BRIDGE_RX_P[11]	N6	AC20	RDN[8]
BRIDGE_RX_P[12]	P10	AC21	S_DIG_2_C
BRIDGE_RX_P[13]	N8	AC22	S_DIP[7]
BRIDGE_RX_P[14]	P5	AC23	S_DIP[0]
BRIDGE_RX_P[15]	R9	AC24	S_PB[3]
BRIDGE_RX_P[2]	H7	AC25	FLASH_D[15]
BRIDGE_RX_P[3]	H6	AC26	FLASH_D[14]
BRIDGE_RX_P[4]	J8	AC27	FLASH_D[13]
BRIDGE_RX_P[5]	J6	AC28	FLASH_D[12]
BRIDGE_RX_P[6]	K7	AC29	FLASH_A[21]
BRIDGE_RX_P[7]	K6	AC30	FLASH_A[20]
BRIDGE_RX_P[8]	M7	AC31	FLASH_A[2]
BRIDGE_RX_P[9]	M9	AC32	GND
BRIDGE_RXCLK_N	L6	AD1	No connect
BRIDGE_RXCLK_P	L7	AD2	No connect
BRIDGE_TX_N[0]	W2	AD3	BRIDGE_TX_N[8]
BRIDGE_TX_N[1]	W4	AD4	BRIDGE_TX_P[8]
BRIDGE_TX_N[10]	AE2	AD5	No connect
BRIDGE_TX_N[11]	AE4	AD6	No connect
BRIDGE_TX_N[12]	AF2	AD7	No connect
BRIDGE_TX_N[13]	AF4	AD8	No connect
BRIDGE_TX_N[14]	AG1	AD9	GX_FLASH_D[9]
BRIDGE_TX_N[15]	AG4	AD10	No connect
BRIDGE_TX_N[2]	Y2	AD11	No connect
BRIDGE_TX_N[3]	Y4	AD12	GX_FLASH_D[3]
BRIDGE_TX_N[4]	AA3	AD13	GX_EPC16_WEN
BRIDGE_TX_N[5]	AB3	AD14	GX_FLASH_D[14]
BRIDGE_TX_N[6]	AA4	AD15	No connect
BRIDGE_TX_N[7]	AC2	AD16	1.5V_S_INT
BRIDGE_TX_N[8]	AD3	AD17	GND

Table 50. Stratix Pinout (Part 6 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
BRIDGE_TX_N[9]	AC3	AD18	S_PGM[0]
BRIDGE_TX_P[0]	W1	AD19	S_DIG_1_C
BRIDGE_TX_P[1]	W3	AD20	S_DIG_1_G
BRIDGE_TX_P[10]	AE1	AD21	S_DIG_2_A
BRIDGE_TX_P[11]	AE3	AD22	S_DIG_2_E
BRIDGE_TX_P[12]	AF1	AD23	S_DIP[2]
BRIDGE_TX_P[13]	AF3	AD24	S_DIP[1]
BRIDGE_TX_P[14]	AG2	AD25	FLASH_D[8]
BRIDGE_TX_P[15]	AG3	AD26	FLASH_D[9]
BRIDGE_TX_P[2]	Y1	AD27	FLASH_D[10]
BRIDGE_TX_P[3]	Y3	AD28	FLASH_D[11]
BRIDGE_TX_P[4]	AA2	AD29	FLASH_A[18]
BRIDGE_TX_P[5]	AB2	AD30	FLASH_A[19]
BRIDGE_TX_P[6]	AA5	AD31	FLASH_A[0]
BRIDGE_TX_P[7]	AB1	AD32	FLASH_A[1]
BRIDGE_TX_P[8]	AD4	AE1	BRIDGE_TX_P[10]
BRIDGE_TX_P[9]	AC4	AE2	BRIDGE_TX_N[10]
BRIDGE_TXCLK_N	U1	AE3	BRIDGE_TX_P[11]
BRIDGE_TXCLK_P	U2	AE4	BRIDGE_TX_N[11]
CE_S_N	AF18	AE5	No connect
CEO_S_N	AH15	AE6	No connect
CF_ATASEL_N	H11	AE7	No connect
CF_CS_N	K12	AE8	No connect
CF_POWER	F12	AE9	GX_FLASH_D[12]
CF_PRESENT_N	J12	AE10	No connect
CF_REG	K13	AE11	GX_FLASH_D[5]
CF_RESET_N	H12	AE12	GX_FLASH_D[0]
CLK_FROM_SCRUZ	B15	AE13	GX_EPC16_CEN
CLK_TO_SCRUZ	AL18	AE14	No connect
CRC_ERROR	AF20	AE15	TP[29]
FLASH_A[0]	AD31	AE16	GND_PLL
FLASH_A[1]	AD32	AE17	3.3V_PLL
FLASH_A[10]	AF29	AE18	MSEL[1]

Table 50. Stratix Pinout (Part 7 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
FLASH_A[11]	AF30	AE19	MSEL[2]
FLASH_A[12]	AF31	AE20	S_DIG_1_D
FLASH_A[13]	AF32	AE21	No connect
FLASH_A[14]	AE29	AE22	No connect
FLASH_A[15]	AE30	AE23	S_DIP[5]
FLASH_A[16]	AE31	AE24	S_DIP[4]
FLASH_A[17]	AE32	AE25	FLASH_D[5]
FLASH_A[18]	AD29	AE26	FLASH_D[4]
FLASH_A[19]	AD30	AE27	FLASH_D[6]
FLASH_A[2]	AC31	AE28	FLASH_D[7]
FLASH_A[20]	AC30	AE29	FLASH_A[14]
FLASH_A[21]	AC29	AE30	FLASH_A[15]
FLASH_A[3]	AB32	AE31	FLASH_A[16]
FLASH_A[4]	AB26	AE32	FLASH_A[17]
FLASH_A[5]	AA24	AF1	BRIDGE_TX_P[12]
FLASH_A[6]	AG29	AF2	BRIDGE_TX_N[12]
FLASH_A[7]	AG30	AF3	BRIDGE_TX_P[13]
FLASH_A[8]	AG32	AF4	BRIDGE_TX_N[13]
FLASH_A[9]	AG31	AF5	No connect
FLASH_BYTEN	Y24	AF6	No connect
FLASH_CEN	AA26	AF7	No connect
FLASH_D[0]	AF25	AF8	No connect
FLASH_D[1]	AF26	AF9	GX_FLASH_D[13]
FLASH_D[10]	AD27	AF10	GX_FLASH_D[6]
FLASH_D[11]	AD28	AF11	No connect
FLASH_D[12]	AC28	AF12	No connect
FLASH_D[13]	AC27	AF13	No connect
FLASH_D[14]	AC26	AF14	S_RUNLU
FLASH_D[15]	AC25	AF15	NIO_PULLUP
FLASH_D[2]	AF28	AF16	1.5V_S_INT
FLASH_D[3]	AF27	AF17	GND
FLASH_D[4]	AE26	AF18	CE_S_N
FLASH_D[5]	AE25	AF19	S_PLL_ENA

Table 50. Stratix Pinout (Part 8 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
FLASH_D[6]	AE27	AF20	CRC_ERROR
FLASH_D[7]	AE28	AF21	No connect
FLASH_D[8]	AD25	AF22	S_DIG_2_D
FLASH_D[9]	AD26	AF23	S_LED[1]
FLASH_OEN	AB27	AF24	S_DIP[6]
FLASH_RESETN	AA25	AF25	FLASH_D[0]
FLASH_WEN	AA27	AF26	FLASH_D[1]
GND	A2	AF27	FLASH_D[3]
GND	A10	AF28	FLASH_D[2]
GND	A23	AF29	FLASH_A[10]
GND	A31	AF30	FLASH_A[11]
GND	AA10	AF31	FLASH_A[12]
GND	AA16	AF32	FLASH_A[13]
GND	AA17	AG1	BRIDGE_TX_N[14]
GND	AA23	AG2	BRIDGE_TX_P[14]
GND	AB8	AG3	BRIDGE_TX_P[15]
GND	AB25	AG4	BRIDGE_TX_N[15]
GND	AC1	AG5	No connect
GND	AC32	AG6	GND
GND	AD17	AG7	No connect
GND	AF17	AG8	No connect
GND	AG6	AG9	GX_FLASH_D[10]
GND	AG27	AG10	GX_FLASH_D[7]
GND	AH6	AG11	GX_FLASH_D[8]
GND	AH8	AG12	GX_EPC16_RPN
GND	AH10	AG13	No connect
GND	AH12	AG14	S_PGM[1]
GND	AH21	AG15	PORSEL
GND	AH23	AG16	1.5V_PLL
GND	AH25	AG17	1.5V_PLL
GND	AH27	AG18	MSEL[0]
GND	AL1	AG19	No connect
GND	AL2	AG20	S_DIG_1_E

Table 50. Stratix Pinout (Part 9 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
GND	AL31	AG21	S_DIG_1_F
GND	AL32	AG22	S_PB[1]
GND	AM2	AG23	S_DIG_2_B
GND	AM10	AG24	S_DIP[3]
GND	AM23	AG25	No connect
GND	AM31	AG26	No connect
GND	B1	AG27	GND
GND	B2	AG28	No connect
GND	B31	AG29	FLASH_A[6]
GND	B32	AG30	FLASH_A[7]
GND	E6	AG31	FLASH_A[9]
GND	E8	AG32	FLASH_A[8]
GND	E10	AH1	No connect
GND	E12	AH2	No connect
GND	E21	AH3	GND_PLL
GND	E23	AH4	No connect
GND	E25	AH5	GX_FLASH_A[2]
GND	E27	AH6	GND
GND	F6	AH7	No connect
GND	F27	AH8	GND
GND	H18	AH9	GX_FLASH_A[19]
GND	H24	AH10	GND
GND	J17	AH11	No connect
GND	K1	AH12	GND
GND	K32	AH13	No connect
GND	L8	AH14	S_PB_DEV_CLR_N
GND	L25	AH15	CEO_S_N
GND	M13	AH16	GND_PLL
GND	M15	AH17	GND_PLL
GND	M16	AH18	S_DIG_1_A
GND	M17	AH19	RUP[8]
GND	M18	AH20	S_MICTOR_EP_[2]
GND	M20	AH21	GND

Table 50. Stratix Pinout (Part 10 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
GND	N12	AH22	S_MICTOR_EP_[13]
GND	N14	AH23	GND
GND	N16	AH24	S_MICTOR_OP_[9]
GND	N17	AH25	GND
GND	N19	AH26	No connect
GND	N21	AH27	GND
GND	P13	AH28	No connect
GND	P15	AH29	No connect
GND	P18	AH30	GND_PLL
GND	P20	AH31	No connect
GND	R12	AH32	No connect
GND	R14	AJ1	GND_PLL
GND	R16	AJ2	1.5V_PLL
GND	R17	AJ3	1.5V_S_INT
GND	R19	AJ4	GX_FLASH_A[4]
GND	R21	AJ5	GX_FLASH_A[3]
GND	T12	AJ6	GX_FLASH_A[8]
GND	T13	AJ7	GX_FLASH_A[13]
GND	T15	AJ8	GX_FLASH_A[17]
GND	T18	AJ9	No connect
GND	T20	AJ10	No connect
GND	T21	AJ11	No connect
GND	U12	AJ12	No connect
GND	U13	AJ13	No connect
GND	U15	AJ14	S_VCCSEL
GND	U18	AJ15	GND_PLL
GND	U20	AJ16	STX_PMC_CLK
GND	U21	AJ17	SCRUZ_CLK_OSC_A
GND	V12	AJ18	S_DIG_1_B
GND	V14	AJ19	GND_PLL
GND	V16	AJ20	S_MICTOR_EP_[7]
GND	V17	AJ21	S_MICTOR_EP_[5]
GND	V19	AJ22	S_MICTOR_OP_CLK

Table 50. Stratix Pinout (Part 11 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
GND	V21	AJ23	S_MICTOR_EP_[15]
GND	W13	AJ24	S_MICTOR_OP_[8]
GND	W15	AJ25	S_MICTOR_OP_[5]
GND	W18	AJ26	S_MICTOR_OP_[14]
GND	W20	AJ27	S_MICTOR_OP_[7]
GND	Y14	AJ28	No connect
GND	Y16	AJ29	No connect
GND	Y17	AJ30	1.5V_S_INT
GND	Y19	AJ31	1.5V_PLL
GND_PLL	A15	AJ32	GND_PLL
GND_PLL	AB4	AK1	3.3V_S_IO
GND_PLL	AB5	AK2	3.3V_S_IO
GND_PLL	AB16	AK3	GX_FLASH_A[1]
GND_PLL	AB28	AK4	GX_FLASH_A[0]
GND_PLL	AB29	AK5	No connect
GND_PLL	AE16	AK6	GX_FLASH_A[9]
GND_PLL	AH3	AK7	GX_FLASH_A[11]
GND_PLL	AH16	AK8	No connect
GND_PLL	AH17	AK9	No connect
GND_PLL	AH30	AK10	No connect
GND_PLL	AJ1	AK11	No connect
GND_PLL	AJ15	AK12	No connect
GND_PLL	AJ19	AK13	No connect
GND_PLL	AJ32	AK14	No connect
GND_PLL	AK15	AK15	GND_PLL
GND_PLL	AL15	AK16	No connect
GND_PLL	AL17	AK17	No connect
GND_PLL	AL19	AK18	S_DIG_2_DP
GND_PLL	AM15	AK19	XTAL3_OUT_STX
GND_PLL	AM17	AK20	S_MICTOR_EP_[1]
GND_PLL	AM19	AK21	S_MICTOR_EP_[4]
GND_PLL	B19	AK22	S_MICTOR_EP_[9]
GND_PLL	C15	AK23	S_MICTOR_EP_[11]

Table 50. Stratix Pinout (Part 12 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
GND_PLL	C17	AK24	S_MICTOR_OP_[2]
GND_PLL	D1	AK25	S_MICTOR_OP_[4]
GND_PLL	D15	AK26	S_MICTOR_OP_[11]
GND_PLL	D17	AK27	S_MICTOR_OP_[15]
GND_PLL	D32	AK28	No connect
GND_PLL	E3	AK29	S_LED[5]
GND_PLL	E17	AK30	No connect
GND_PLL	E30	AK31	3.3V_S_IO
GND_PLL	F17	AK32	3.3V_S_IO
GND_PLL	H15	AL1	GND
GND_PLL	L4	AL2	GND
GND_PLL	L5	AL3	GX_FLASH_A[7]
GND_PLL	L16	AL4	GX_FLASH_A[6]
GND_PLL	L28	AL5	GX_FLASH_A[10]
GND_PLL	L29	AL6	GX_FLASH_A[15]
GND_PLL	T3	AL7	GX_FLASH_A[16]
GND_PLL	T4	AL8	No connect
GND_PLL	T5	AL9	No connect
GND_PLL	T6	AL10	No connect
GND_PLL	T7	AL11	No connect
GND_PLL	T22	AL12	No connect
GND_PLL	T24	AL13	No connect
GND_PLL	T26	AL14	No connect
GND_PLL	U3	AL15	GND_PLL
GND_PLL	U4	AL16	N31352757
GND_PLL	U7	AL17	GND_PLL
GND_PLL	U9	AL18	CLK_TO_SCRUZ
GND_PLL	U11	AL19	GND_PLL
GND_PLL	U26	AL20	S_MICTOR_EP_[0]
GND_PLL	U29	AL21	S_MICTOR_EP_[3]
GND_PLL	U30	AL22	S_MICTOR_EP_[8]
GND_PLL	U31	AL23	S_MICTOR_EP_[10]
GND_PLL	U32	AL24	S_MICTOR_EP_[14]

Table 50. Stratix Pinout (Part 13 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
GX_ALERTN	L14	AL25	S_MICTOR_OP_[3]
GX_EPC16_CEN	AE13	AL26	S_MICTOR_OP_[10]
GX_EPC16_OEN	AC13	AL27	No connect
GX_EPC16_RPN	AG12	AL28	S_MICTOR_OP_[6]
GX_EPC16_WEN	AD13	AL29	S_LED[3]
GX_FLASH_A[0]	AK4	AL30	S_LED[4]
GX_FLASH_A[1]	AK3	AL31	GND
GX_FLASH_A[10]	AL5	AL32	GND
GX_FLASH_A[11]	AK7	AM2	GND
GX_FLASH_A[12]	AM5	AM3	3.3V_S_IO
GX_FLASH_A[13]	AJ7	AM4	GX_FLASH_A[5]
GX_FLASH_A[14]	AM6	AM5	GX_FLASH_A[12]
GX_FLASH_A[15]	AL6	AM6	GX_FLASH_A[14]
GX_FLASH_A[16]	AL7	AM7	GX_FLASH_A[18]
GX_FLASH_A[17]	AJ8	AM8	GX_FLASH_A[20]
GX_FLASH_A[18]	AM7	AM9	No connect
GX_FLASH_A[19]	AH9	AM10	GND
GX_FLASH_A[2]	AH5	AM11	No connect
GX_FLASH_A[20]	AM8	AM12	3.3V_S_IO
GX_FLASH_A[3]	AJ5	AM13	No connect
GX_FLASH_A[4]	AJ4	AM14	No connect
GX_FLASH_A[5]	AM4	AM15	GND_PLL
GX_FLASH_A[6]	AL4	AM16	No connect
GX_FLASH_A[7]	AL3	AM17	GND_PLL
GX_FLASH_A[8]	AJ6	AM18	No connect
GX_FLASH_A[9]	AK6	AM19	GND_PLL
GX_FLASH_D[0]	AE12	AM20	S_MICTOR_EP_CLK
GX_FLASH_D[1]	AC12	AM21	3.3V_S_IO
GX_FLASH_D[10]	AG9	AM22	S_MICTOR_EP_[6]
GX_FLASH_D[11]	AC9	AM23	GND
GX_FLASH_D[12]	AE9	AM24	S_MICTOR_EP_[12]
GX_FLASH_D[13]	AF9	AM25	S_MICTOR_OP_[1]
GX_FLASH_D[14]	AD14	AM26	S_MICTOR_OP_[0]

Table 50. Stratix Pinout (Part 14 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
GX_FLASH_D[15]	AB13	AM27	S_MICTOR_OP_[13]
GX_FLASH_D[2]	AA12	AM28	S_MICTOR_OP_[12]
GX_FLASH_D[3]	AD12	AM29	S_LED[2]
GX_FLASH_D[4]	AB11	AM30	3.3V_S_IO
GX_FLASH_D[5]	AE11	AM31	GND
GX_FLASH_D[6]	AF10	B1	GND
GX_FLASH_D[7]	AG10	B2	GND
GX_FLASH_D[8]	AG11	B3	SCRUZ_CARDSELN
GX_FLASH_D[9]	AD9	B4	No connect
GX_OVERTEMPN	F13	B5	SCRUZ_IO[29]
GX_SMB_CLK	H13	B6	SCRUZ_IO[34]
GX_SMB_DATA	C14	B7	SCRUZ_IO[18]
LAN_A[0]	H30	B8	SCRUZ_IO[20]
LAN_A[1]	G30	B9	SCRUZ_IO[10]
LAN_A[10]	N32	B10	SCRUZ_IO[16]
LAN_A[11]	N31	B11	SCRUZ_IO[14]
LAN_A[12]	N30	B12	SCRUZ_IO[1]
LAN_A[13]	N29	B13	SCRUZ_IO[7]
LAN_A[14]	M30	B14	S_OVERTEMPN
LAN_A[2]	R29	B15	CLK_FROM_SCRUZ
LAN_A[3]	R30	B16	No connect
LAN_A[4]	R31	B17	No connect
LAN_A[5]	R32	B18	No connect
LAN_A[6]	P32	B19	GND_PLL
LAN_A[7]	P31	B20	PMC_GNTN
LAN_A[8]	P30	B21	STX_PMC_REQN
LAN_A[9]	P29	B22	PMC_AD[4]
LAN_AEN	M29	B23	PMC_SERRN
LAN_BEN[0]	K30	B24	PMC_DEVSELN
LAN_BEN[1]	J30	B25	PMC_C_BEN[2]
LAN_BEN[2]	J29	B26	PMC_AD[21]
LAN_BEN[3]	H32	B27	PMC_AD[17]
LAN_D[0]	J26	B28	PMC_AD[27]

Table 50. Stratix Pinout (Part 15 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
LAN_D[1]	J25	B29	PMC_AD[31]
LAN_D[10]	R27	B30	STX_PMC_REQN
LAN_D[11]	R28	B31	GND
LAN_D[12]	P27	B32	GND
LAN_D[13]	P28	C1	3.3V_S_IO
LAN_D[14]	N26	C2	3.3V_S_IO
LAN_D[15]	N25	C3	SCRUZ_IO[37]
LAN_D[16]	P24	C4	SCRUZ_IO[39]
LAN_D[17]	P23	C5	SCRUZ_SYS_RESETN
LAN_D[18]	N28	C6	SCRUZ_IO[28]
LAN_D[19]	N27	C7	SCRUZ_IO[30]
LAN_D[2]	H26	C8	SCRUZ_IO[24]
LAN_D[20]	N23	C9	SCRUZ_IO[23]
LAN_D[21]	N24	C10	SCRUZ_IO[12]
LAN_D[22]	M25	C11	SCRUZ_IO[15]
LAN_D[23]	M24	C12	SCRUZ_IO[2]
LAN_D[24]	M27	C13	SCRUZ_IO[3]
LAN_D[25]	M26	C14	GX_SMB_DATA
LAN_D[26]	L26	C15	GND_PLL
LAN_D[27]	L27	C16	S_DATA[3]
LAN_D[28]	K25	C17	GND_PLL
LAN_D[29]	K26	C18	No connect
LAN_D[3]	H25	C19	PMC_RESETN
LAN_D[30]	K27	C20	No connect
LAN_D[31]	K28	C21	STX_PMC_GNTN
LAN_D[4]	J28	C22	PMC_AD[3]
LAN_D[5]	J27	C23	PMC_AD[12]
LAN_D[6]	R24	C24	PMC_STOPN
LAN_D[7]	R23	C25	PMC_FRAMEN
LAN_D[8]	P26	C26	PMC_AD[20]
LAN_D[9]	P25	C27	PMC_AD[23]
LAN_DATACS_N	G31	C28	PMC_AD[26]
LAN_INTRQ[0]	L30	C29	PMC_AD[30]

Table 50. Stratix Pinout (Part 16 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
LAN_IOCHRDY	K31	C30	STX_PMC_GNTN
LAN_IORN	M28	C31	3.3V_S_IO
LAN_IOWN	L32	C32	3.3V_S_IO
LAN_LDEVN	J31	D1	GND_PLL
LAN_LOOPBACK	J32	D2	1.5V_PLL
LAN_RESET	L31	D3	1.5V_S_INT
LAN_SRDY_N	G32	D4	No connect
LAN_VLBUS_N	H29	D5	SCRUZ_IO[36]
MSEL[0]	AG18	D6	SCRUZ_IO[27]
MSEL[1]	AE18	D7	SCRUZ_IO[32]
MSEL[2]	AE19	D8	SCRUZ_IO[19]
N31352757	AL16	D9	SCRUZ_IO[25]
No connect	A4	D10	SCRUZ_IO[11]
No connect	A14	D11	SCRUZ_IO[17]
No connect	A16	D12	SCRUZ_IO[8]
No connect	A17	D13	SCRUZ_IO[4]
No connect	A18	D14	No connect
No connect	A26	D15	GND_PLL
No connect	AA6	D16	S_TDI[1]
No connect	AA7	D17	GND_PLL
No connect	AA8	D18	No connect
No connect	AA9	D19	PMC_RESETN
No connect	AA11	D20	No connect
No connect	AA13	D21	No connect
No connect	AA14	D22	PMC_AD[2]
No connect	AA15	D23	PMC_AD[11]
No connect	AA18	D24	PMC_PERRN
No connect	AA19	D25	PMC_IRDYN
No connect	AA22	D26	PMC_AD[19]
No connect	AB6	D27	PMC_AD[22]
No connect	AB7	D28	PMC_AD[25]
No connect	AB9	D29	PMC_AD[29]
No connect	AB10	D30	1.5V_S_INT

Table 50. Stratix Pinout (Part 17 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	AB12	D31	1.5V_PLL
No connect	AB14	D32	GND_PLL
No connect	AB15	E1	No connect
No connect	AB18	E2	No connect
No connect	AB23	E3	GND_PLL
No connect	AC5	E4	No connect
No connect	AC6	E5	SCRUZ_IO[38]
No connect	AC7	E6	GND
No connect	AC8	E7	SCRUZ_IO[35]
No connect	AC10	E8	GND
No connect	AC11	E9	SCRUZ_IO[21]
No connect	AC14	E10	GND
No connect	AC15	E11	SCRUZ_IO[9]
No connect	AC18	E12	GND
No connect	AC19	E13	SCRUZ_IO[5]
No connect	AD1	E14	S_DATA[0]
No connect	AD2	E15	TMS
No connect	AD5	E16	1.5V_PLL
No connect	AD6	E17	GND_PLL
No connect	AD7	E18	S_TEMPDIODEN
No connect	AD8	E19	S_DCLK_BUF
No connect	AD10	E20	No connect
No connect	AD11	E21	GND
No connect	AD15	E22	PMC_AD[1]
No connect	AE5	E23	GND
No connect	AE6	E24	PMC_PAR
No connect	AE7	E25	GND
No connect	AE8	E26	PMC_AD[18]
No connect	AE10	E27	GND
No connect	AE14	E28	PMC_AD[24]
No connect	AE21	E29	No connect
No connect	AE22	E30	GND_PLL
No connect	AF5	E31	No connect

Table 50. Stratix Pinout (Part 18 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	AF6	E32	No connect
No connect	AF7	F1	No connect
No connect	AF8	F2	No connect
No connect	AF11	F3	No connect
No connect	AF12	F4	No connect
No connect	AF13	F5	No connect
No connect	AF21	F6	GND
No connect	AG5	F7	No connect
No connect	AG7	F8	No connect
No connect	AG8	F9	No connect
No connect	AG13	F10	No connect
No connect	AG19	F11	No connect
No connect	AG25	F12	CF_POWER
No connect	AG26	F13	GX_OVERTEMPN
No connect	AG28	F14	S_DATA[1]
No connect	AH1	F15	S_DATA[2]
No connect	AH2	F16	S_TDO1_SW
No connect	AH4	F17	GND_PLL
No connect	AH7	F18	S_TEMPDIODEP
No connect	AH11	F19	PMC_INTCN
No connect	AH13	F20	PMC_INTDN
No connect	AH26	F21	No connect
No connect	AH28	F22	No connect
No connect	AH29	F23	PMC_AD[10]
No connect	AH31	F24	No connect
No connect	AH32	F25	No connect
No connect	AJ9	F26	PMC_AD[17]
No connect	AJ10	F27	GND
No connect	AJ11	F28	No connect
No connect	AJ12	F29	No connect
No connect	AJ13	F30	No connect
No connect	AJ28	F31	No connect
No connect	AJ29	F32	No connect

Table 50. Stratix Pinout (Part 19 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	AK5	G1	No connect
No connect	AK8	G2	No connect
No connect	AK9	G3	No connect
No connect	AK10	G4	No connect
No connect	AK11	G5	BRIDGE_RX_P[1]
No connect	AK12	G6	BRIDGE_RX_N[1]
No connect	AK13	G7	No connect
No connect	AK14	G8	No connect
No connect	AK16	G9	No connect
No connect	AK17	G10	No connect
No connect	AK28	G11	No connect
No connect	AK30	G12	No connect
No connect	AL8	G13	No connect
No connect	AL9	G14	TCK
No connect	AL10	G15	TRSTN
No connect	AL11	G16	S_STATUS_BUF_N
No connect	AL12	G17	1.5V_PLL
No connect	AL13	G18	S_CDONE_BUF_N
No connect	AL14	G19	S_DATA[4]
No connect	AL27	G20	No connect
No connect	AM9	G21	No connect
No connect	AM11	G22	No connect
No connect	AM13	G23	PMC_AD[9]
No connect	AM14	G24	PMC_C_BEN[1]
No connect	AM16	G25	No connect
No connect	AM18	G26	No connect
No connect	B4	G27	No connect
No connect	B16	G28	No connect
No connect	B17	G29	No connect
No connect	B18	G30	LAN_A[1]
No connect	C18	G31	LAN_DATACS_N
No connect	C20	G32	LAN_SRDY_N
No connect	D4	H1	No connect

Table 50. Stratix Pinout (Part 20 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	D14	H2	No connect
No connect	D18	H3	No connect
No connect	D20	H4	No connect
No connect	D21	H5	BRIDGE_RX_N[3]
No connect	E1	H6	BRIDGE_RX_P[3]
No connect	E2	H7	BRIDGE_RX_P[2]
No connect	E4	H8	BRIDGE_RX_N[2]
No connect	E20	H9	No connect
No connect	E29	H10	No connect
No connect	E31	H11	CF_ATASEL_N
No connect	E32	H12	CF_RESET_N
No connect	F1	H13	GX_SMB_CLK
No connect	F2	H14	S_ALERTN
No connect	F3	H15	GND_PLL
No connect	F4	H16	1.5V_S_INT
No connect	F5	H17	3.3V_PLL
No connect	F7	H18	GND
No connect	F8	H19	PMC_LOCKN
No connect	F9	H20	PMC_M66EN
No connect	F10	H21	No connect
No connect	F11	H22	PMC_AD[0]
No connect	F21	H23	PMC_AD[8]
No connect	F22	H24	GND
No connect	F24	H25	LAN_D[3]
No connect	F25	H26	LAN_D[2]
No connect	F28	H27	No connect
No connect	F29	H28	No connect
No connect	F30	H29	LAN_VLBUS_N
No connect	F31	H30	LAN_A[0]
No connect	F32	H31	No connect
No connect	G1	H32	LAN_BEN[3]
No connect	G2	J1	No connect
No connect	G3	J2	No connect

Table 50. Stratix Pinout (Part 21 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	G4	J3	No connect
No connect	G7	J4	No connect
No connect	G8	J5	BRIDGE_RX_N[5]
No connect	G9	J6	BRIDGE_RX_P[5]
No connect	G10	J7	BRIDGE_RX_N[4]
No connect	G11	J8	BRIDGE_RX_P[4]
No connect	G12	J9	No connect
No connect	G13	J10	No connect
No connect	G20	J11	No connect
No connect	G21	J12	CF_PRESENT_N
No connect	G22	J13	No connect
No connect	G25	J14	S_SMB_DATA
No connect	G26	J15	S_SMB_CLK
No connect	G27	J16	1.5V_S_INT
No connect	G28	J17	GND
No connect	G29	J18	S_CONFIG_BUF_N
No connect	H1	J19	S_DATA[5]
No connect	H2	J20	S_DATA[7]
No connect	H3	J21	PMC_BUSMODEN[2]
No connect	H4	J22	No connect
No connect	H9	J23	PMC_C_BEN[0]
No connect	H10	J24	PMC_AD[15]
No connect	H21	J25	LAN_D[1]
No connect	H27	J26	LAN_D[0]
No connect	H28	J27	LAN_D[5]
No connect	H31	J28	LAN_D[4]
No connect	J1	J29	LAN_BEN[2]
No connect	J2	J30	LAN_BEN[1]
No connect	J3	J31	LAN_LDEVN
No connect	J4	J32	LAN_LOOPBACK
No connect	J9	K1	GND
No connect	J10	K2	No connect
No connect	J11	K3	No connect

Table 50. Stratix Pinout (Part 22 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	J13	K4	No connect
No connect	J22	K5	BRIDGE_RX_N[7]
No connect	K2	K6	BRIDGE_RX_P[7]
No connect	K3	K7	BRIDGE_RX_P[6]
No connect	K4	K8	BRIDGE_RX_N[6]
No connect	K9	K9	No connect
No connect	K10	K10	No connect
No connect	K11	K11	No connect
No connect	K14	K12	CF_CS_N
No connect	K15	K13	CF_REG
No connect	K20	K14	No connect
No connect	K22	K15	No connect
No connect	K29	K16	3.3V_S_IO
No connect	L1	K17	3.3V_S_IO
No connect	L2	K18	PMC_INTBN
No connect	L3	K19	S_DATA[6]
No connect	L9	K20	No connect
No connect	L10	K21	PMC_BUSMODEN[3]
No connect	L11	K22	No connect
No connect	L12	K23	PMC_AD[7]
No connect	L13	K24	PMC_AD[14]
No connect	L15	K25	LAN_D[28]
No connect	L18	K26	LAN_D[29]
No connect	L19	K27	LAN_D[30]
No connect	L22	K28	LAN_D[31]
No connect	M2	K29	No connect
No connect	M3	K30	LAN_BEN[0]
No connect	M4	K31	LAN_IOCHRDY
No connect	M5	K32	GND
No connect	M10	L1	No connect
No connect	M11	L2	No connect
No connect	M22	L3	No connect
No connect	M23	L4	GND_PLL

Table 50. Stratix Pinout (Part 23 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	M31	L5	GND_PLL
No connect	N1	L6	BRIDGE_RXCLK_N
No connect	N2	L7	BRIDGE_RXCLK_P
No connect	N3	L8	GND
No connect	N4	L9	No connect
No connect	N11	L10	No connect
No connect	N22	L11	No connect
No connect	P1	L12	No connect
No connect	P2	L13	No connect
No connect	P3	L14	GX_ALERTN
No connect	P4	L15	No connect
No connect	P7	L16	GND_PLL
No connect	P8	L17	3.3V_PLL
No connect	P11	L18	No connect
No connect	P22	L19	No connect
No connect	R1	L20	PMC_BUSMODEN[1]
No connect	R2	L21	PMC_BUSMODEN[4]
No connect	R3	L22	No connect
No connect	R4	L23	PMC_AD[6]
No connect	R7	L24	PMC_AD[13]
No connect	R8	L25	GND
No connect	R11	L26	LAN_D[26]
No connect	R25	L27	LAN_D[27]
No connect	R26	L28	GND_PLL
No connect	T1	L29	GND_PLL
No connect	T2	L30	LAN_INTRQ[0]
No connect	T11	L31	LAN_RESET
No connect	T31	L32	LAN_IOWN
No connect	T32	M1	3.3V_S_IO
No connect	U5	M2	No connect
No connect	U6	M3	No connect
No connect	U22	M4	No connect
No connect	U27	M5	No connect

Table 50. Stratix Pinout (Part 24 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	U28	M6	BRIDGE_RX_N[8]
No connect	V1	M7	BRIDGE_RX_P[8]
No connect	V2	M8	BRIDGE_RX_N[9]
No connect	V3	M9	BRIDGE_RX_P[9]
No connect	V4	M10	No connect
No connect	V5	M11	No connect
No connect	V6	M12	1.5V_S_INT
No connect	V7	M13	GND
No connect	V8	M14	1.5V_S_INT
No connect	V9	M15	GND
No connect	V10	M16	GND
No connect	V22	M17	GND
No connect	V25	M18	GND
No connect	V26	M19	1.5V_S_INT
No connect	W5	M20	GND
No connect	W6	M21	1.5V_S_INT
No connect	W7	M22	No connect
No connect	W8	M23	No connect
No connect	W9	M24	LAN_D[23]
No connect	W10	M25	LAN_D[22]
No connect	W11	M26	LAN_D[25]
No connect	W12	M27	LAN_D[24]
No connect	W21	M28	LAN_IORN
No connect	W22	M29	LAN_AEN
No connect	Y5	M30	LAN_A[14]
No connect	Y6	M31	No connect
No connect	Y7	M32	3.3V_S_IO
No connect	Y8	N1	No connect
No connect	Y9	N2	No connect
No connect	Y10	N3	No connect
No connect	Y11	N4	No connect
No connect	Y12	N5	BRIDGE_RX_N[11]
No connect	Y21	N6	BRIDGE_RX_P[11]

Table 50. Stratix Pinout (Part 25 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
No connect	Y22	N7	BRIDGE_RX_N[13]
NIO_PULLUP	AF15	N8	BRIDGE_RX_P[13]
PMC_AD[0]	H22	N9	BRIDGE_RX_P[10]
PMC_AD[1]	E22	N10	BRIDGE_RX_N[10]
PMC_AD[10]	F23	N11	No connect
PMC_AD[11]	D23	N12	GND
PMC_AD[12]	C23	N13	1.5V_S_INT
PMC_AD[13]	L24	N14	GND
PMC_AD[14]	K24	N15	1.5V_S_INT
PMC_AD[15]	J24	N16	GND
PMC_AD[16]	A25	N17	GND
PMC_AD[17]	B27	N18	1.5V_S_INT
PMC_AD[17]	F26	N19	GND
PMC_AD[18]	E26	N20	1.5V_S_INT
PMC_AD[19]	D26	N21	GND
PMC_AD[2]	D22	N22	No connect
PMC_AD[20]	C26	N23	LAN_D[20]
PMC_AD[21]	B26	N24	LAN_D[21]
PMC_AD[22]	D27	N25	LAN_D[15]
PMC_AD[23]	C27	N26	LAN_D[14]
PMC_AD[24]	E28	N27	LAN_D[19]
PMC_AD[25]	D28	N28	LAN_D[18]
PMC_AD[26]	C28	N29	LAN_A[13]
PMC_AD[27]	B28	N30	LAN_A[12]
PMC_AD[28]	A28	N31	LAN_A[11]
PMC_AD[29]	D29	N32	LAN_A[10]
PMC_AD[3]	C22	P1	No connect
PMC_AD[30]	C29	P2	No connect
PMC_AD[31]	B29	P3	No connect
PMC_AD[4]	B22	P4	No connect
PMC_AD[5]	A22	P5	BRIDGE_RX_P[14]
PMC_AD[6]	L23	P6	BRIDGE_RX_N[14]
PMC_AD[7]	K23	P7	No connect

Table 50. Stratix Pinout (Part 26 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
PMC_AD[8]	H23	P8	No connect
PMC_AD[9]	G23	P9	BRIDGE_RX_N[12]
PMC_BUSMODEN[1]	L20	P10	BRIDGE_RX_P[12]
PMC_BUSMODEN[2]	J21	P11	No connect
PMC_BUSMODEN[3]	K21	P12	1.5V_S_INT
PMC_BUSMODEN[4]	L21	P13	GND
PMC_C_BEN[0]	J23	P14	1.5V_S_INT
PMC_C_BEN[1]	G24	P15	GND
PMC_C_BEN[2]	B25	P16	1.5V_S_INT
PMC_C_BEN[3]	A27	P17	1.5V_S_INT
PMC_DEVSELN	B24	P18	GND
PMC_FRAMEN	C25	P19	1.5V_S_INT
PMC_GNTN	B20	P20	GND
PMC_INTAN	A29	P21	1.5V_S_INT
PMC_INTBN	K18	P22	No connect
PMC_INTCN	F19	P23	LAN_D[17]
PMC_INTDN	F20	P24	LAN_D[16]
PMC_IRDYN	D25	P25	LAN_D[9]
PMC_LOCKN	H19	P26	LAN_D[8]
PMC_M66EN	H20	P27	LAN_D[12]
PMC_PAR	E24	P28	LAN_D[13]
PMC_PERRN	D24	P29	LAN_A[9]
PMC_REQN	A20	P30	LAN_A[8]
PMC_RESETN	C19	P31	LAN_A[7]
PMC_RESETN	D19	P32	LAN_A[6]
PMC_SERRN	B23	R1	No connect
PMC_STOPN	C24	R2	No connect
PMC_TRDYN	A24	R3	No connect
PORSEL	AG15	R4	No connect
RDN[8]	AC20	R5	BRIDGE_RX_N[0]
RUP[8]	AH19	R6	BRIDGE_RX_P[0]
S_ALERTN	H14	R7	No connect
S_CDONE_BUF_N	G18	R8	No connect

Table 50. Stratix Pinout (Part 27 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
S_CONFIG_BUF_N	J18	R9	BRIDGE_RX_P[15]
S_DATA[0]	E14	R10	BRIDGE_RX_N[15]
S_DATA[1]	F14	R11	No connect
S_DATA[2]	F15	R12	GND
S_DATA[3]	C16	R13	1.5V_S_INT
S_DATA[4]	G19	R14	GND
S_DATA[5]	J19	R15	1.5V_S_INT
S_DATA[6]	K19	R16	GND
S_DATA[7]	J20	R17	GND
S_DCLK_BUF	E19	R18	1.5V_S_INT
S_DIG_1_A	AH18	R19	GND
S_DIG_1_B	AJ18	R20	1.5V_S_INT
S_DIG_1_C	AD19	R21	GND
S_DIG_1_D	AE20	R22	1.5V_S_INT
S_DIG_1_DP	AB19	R23	LAN_D[7]
S_DIG_1_E	AG20	R24	LAN_D[6]
S_DIG_1_F	AG21	R25	No connect
S_DIG_1_G	AD20	R26	No connect
S_DIG_2_A	AD21	R27	LAN_D[10]
S_DIG_2_B	AG23	R28	LAN_D[11]
S_DIG_2_C	AC21	R29	LAN_A[2]
S_DIG_2_D	AF22	R30	LAN_A[3]
S_DIG_2_DP	AK18	R31	LAN_A[4]
S_DIG_2_E	AD22	R32	LAN_A[5]
S_DIG_2_F	AB21	T1	No connect
S_DIG_2_G	AA21	T2	No connect
S_DIP[0]	AC23	T3	GND_PLL
S_DIP[1]	AD24	T4	GND_PLL
S_DIP[2]	AD23	T5	GND_PLL
S_DIP[3]	AG24	T6	GND_PLL
S_DIP[4]	AE24	T7	GND_PLL
S_DIP[5]	AE23	T8	1.5V_PLL
S_DIP[6]	AF24	T9	1.5V_S_INT

Table 50. Stratix Pinout (Part 28 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
S_DIP[7]	AC22	T10	3.3V_S_IO
S_EPC16_CEN	V23	T11	No connect
S_EPC16_OEN	Y26	T12	GND
S_EPC16_RPN	W28	T13	GND
S_EPC16_WEN	V24	T14	1.5V_S_INT
S_HEADER[0]	AA29	T15	GND
S_HEADER[1]	AA28	T16	1.5V_S_INT
S_HEADER[10]	W29	T17	1.5V_S_INT
S_HEADER[11]	W30	T18	GND
S_HEADER[12]	W31	T19	1.5V_S_INT
S_HEADER[13]	W32	T20	GND
S_HEADER[14]	V29	T21	GND
S_HEADER[15]	V30	T22	GND_PLL
S_HEADER[16]	V31	T23	3.3V_S_IO
S_HEADER[17]	V32	T24	GND_PLL
S_HEADER[18]	Y23	T25	1.5V_PLL
S_HEADER[19]	Y25	T26	GND_PLL
S_HEADER[2]	AB30	T27	XTAL2_STX_P
S_HEADER[3]	AB31	T28	XTAL2_STX_N
S_HEADER[4]	AA30	T29	XTAL1_STX_P
S_HEADER[5]	AA31	T30	XTAL1_STX_N
S_HEADER[6]	Y29	T31	No connect
S_HEADER[7]	Y30	T32	No connect
S_HEADER[8]	Y31	U1	BRIDGE_TXCLK_N
S_HEADER[9]	Y32	U2	BRIDGE_TXCLK_P
S_LED[0]	AB22	U3	GND_PLL
S_LED[1]	AF23	U4	GND_PLL
S_LED[2]	AM29	U5	No connect
S_LED[3]	AL29	U6	No connect
S_LED[4]	AL30	U7	GND_PLL
S_LED[5]	AK29	U8	1.5V_PLL
S_MICTOR_EP_[0]	AL20	U9	GND_PLL
S_MICTOR_EP_[1]	AK20	U10	3.3V_S_IO

Table 50. Stratix Pinout (Part 29 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
S_MICTOR_EP_[10]	AL23	U11	GND_PLL
S_MICTOR_EP_[11]	AK23	U12	GND
S_MICTOR_EP_[12]	AM24	U13	GND
S_MICTOR_EP_[13]	AH22	U14	1.5V_S_INT
S_MICTOR_EP_[14]	AL24	U15	GND
S_MICTOR_EP_[15]	AJ23	U16	1.5V_S_INT
S_MICTOR_EP_[2]	AH20	U17	1.5V_S_INT
S_MICTOR_EP_[3]	AL21	U18	GND
S_MICTOR_EP_[4]	AK21	U19	1.5V_S_INT
S_MICTOR_EP_[5]	AJ21	U20	GND
S_MICTOR_EP_[6]	AM22	U21	GND
S_MICTOR_EP_[7]	AJ20	U22	No connect
S_MICTOR_EP_[8]	AL22	U23	3.3V_S_IO
S_MICTOR_EP_[9]	AK22	U24	1.5V_S_INT
S_MICTOR_EP_CLK	AM20	U25	1.5V_PLL
S_MICTOR_OP_[0]	AM26	U26	GND_PLL
S_MICTOR_OP_[1]	AM25	U27	No connect
S_MICTOR_OP_[10]	AL26	U28	No connect
S_MICTOR_OP_[11]	AK26	U29	GND_PLL
S_MICTOR_OP_[12]	AM28	U30	GND_PLL
S_MICTOR_OP_[13]	AM27	U31	GND_PLL
S_MICTOR_OP_[14]	AJ26	U32	GND_PLL
S_MICTOR_OP_[15]	AK27	V1	No connect
S_MICTOR_OP_[2]	AK24	V2	No connect
S_MICTOR_OP_[3]	AL25	V3	No connect
S_MICTOR_OP_[4]	AK25	V4	No connect
S_MICTOR_OP_[5]	AJ25	V5	No connect
S_MICTOR_OP_[6]	AL28	V6	No connect
S_MICTOR_OP_[7]	AJ27	V7	No connect
S_MICTOR_OP_[8]	AJ24	V8	No connect
S_MICTOR_OP_[9]	AH24	V9	No connect
S_MICTOR_OP_CLK	AJ22	V10	No connect
S_OVERTEMP_N	B14	V11	1.5V_S_INT

Table 50. Stratix Pinout (Part 30 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
S_PB[0]	AB20	V12	GND
S_PB[1]	AG22	V13	1.5V_S_INT
S_PB[2]	AB24	V14	GND
S_PB[3]	AC24	V15	1.5V_S_INT
S_PB_DEV_CLR_N	AH14	V16	GND
S_PGM[0]	AD18	V17	GND
S_PGM[1]	AG14	V18	1.5V_S_INT
S_PGM[2]	AA20	V19	GND
S_PLL_ENA	AF19	V20	1.5V_S_INT
S_RS232_CTS	Y28	V21	GND
S_RS232_RTS	W23	V22	No connect
S_RS232_RXD	Y27	V23	S_EPC16_CEN
S_RS232_TXD	W24	V24	S_EPC16_WEN
S_RUNLU	AF14	V25	No connect
S_SMB_CLK	J15	V26	No connect
S_SMB_DATA	J14	V27	TP[21]
S_STATUS_BUF_N	G16	V28	TP[22]
S_TDI[1]	D16	V29	S_HEADER[14]
S_TDO1_SW	F16	V30	S_HEADER[15]
S_TEMPDIODEN	E18	V31	S_HEADER[16]
S_TEMPDIODEP	F18	V32	S_HEADER[17]
S_VCCSEL	AJ14	W1	BRIDGE_TX_P[0]
SCRUZ_CARDSELN	B3	W2	BRIDGE_TX_N[0]
SCRUZ_CLK_OSC_A	AJ17	W3	BRIDGE_TX_P[1]
SCRUZ_IO[0]	A11	W4	BRIDGE_TX_N[1]
SCRUZ_IO[1]	B12	W5	No connect
SCRUZ_IO[10]	B9	W6	No connect
SCRUZ_IO[11]	D10	W7	No connect
SCRUZ_IO[12]	C10	W8	No connect
SCRUZ_IO[13]	A9	W9	No connect
SCRUZ_IO[14]	B11	W10	No connect
SCRUZ_IO[15]	C11	W11	No connect
SCRUZ_IO[16]	B10	W12	No connect

Table 50. Stratix Pinout (Part 31 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
SCRUZ_IO[17]	D11	W13	GND
SCRUZ_IO[18]	B7	W14	1.5V_S_INT
SCRUZ_IO[19]	D8	W15	GND
SCRUZ_IO[2]	C12	W16	1.5V_S_INT
SCRUZ_IO[20]	B8	W17	1.5V_S_INT
SCRUZ_IO[21]	E9	W18	GND
SCRUZ_IO[22]	A8	W19	1.5V_S_INT
SCRUZ_IO[23]	C9	W20	GND
SCRUZ_IO[24]	C8	W21	No connect
SCRUZ_IO[25]	D9	W22	No connect
SCRUZ_IO[26]	A7	W23	S_RS232_RTS
SCRUZ_IO[27]	D6	W24	S_RS232_TXD
SCRUZ_IO[28]	C6	W25	TP[25]
SCRUZ_IO[29]	B5	W26	TP[24]
SCRUZ_IO[3]	C13	W27	TP[23]
SCRUZ_IO[30]	C7	W28	S_EPC16_RPN
SCRUZ_IO[31]	A5	W29	S_HEADER[10]
SCRUZ_IO[32]	D7	W30	S_HEADER[11]
SCRUZ_IO[33]	A6	W31	S_HEADER[12]
SCRUZ_IO[34]	B6	W32	S_HEADER[13]
SCRUZ_IO[35]	E7	Y1	BRIDGE_TX_P[2]
SCRUZ_IO[36]	D5	Y2	BRIDGE_TX_N[2]
SCRUZ_IO[37]	C3	Y3	BRIDGE_TX_P[3]
SCRUZ_IO[38]	E5	Y4	BRIDGE_TX_N[3]
SCRUZ_IO[39]	C4	Y5	No connect
SCRUZ_IO[4]	D13	Y6	No connect
SCRUZ_IO[5]	E13	Y7	No connect
SCRUZ_IO[6]	A13	Y8	No connect
SCRUZ_IO[7]	B13	Y9	No connect
SCRUZ_IO[8]	D12	Y10	No connect
SCRUZ_IO[9]	E11	Y11	No connect
SCRUZ_SYS_RESETN	C5	Y12	No connect
STX_PMC_CLK	A19	Y13	1.5V_S_INT

Table 50. Stratix Pinout (Part 32 of 32)

Alphabetical by Signal Name		Alphabetical by Pin Name	
Signal Name	Pin Number	Pin Number	Signal Name
STX_PMC_CLK	AJ16	Y14	GND
STX_PMC_GNTN	C21	Y15	1.5V_S_INT
STX_PMC_GNTN	C30	Y16	GND
STX_PMC_REQN	B21	Y17	GND
STX_PMC_REQN	B30	Y18	1.5V_S_INT
TCK	G14	Y19	GND
TMS	E15	Y20	1.5V_S_INT
TP[21]	V27	Y21	No connect
TP[22]	V28	Y22	No connect
TP[23]	W27	Y23	S_HEADER[18]
TP[24]	W26	Y24	FLASH_BYTEN
TP[25]	W25	Y25	S_HEADER[19]
TP[29]	AE15	Y26	S_EPC16_OEN
TRSTN	G15	Y27	S_RS232_RXD
XTAL1_STX_N	T30	Y28	S_RS232_CTS
XTAL1_STX_P	T29	Y29	S_HEADER[6]
XTAL2_STX_N	T28	Y30	S_HEADER[7]
XTAL2_STX_P	T27	Y31	S_HEADER[8]
XTAL3_OUT_STX	AK19	Y32	S_HEADER[9]



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