PCI Express Compiler

Introduction

The PCI Express Compiler generates customized PCI Express MegaCore® functions that you can use to design PCI Express endpoints, including nontransparent bridges, or unique designs combining multiple PCI Express components in a single Altera® device. The PCI Express MegaCore functions are compliant with *PCI Express Base Specification Revision 1.0a*, implementing all required and most optional specification features for the transaction, data link, and physical layers.

Features

The PCI Express Compiler includes the following features:

- Suitable for endpoints, including non-transparent bridges
- x1 and x4 MegaCore functions
- Stratix® II & Stratix GX device support
  - Intel's PIPE interface (8- or 16-bit) between the MAC and PHY layers for Stratix II devices
  - Integrated PHY layer for Stratix GX devices
- Supports all memory, I/O, configuration, and message transactions
- Highly optimized application interface for maximizing throughput and minimizing latency
- Supports up to four virtual channels (VCs)
  - Dedicated receive buffer per VC, configurable from 1 to 16 Kbytes deep
  - Configurable receive buffer allocation & flow control credits
- Configurable maximum payload up to 2 KBytes (128, 256, 512, 1024, or 2048 bytes)
- Configurable retry buffer size (from 256 bytes to 16 KBytes)
- Optional end-to-end cyclic redundancy code (ECRC) generation/checking
- Flexible reference clock support, including 100, 125, or 156.25 MHz
- Optional advanced error reporting (AER)
- Message signaled interrupt (MSI) generation
- Legacy PCI interrupt message generation
- Configurable base address register (BAR) sizes and address spaces, including expansion ROM for endpoints (type 0 configuration space header)
- Configurable PCI read-only registers
- Support for PCI legacy power management device states (D0, $D3_{HOT}$, and $D3_{COLD}$)
- System debug support, including inputs to enable specific modes (e.g., remote boot, error generation) and outputs for monitoring errors, state machine, flow control, etc.
- Easy-to-use IP Toolbench interface to configure the MegaCore functions and testbench
- IP functional simulation models for use in Altera-supported VHDL and Verliog HDL simulators
- Support for OpenCore® Plus evaluation

Reference Design & Testbench

The PCI Express Compiler includes an endpoint testbench that incorporates a root port bus functional model (BFM) and an endpoint design example. The endpoint design example illustrates the application interface to the PCI Express MegaCore function and is delivered as clear-text source-code (VHDL and Verilog HDL), suitable for both simulation and synthesis, as well as OpenCore Plus evaluation of the MegaCore function in hardware. The root port BFM incorporates a driver and an IP functional simulation model of a root port. Figure 1 illustrates the endpoint testbench setup.

Figure 1. Endpoint Testbench
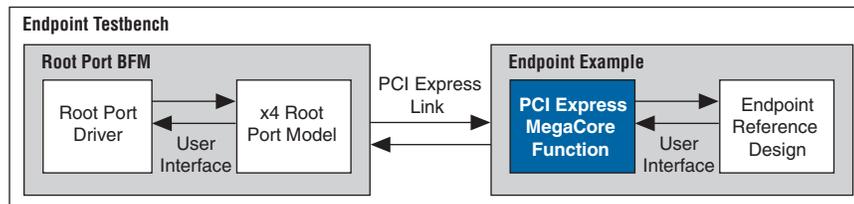
The root port driver provides preset transaction lists to set up the endpoint configuration registers, exercise target endpoint memory, and start the endpoint direct memory access (DMA). The endpoint design example is used as a target memory for read and write transactions from PCI Express, and as a DMA for read and write requests to PCI Express. The endpoint design example supports up to 2 VCs.

Hardware Testing

The PCI Express x4 MegaCore function has undergone significant hardware testing to ensure a reliable solution. The core was tested at the *PCI-SIG PCI Express Compliance Workshop* in February 2005, with high-quality results, including 100% of the Gold Tests, and 22 of 23 (96%) Interoperability Tests. Table 1 lists the products used in these tests.

Table 1. Hardware Interoperability Testing

Type	Vendor	Products
Motherboard	Intel	Lakeport/ICH7, SE7525RP2, Harwich
	Hewlett-Packard	HP Workstation xw9300, uATX–Commercial Desktop, ATX Commercial Desktop–ATI chipset, Server I, SFF–Commercial Desktop
	nVidia	NFORCE'04-2, C19
	Tyan	Thunder K8WE (S2895), Thunder K8SRE (S2891)
	VIA	PT880Pro, VT8251
Test Equipment	Catalyst	PCI Express SPX16A, SPX16E, SPX-4B
	Finisar	Doctor PCI Express Analyzer
	LeCroy	PETrainer, SDA6000A
	Wavecrest	SIA 3600
	Allion	Allion Physical Test
Bridge or Switch	PLX	PEX8114 PCI-X Bridge, PEX8516 16-Lane/4-Port Switch, PEX8111 PCI Bridge

For additional information on Altera products, visit www.altera.com. For updated information on Altera's PCI Express solutions, visit www.altera.com/pciexpress.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com

I.S. EN ISO 9001