EFEC20 IP Core

DS-1034-1.2 Data Sheet

The Altera 20% Enhanced Forward Error Correction (EFEC20) IP core includes a high-performance encoder and decoder for Optical Transport Network (OTN) FEC applications. Bose-Chaudhuri-Hocquenghem (BCH) streaming turbo product codes correct errors in data transmitted across communication channels with various bit error rates (BERs). EFEC20 performs high-gain error correction with 20% overhead and is available for 100 gigabits per second (Gbps)/Optical Channel Transport Unit (OTU)4 data transmission.

Features

EFEC20 includes the following features:

- High-performance encoder and decoder for error detection and correction
- 100 Gbps OTN rate with 640 bit datapath width
- 20% overhead for Stratix® IV and Stratix V devices
- Latency of < 32 µs
- Net electrical coding gain (NECG) of > 10.3 dB
- Error statistic monitoring, including the following types:
  - Corrected zeros and ones errors
  - Corrected errors and uncorrectable errors
  - 100 Gbps/OTU4 frame count

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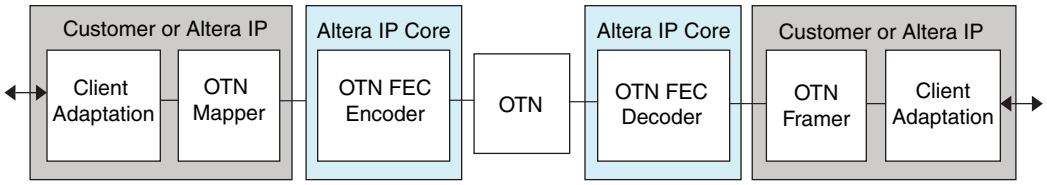
Architecture

Figure 1 illustrates the system architecture of the EFEC20 IP core. Data from an incoming client is adapted to OTN before it is written to the OTN mapper. The data is encoded with redundant data at the FEC encoder before it is transmitted across the network. The redundant data is decoded at the FEC decoder and identified errors are corrected before the data is written to the OTN framer. The data is then adapted back to the original client.

Figure 1. EFEC20 System Architecture



Device Family Support

Table 1 defines the device support levels for Altera IP cores.

Table 1. Altera IP Core Device Support Levels

FPGA Device Families	HardCopy® Device Families
Preliminary support—The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.	**HardCopy Companion**—The IP core is verified with preliminary timing models for the HardCopy companion device. The IP core meets all functional requirements, but might still be undergoing timing analysis for the HardCopy device family. It can be used in production designs with caution.
Final support—The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.	**HardCopy Compilation**—The IP core is verified with final timing models for the HardCopy device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 2 lists the level of support for EFEC20 in each of the Altera device families.

Table 2. Device Family Support

Device Family	Support
Stratix IV GT	Final
Stratix IV E/GX	Preliminary
Stratix V E/GX/GS/GT	Preliminary
All other device families	Not available

IP Core Verification

Before releasing a version of the EFEC20 IP core, Altera runs comprehensive regression tests to verify its quality and correctness.

Performance and Resource Utilization

Stratix IV devices use combinational adaptive look-up tables (ALUTs) and logic registers. Table 3 shows the typical performance for 100 Gbps EFEC20 on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus® II software.

Table 3. Performance - EFEC20 on Stratix IV GT *(1)*

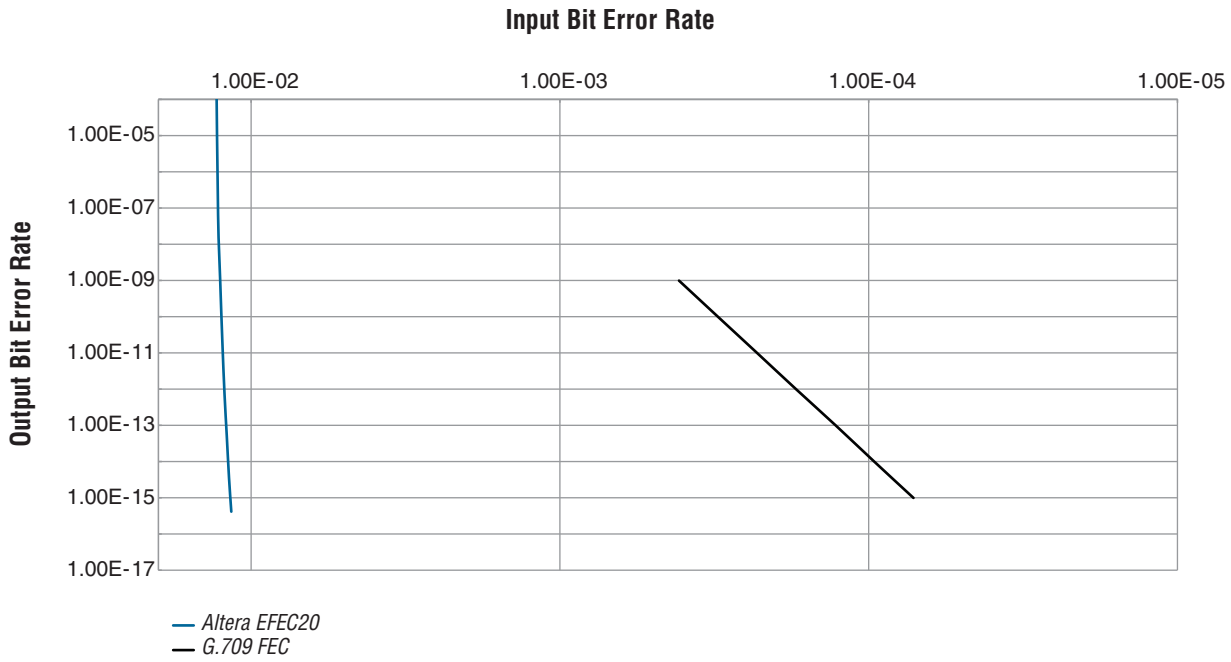
Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	—	—	—	—	—	> 10.3 dB	< 32 µs
Decoder	—	—	—	—	—		

Note to Table 3:

(1) Please contact Altera's OTN account manager at otn_info@altera.com for detailed performance information.

Figure 2 shows the Input BER and Output BER of the EFEC20 in comparison to the International Telecommunication Union, Telecommunication Standardization Sector (ITU-T) G.709 standardized FEC application.

Figure 2. EFEC20 Bit Error Rate



Port Listing

Table 4 lists the encoder input and output ports for connecting to the EFEC20 IP core.

Table 4. Encoder I/O Port Listing

I/O	Port	Port Width (Bits)	Description
Input	sys_clk	1	Clock port.
Input	i_rst	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.
Input	i_enable_n	1	Enable encoder and decoder port. This is a synchronous signal and is active low.
Input	i_max_column_width	8	This input signals the OTN column count to adjust for the various OTN overhead rates supported by this application.
Input	i_row	2	Input OTN frame row port. This is a synchronous signal.
Input	i_col	8	Input OTN frame column port. This is a synchronous signal.
Input	i_data_en	1	Input enable data port. This is a synchronous signal and is active high.
Input	i_data	640	Input data port.
Output	o_row	2	Output OTN frame row port. This is a synchronous signal.
Output	o_col	8	Output OTN frame column port. This is a synchronous signal.
Output	o_data_en	1	Output enable data port. This is a synchronous signal and is active high.
Output	o_data	640	Output data port.

Table 5 lists the decoder input ports and output ports for connecting to the EFEC20 IP core.

Table 5. Decoder I/O Port Listing (Part 1 of 2)

I/O	Port	Port Width (Bits)	Description
Input	sys_clk	1	Clock port.
Input	i_rst	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.
Input	i_enable_n	1	Enable encoder and decoder port. This is a synchronous signal and is active low.
Input	i_max_column_width	8	This input signals the OTN column count to adjust for the various OTN overhead rates supported by this application.
Input	i_error_scrambler_en_n	1	This input enables error scrambling. This is a synchronous signal and is active low.

Table 5. Decoder I/O Port Listing (Part 2 of 2)

I/O	Port	Port Width (Bits)	Description
Input	i_row	2	Input OTN frame row port. This is a synchronous signal.
Input	i_col	8	Input OTN frame column port. This is a synchronous signal.
Input	i_data_en	1	Input enable data port. This is a synchronous signal and is active high.
Input	i_data	640	Input data port.
Input	i_latch_counters	1	This input controls performance latch counters. The input latch counter pulses to receive the value count from one latch to the next latch. This is a synchronous signal and is active high.
Output	o_0s_fec_errors	32	This output signals the number of zeros errors within the performance interval controlled by i_latch_counters. This is a synchronous signal.
Output	o_1s_fec_errors	32	This output signals the number of ones errors within the performance interval controlled by i_latch_counters. This is a synchronous signal.
Output	o_fec_errors	32	This output signals the total number of errors within the performance interval controlled by i_latch_counters. This is a synchronous signal.
Output	o_uncorrectables	32	This output signals the number of uncorrectable RS codes. It is controlled by i_latch_counters
Output	o_otu4_frames	32	Output OTU4 frames port. This is a synchronous signal and is controlled by i_latch_counters.
Output	o_row	2	Output OTN frame row port. This is a synchronous signal.
Output	o_col	8	Output OTN frame column port. This is a synchronous signal.
Output	o_data_en	1	Output enable data port. This is a synchronous signal and is active high.
Output	o_data	640	Output data port.

Document Revision History

Table 6 shows the revision history for this document.

Table 6. Document Revision History

Date	Version	Changes
May 2012	1.2	Added otn_info@altera.com mailbox.
March 2012	1.1	Updated NECG.
February 2012	1.0	Initial release.