2D-FEC IP Core

The Altera Two-Dimensional Enhanced Forward Error Correction (2D-FEC) IP Core comprises a high-performance encoder and decoder for Optical Transport Network (OTN) FEC applications. 2D-FEC is a product code comprised of two Bose-Chaudhuri-Hocquenghem (BCH) codes for iterative decoding of transmitted data. The decoding algorithm provides error correction while eliminating the detection of false errors in the OTN frame. 2D-FEC performs high-gain FEC with 7% overhead for transmission at 40 gigabits per second (Gbps)/Optical Channel Transport Unit (OTU)3.

Features

2D-FEC includes the following features:

- High-performance encoder and decoder for error detection and correction
- 40 Gbps OTN rate with 256 bit datapath width
- 7% overhead for Stratix® IV and Stratix V devices
- Latency of 60 µs
- Net electrical coding gain (NECG) of > 9.3 dB
- Error statistic monitoring, including the following types:
  - Corrected zeros and ones errors
  - Corrected errors and uncorrectable errors
  - 40 Gbps/OTU3 frame count

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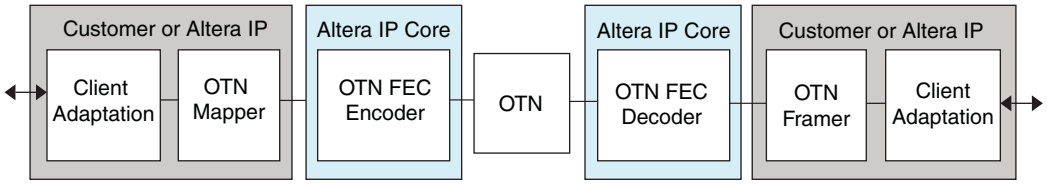
Architecture

Figure 1 illustrates the system architecture of the 2D-FEC IP core. Data from an incoming client is adapted to OTN before it is written to the OTN mapper. The data is encoded with redundant data at the FEC encoder before it is transmitted across the network. The redundant data is decoded at the FEC decoder and identified errors are corrected before the data is written to the OTN framer. The data is then adapted back to the original client.

Figure 1. 2D-FEC System Architecture



Device Family Support

Table 1 defines the device support levels for Altera IP cores.

Table 1. Altera IP Core Device Support Levels

FPGA Device Families	HardCopy® Device Families
Preliminary support—The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.	**HardCopy Companion**—The IP core is verified with preliminary timing models for the HardCopy companion device. The IP core meets all functional requirements, but might still be undergoing timing analysis for the HardCopy device family. It can be used in production designs with caution.
Final support—The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.	**HardCopy Compilation**—The IP core is verified with final timing models for the HardCopy device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 2 lists the level of support for 2D-FEC in each of the Altera device families.

Table 2. Device Family Support

Device Family	Support
Stratix IV GT	Final
Stratix IV E/GX	Preliminary
Stratix V E/GX/GS/GT	Preliminary
All other device families	Not available

IP Core Verification

Before releasing a version of the 2D-FEC IP core, Altera runs comprehensive regression tests to verify its quality and correctness.

Performance and Resource Utilization

Stratix IV devices use combinational adaptive look-up tables (ALUTs) and logic registers. Table 3 shows the typical performance for 40 Gbps 2D-FEC on the Stratix IV GT (EP4S100G5H40I1(N)) device as reported by the Quartus® II software.

Table 3. Performance - 40 Gbps 2D-FEC on Stratix IV GT

Options	ALUTS	Logic Registers	Decoder Memory (M9K)	Memory (144K)	f_{MAX} (MHz)	Net Electrical Gain (NECG)	Latency
Encoder	7,219K	7,428	81 blocks	0 blocks	208	9.3 dB	60 µs
Decoder	67,585K	59,306	698 blocks	16 blocks	192		

Port Listing

Table 4 lists the encoder input and output ports for connecting to the 2D-FEC IP core.

Table 4. Encoder I/O Port Listing

I/O	Port	Port Width (Bits)	Description
Input	sys_clk	1	Clock port.
Input	rst	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.
Input	i_enable_n	1	Enable encoder and decoder port. This is a synchronous signal and is active low.
Input	i_row	2	Input OTN frame row port. This is a synchronous signal.
Input	i_col	7	Input OTN frame column port. This is a synchronous signal.
Input	i_data	256	Input data port.
Output	o_row	2	Output OTN frame row port. This is a synchronous signal.
Output	o_col	7	Output OTN frame column port. This is a synchronous signal.
Output	o_data	256	Output data port.

Table 5 lists the decoder input and output ports for connecting to the 2D-FEC IP core. All error counts are accumulated on a per-clock cycle basis.

Table 5. Decoder I/O Port Listing (Part 1 of 2)

I/O	Port	Port Width (Bits)	Description
Input	sys_clk	1	Clock port.
Input	rst	1	This reset port is expected to meet removal and recovery constraints for sys_clk. This is an asynchronous reset and is active high.

Table 5. Decoder I/O Port Listing (Part 2 of 2)

I/O	Port	Port Width (Bits)	Description
Input	i_enable_n	1	Enable encoder and decoder port. This is a synchronous signal and is active low.
Input	i_row	2	Input OTN frame row port. This is a synchronous signal.
Input	i_col	7	Input OTN frame column port. This is a synchronous signal.
Input	i_data	256	Input data port.
Output	o_uncorrectable_code_errors_valid	1	This output is the valid signal for o_uncorrectable_code_errors. This is a synchronous signal and is active high.
Output	o_uncorrectable_code_errors	1	This output signals the number of uncorrectable RS codes. This is a synchronous signal and is active high.
Output	o_correctable_code_errors_valid	1	This output is the valid signal for o_correctable_code_errors. This is a synchronous signal and is active high.
Output	o_correctable_code_errors	1	This output signals the number of correctable RS codes. This is a synchronous signal and is active high.
Output	o_ones_errors	9	This output signals the total number of corrected ones errors.
Output	o_odd_ones_errors	8	This output signals the number of corrected odd ones errors.
Output	o_even_ones_errors	8	This output signals the number of corrected even ones errors.
Output	o_zeros_errors	9	This output signals the total number of corrected zeros errors.
Output	o_odd_zeros_errors	8	This output signals the number of corrected odd zeros errors.
Output	o_even_zeros_errors	8	This output signals the number of corrected even zeros errors.
Output	o_errors_valid	1	This output is the valid signal for o_ones_errors, o_odd_ones_errors, o_even_ones_errors, o_zeros_errors, o_odd_zeros_errors, and o_even_zeros_errors. This is a synchronous signal and is active high.
Output	o_dec_locked	1	This output signals that the decoder has locked to the OTN datapath and valid error correction can occur. This is a synchronous signal and is active high.
Output	o_row	2	Output OTN frame row port. This is a synchronous signal.
Output	o_col	7	Output OTN frame column port. This is a synchronous signal.
Output	o_data	256	Output data port.

Document Revision History

Table 6 shows the revision history for this document.

Table 6. Document Revision History

Date	Version	Changes
February 2012	1.0	Initial release.