Motor Control IP Suite Components for Drive-on-Chip Reference Designs

The Altera® drive-on-chip reference designs include IP components required by multiple motor control applications. You can use the IP components with Altera reference designs or with your standalone motor control applications. This data sheet describes the following four components from Altera's motor control IP suite:

- Sigma-delta analog-to-digital converter (ADC) interface to sample and low-pass filter the ADC serial input. The interface includes: a decimating third-order sinc (sinc^3) filter in the FPGA; control loop filters with software selectable decimation factors; overcurrent detection filters with software selectable decimation factors; and clock synchronization
- Direct-current (DC)-link monitor and ballast control interface to monitor DC-link voltage
- 6-channel pulse-width modulation (PWM) interface to drive the transistors and generate a configurable timing output strobe to trigger ADC conversion/sinc^3 filter reset
- 5-state drive system monitor to act as an interlock between the state of the system and the requested operation

Qsys system integration tool component interfaces, including Avalon Memory-Mapped (Avalon-MM) interface signals and conduit signals, are provided for each IP component.

This data sheet describes the motor control IP suite components for drive-on-chip reference designs and includes the following sections:

- Resource Utilization
- Installing the IP Suite Components
- Functional Description
- Qsys Component Interfaces
- Register Descriptions
- Document Revision History

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Resource Utilization

Table 1 describes approximate logic cell utilization for the motor control IP suite components on Cyclone® IV (EP4CE55F23C7) and Cyclone V SoC devices; the exact utilization values are project dependant.

Table 1. IP Suite Component Resource Utilization

IP Suite Component	Cyclone IV Device Logic Cells	Cyclone V SoC Device ALUTs
Sigma-delta ADC interface	750	
DC-link and ballast control interface	450	
6-channel PWM interface	350	
Drive system monitor	100	

The motor control IP suite components for drive-on-chip reference designs do not require embedded memory or digital signal processing (DSP) resources.

Installing the IP Suite Components

The motor control IP suite components for drive-on-chip reference designs are available as a **.zip** archive. Once installed, the drive-on-chip components appear in the **Motor Control Suite** under the **Component Library** in Qsys. Each IP suite component has an individual directory within the **.zip** archive. The top level directory for each component includes a HDL subdirectory containing the ***_hw.tcl** file (where * refers to the IP component name) necessary for integration within Qsys. The HDL subdirectory also includes one or more plain-text Verilog HDL source files for the component.

Installing IP Suite Components in a Quartus® II Project

To use the motor control IP suite components in a single Altera Complete Design Suite project, unzip the IP component directories into a directory named "ip" within the Quartus II project. The Quartus II software automatically searches for components in the **ip** directory and makes them available in the component library.

Installing IP Suite Components in Multiple Quartus II Projects

To include the motor control IP suite components on a project-by-project basis, a **search_path.ipx** file is included as a project file. For each IP component, add a `<path> ... </path>` construct as follows:

```
<library>
  ...
 <path path="./../../components/ssg_emb_dsm/**/*" >
    <tag2 key="COMPONENT_IN_PROJECT" value="false" />
  </path>
...]
</library>
```

Installing IP Suite Components in All Quartus II Projects

To add the motor control IP suite components to all Quartus II software projects, use the IP Search Path feature. To open the IP Search Path, perform the following steps:

1. Open Qsys
2. Select **Tools**
3. Click on the **Options** menu
4. Select **IP Search Path** from the **Category** options
5. Click **Add** to open the IP Search Path
6. Browse the to directory where the IP Suite Components were unzipped, select and click **Open** and **Finish**

Functional Description

This section describes the functionality of the motor control IP suite components for Altera's drive-on-chip reference designs. Figure 1 shows a simplified system block diagram of the motor control IP suite components within an FPGA.

Figure 1. Motor Control IP Suite Components on FPGAs

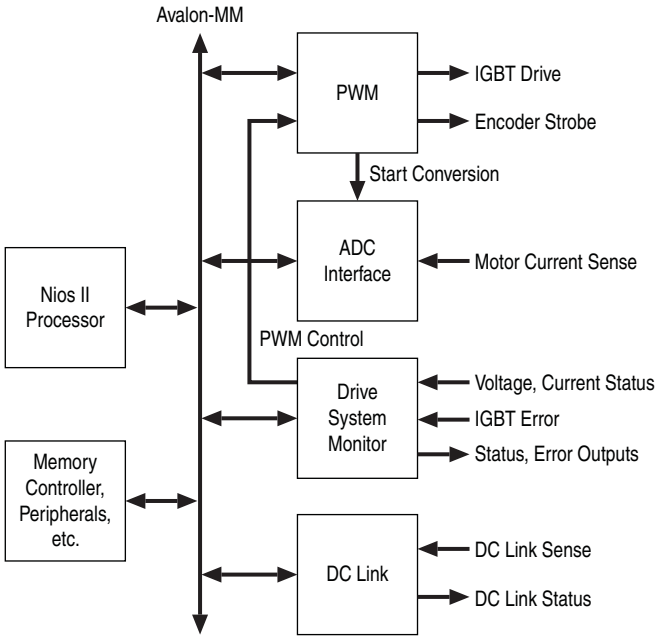
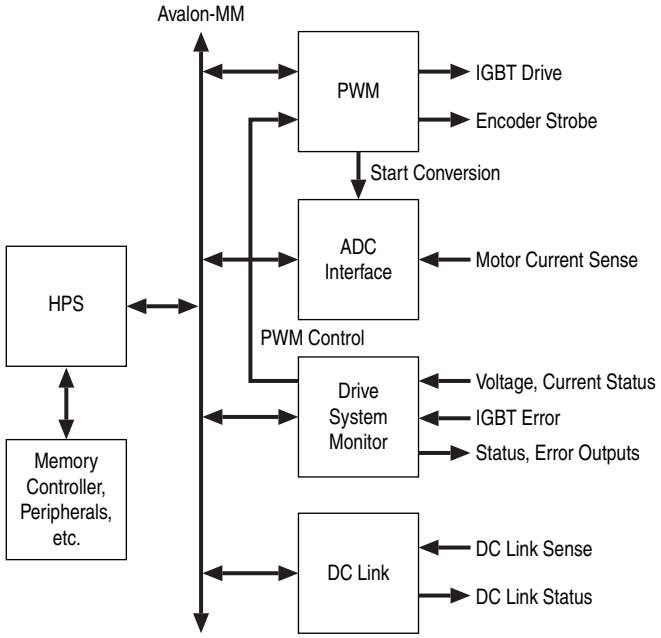


Figure 1 shows a simplified system block diagram of the motor control IP suite components within an SoC.

Figure 2. Motor Control IP Suite Components on SoCs



Sigma-Delta ADC Interface

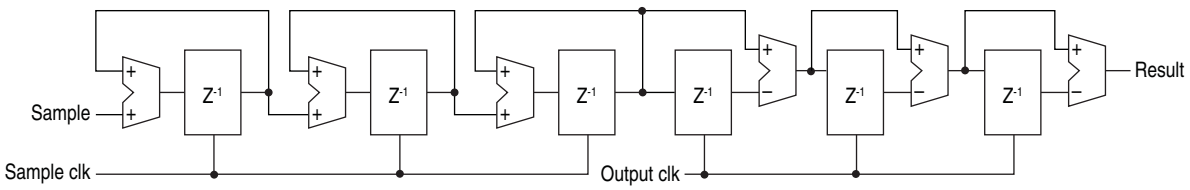
The sigma-delta ADC interface samples the 20-MHz 1-bit ADC serial input. A decimating sinc^3 filter in the FPGA then low-pass filters the serial input. The sinc^3 filter does not require hardware multipliers.

For register information, refer to "Sigma-Delta ADC Interface Control and Status Registers (1)" on page 12.

Sinc^3 Filter

Figure 3 shows the architecture of the sinc^3 filter. The input samples pass through three integrator stages before they are decimated by a factor *M*. Every *M*th sample is reserved and *M-1* samples are discarded. These reserved samples are passed through three differentiators to produce a final output value.

Figure 3. Sinc^3 Filter Topology with Decimation Factor *M*



The pulse-width modulation (PWM) block triggers ADC conversion with a reset signal that resets the filters and control logic. The direct-current gain of the sinc^3 filter is calculated as $Gain_{DC} = M^K$ *(where K = 3 for sinc^3)*. To account for word growth in the filter stages, the internal bus width of the filters is calculated as *Internal bus width = 1 + $Klog_2M$.* The output data rate for an input sample rate f_S and decimation factor M is calculated as *Data rate = f_S/M.*

The sinc^3 filter requires a time period 3× longer than the time period of the output data rate to settle. When the settling time is satisfied and the ADC conversion is complete, an interrupt is signalled to the processor. The performance of N-bit ADC is calculated as *SNR = 6.02N + 1.76dB*, where SNR is the signal to noise ratio; if additional noise is present in the system the performance value is affected. The effective number of bits (ENOB) is calculated as *ENOB = (SINAD - 1.76dB)/6.02*, where SINAD is the signal to noise and distortion. SNR, SINAD, and ENOB are determined by decimation ratio.

Table 2 describes the sinc^3 filter where f_S equals 20 MHz.

Table 2. Sinc^3 Filter: f_S = 20 MHz

Decimation (*M*)	$Gain_{DC}$	Word Size	Bus Width	Data Rate (kHz)	Settling Time (µs)	ENOB
8	512	9	10	2500.0	1.2	6.4
16	4096	12	13	1250.0	2.4	8.9
64	262,144	18	19	312.5	9.6	13.9
128	2,097,152	21	22	156.2	19.2	16.4

Filters

There are two separate filter paths; a control loop filter path and an overcurrent detection filter path.

The control loop filters are slower but more accurate than the overcurrent detection filters with a software selectable decimation factor of *M=128* or *M=64*. The control loop filters have an offset correction feature for zero-offset correction. The filter output is a signed 16 bit (2's complement) format.

The overcurrent detection filters are faster but less accurate than the control loop filters with a software selectable decimation factor of *M=16* or *M=8*. A software configurable overcurrent output provides a direct output to disable the motor when under hardware control.

The control loop and overcurrent detection filters use the same control bit for decimation selection. The possible selections are *control loop M=128, overcurrent M=16*, and *control loop M=64, overcurrent M=8*.

Clocking

Synchronization between the ADC clock and the FPGA system clock is performed at the output stage before data is registered in the Avalon-MM interface slave registers.

The external ADC components require a clock to be sourced from the FPGA and return samples synchronous to the FPGA-sourced clock. The clock within the FPGA drives the ADC filters.

Appropriate timing constraints must be applied in the Quartus II software project to guarantee correct sampling of the ADC interface data. The sampling must be based on the clock to output specification of the chosen ADC.

Offset Adjustment for Sigma-Delta ADC Interface

Table 3 describes typical characteristics of a sigma-delta ADC and the demodulated output of the sinc^3 filter. The output code is a positive value.

Table 3. Sigma-Delta ADC Offset Adjustment Characteristics

Analog Input	Voltage Input	Density of 1s	Demodulated ADC Code (16 bit)
Full-scale range	640 millivolts (mV)	—	—
+ Full-scale range	+ 320 mV	100%	65,535
+ Recommended input range	+ 200 mV	81.25%	53,248
Zero	0 mV	50%	32,768
- Recommended input range	- 200 mV	18.75%	12,288
- Full-scale range	- 320 mV	0%	0

Offset values are added to demodulator results to represent the bipolar input signal and to allow for zero-offset adjustment. The offset values are specified in the `offset_u` or `offset_w` registers.

During normal operation, the offset value is set to 32,768, or 50% of the full-scale range, to bring the demodulated result into the range of -32,768 to +32,767. The offset value is adjusted to correct for zero-offset errors during calibration.

DC-Link Monitor

The DC-link monitor uses an instance of the sinc^3 filter module, similar to the instance used by the sigma-delta interface, to monitor the DC-link voltage. The software configurable reference values are compared with the filtered DC-link voltage value to determine if the DC-link voltage is within the expected range. Status outputs are used to signal overvoltage and undervoltage conditions to external protection circuitry or to activate an external chopper (brake) circuit.

"DC-Link Monitor Control and Status Registers (1)" on page 13 describes the DC-link monitor control and status registers.

ADC Interface Result

The demodulated result of the DC-link monitor is restricted to a positive value because the DC-link voltage cannot be negative. Any negative result after applying the offset correction is clipped to zero.

Offset Adjustment for DC-Link Monitor

Offset values are added to demodulator results to represent the bipolar input signal and to allow for zero-offset adjustment. The offset values are specified in the `Offset` register.

During normal operation, the offset value is set to 16,384 and has double the weighting of the offset value of the ADC interface. The offset value is adjusted to correct for zero-offset errors during calibration.

6-Channel PWM Interface

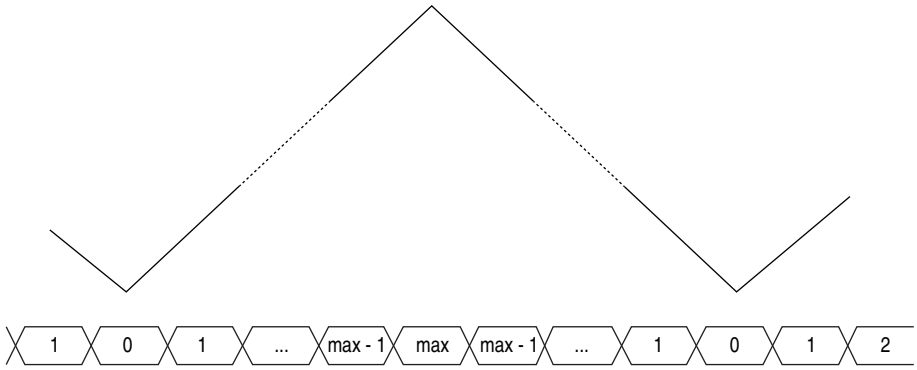
The 6-channel PWM interface operates as three pairs of outputs, with each pair operating differentially to drive the upper and lower power transistors in a half-bridge power stage. The PWM interface ensures a dead time between switching to ensure both outputs are not high at the same time; the dead time prevents short circuit "shoot-through" in the power transistors.

The input clock and a PWM counter set the PWM frequency. The counter alternately ramps up from zero to a maximum value and ramps down from the maximum value to zero. The sequence is as follows:

```
0, 1, 2, … max - 1, max, max - 1, … 2, 1, 0, …
```

Figure 4 shows the PWM counter value changes.

Figure 4. PWM Counter Value



The maximum value of the counter ramp, `max`, is software configurable. The PWM frequency is calculated as $f_{PWM} = f_{CLK}/(2 \times max)$

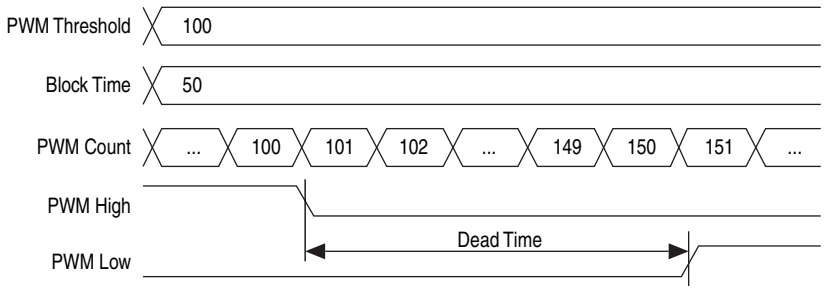
The 16-bit counter resolution with a 50-MHz system clock is sufficient to generate an 8-kHz PWM output. The high- and low-side drive signals for the insulated gate bipolar transistor (IGBT) module are generated by comparing the ramp counter value with the values set in the PWM threshold configuration registers. A dead period is inserted between the switching of the upper and lower drive signals according to the value set in the PWM blocking time configuration register.

The `carrier_latch` output signal is set high for one clock cycle when the PWM counter is at 0 or max. This signal is used as a position encoder to take a position reading.

The `start` output signal is a trigger for the ADC IP to start conversion. The `trigger_up` configuration register sets the PWM count value and the `start` signal is set high for one clock cycle while the PWM is counting up. The `trigger_down` configuration register sets the PWM count value and the `start` signal is set high for one clock cycle while the PWM is counting down. The `trigger_up` and `trigger_down` registers must be set symmetrically to ensure a regular ADC sample position offset prior to the reversal point of the counter. In other words, `trigger_up` = MAX - offset, and `trigger_down` = offset.

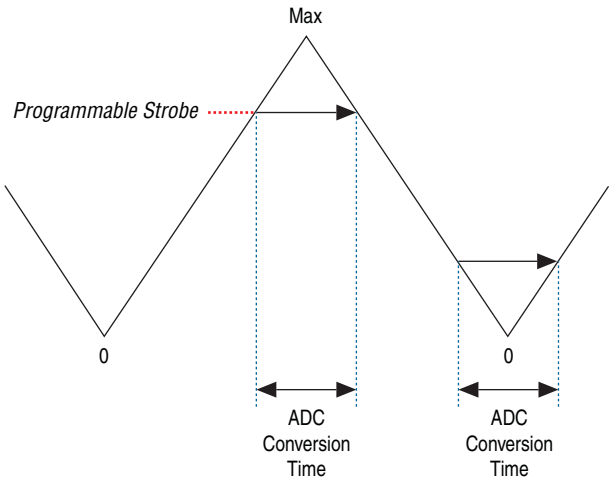
The PWM blocking time configuration register is calculated as *pwm_block = dead time x* f_{CLK}. Dead time refers to the time when both upper and lower IGBTs must be turned off to prevent short circuits; you must obtain specific dead time values from the documentation for the specific IGBT module you are using. For example, with a dead time requirement of 2µs, the `pwm_block` value is calculated as *2µs x 50 MHz*. Figure 5 shows PWM output generation (including dead time).

Figure 5. PWM Output Generation (Including Dead Time)



Based on the PWM counter value, the PWM component generates configurable timing output strobes for triggering ADC conversion for feedback-current readings. You must configure the ADC start pulse to perform the conversion during the quietest period of the PWM cycle, in other words, around the *min* and *max* values of the PWM counter. Figure 6 shows the configurable timing output strobes.

Figure 6. Configurable Timing Output Strobes



"6-Channel PWM Control and Status Registers (1)" on page 15 describes the 6-channel PWM interface control and status registers, including various timing features.

Drive System Monitor

The drive system monitor acts as an interlock between the state of the system and the requested operation. Application software writes to the drive system monitor to request a change of state. The hardware may accept or decline the change of state request, depending on the system status (for example, overvoltage status, undervoltage status, and current measurements alter the system status). A subsequent read from the `Status` register verifies if the change of state was accepted. Table 4 describes the five drive states of the drive system monitor.

Table 4. Drive States of the Drive System Monitor

State	Name	System State
0	Init	The initial drive state. In this state, the PWM is enabled.
1	Pre-charge	In this state, the PWM and lower IGBT are enabled.
2	Pre-Run	In this state, the error inputs are monitored.
3	Run	In this state, the PWM and upper and lower IGBTs are enabled.
4	Error	In this state, the PWM is disabled.

The drive system monitor latches status signals from the system so the signals are available as status register bits and direct outputs. For example, the direct outputs can be used to drive status LEDs.

"Drive System Monitor Control and Status Registers (1)" on page 16 describes the drive system monitor control and status registers.

Qsys Component Interfaces

Each of the four IP components is packaged as Qsys components with Avalon-MM interface signals and conduit signals.

Table 5 describes the Qsys component interfaces for the sigma-delta ADC interface.

Table 5. Sigma-Delta ADC Interface Signals (Part 1 of 2)

Signal Name	Direction	Description
Avalon-MM Interface Signals		
`clk`	Input	The FPGA system clock input signal.
`clk_adc`	Input	The ADC clock input signal.
`reset_n`	Input	The system reset signal. `reset_n` is active low.
`avs_read_n`	Input	The Avalon-MM read strobe signal. `avs_read_n` is active low.
`avs_write_n`	Input	The Avalon-MM write strobe signal. `avs_write_n` is active low.
`avs_address[3:0]`	Input	The Avalon-MM address signal.

Table 5. Sigma-Delta ADC Interface Signals (Part 2 of 2)

Signal Name	Direction	Description
avs_writedata[31:0]	Input	The Avalon-MM write data signal.
avs_readdata[31:0]	Output	The Avalon-MM read data signal.
avs_irq	Output	The conversion complete interrupt signal.
Conduit Signals		
start	Input	The filter reset (start conversion) signal.
sync_dat_u	Input	The sigma-delta bit stream signal for phase U.
sync_dat_w	Input	The sigma-delta bit stream signal for phase V.
overcurrent	Output	The overcurrent status signal.

Table 6 describes the Qsys component interfaces for the DC-Link Monitor.

Table 6. DC-Link Monitor Signals

Signal Name	Direction	Description
Avalon-MM Interface Signals		
clk	Input	The FPGA system clock input signal.
clk_adc	Input	The ADC clock input signal.
reset_n	Input	The system reset signal. reset_n is active low.
avs_read_n	Input	The Avalon-MM read strobe signal. avs_read_n is active low.
avs_write_n	Input	The Avalon-MM write strobe signal. avs_write_n is active low.
avs_address[3:0]	Input	The Avalon-MM address signal.
avs_writedata[31:0]	Input	The Avalon-MM write data signal.
avs_readdata[31:0]	Output	The Avalon-MM read data signal.
Conduit Signals		
sync_dat	Input	The sigma-delta ADC bit stream signal.
dc_link_enable	Input	The chopper IGBT enable signal.
overvoltage	Output	The overvoltage status signal.
undervoltage	Output	The undervoltage status signal.
chopper	Output	The gate signal for chopper.

Table 7 describes the Qsys component interfaces for the 6-channel PWM interface.

Table 7. 6-Channel PWM Interface Signals (Part 1 of 2)

Signal Name	Direction	Description
Avalon-MM Interface Signals		
clk	Input	The FPGA system clock input signal.
reset_n	Input	The system reset signal. reset_n is active low.
avs_read_n	Input	The Avalon-MM read strobe signal. avs_read_n is active low.

Table 7. 6-Channel PWM Interface Signals (Part 2 of 2)

Signal Name	Direction	Description
avs_write_n	Input	The Avalon-MM write strobe signal. avs_write_n is active low.
avs_address[3:0]	Input	The Avalon-MM address signal.
avs_writedata[31:0]	Input	The Avalon-MM write data signal.
avs_readdata[31:0]	Output	The Avalon-MM read data signal.
Conduit Signals		
pwm_enable	Input	The PWM enable signal.
en_upper	Input	The upper IGBT enable signal.
en_lower	Input	The lower IGBT enable signal.
u_h	Output	The upper IGBT gate signal for phase U.
u_l	Output	The lower IGBT gate signal for phase U.
v_h	Output	The upper IGBT gate signal for phase V.
v_l	Output	The lower IGBT gate signal for phase v.
w_h	Output	The upper IGBT gate signal for phase W.
w_l	Output	The lower IGBT gate signal for phase W.
carrier_latch	Output	The latch signal for the position encoder.
start	Output	The start conversion pulse to ADC signal.
carrier[15:0]	Output	The PWM counter value signal.

The BiSS Interface website (http://www.biss-interface.com) has complete details on BiSS technology.

Table 8 describes the Qsys component interfaces for the drive system monitor.

Table 8. Drive System Monitor Signals (Part 1 of 2)

Signal Name	Direction	Description
Avalon-MM Interface Signals		
csi_clk	Input	The FPGA system clock input signal.
csi_reset_n	Input	The system reset signal. csi_reset_n is active low.
avs_read_n	Input	The Avalon-MM read strobe signal. avs_read_n is active low.
avs_write_n	Input	The Avalon-MM write strobe signal. avs_write_n is active low.
avs_address	Input	The Avalon-MM address signal.
avs_writedata[31:0]	Input	The Avalon-MM write data signal.
avs_readdata[31:0]	Output	The Avalon-MM read data signal.
Conduit Signals		
overcurrent	Input	The overcurrent status signal.
overvoltage	Input	The overvoltage status signal.
undervoltage	Input	The undervoltage status signal.

Table 8. Drive System Monitor Signals (Part 2 of 2)

Signal Name	Direction	Description
chopper	Input	The gate signal for chopper.
dc_link_clk_err	Input	The DC-link monitor clock error signal.
igbt_err	Input	The IGBT error signal.
error_out	Output	The output error signal.
overcurrent_latch	Output	The latched version of overcurrent.
overvoltage_latch	Output	The latched version of overvoltage.
undervoltage_latch	Output	The latched version of undervoltage.
dc_link_clk_err_latch	Output	The latched version of dc_link_clk_err.
igbt_err_latch	Output	The latched version of igbt_err.
chopper_latch	Output	The latched version of chopper.
pwm_control[2:0]	Output	The PWM control signal.

Register Descriptions

This section describes the IP component registers.

Table 9 describes the sigma-delta analog-to-digital converter (ADC) interface control and status registers.

Table 9. Sigma-Delta ADC Interface Control and Status Registers (1) (Part 1 of 2)

Address	Name	Bit(s)	Description	HW Reset Value	Access
0x00	–	–	Reserved.	–	–
0x04	offset_u	[31:16]	Reserved.	–	–
		[15:0]	The offset adjustment for zero balance of sinc^3 filter output for phase U. A value of 32,768 corresponds to a 0-mV offset.	0x0	RW
0x08	offset_w	[31:16]	Reserved.	–	–
		[15:0]	The offset adjustment for zero balance of sinc^3 filter output for phase W. A value of 32,768 corresponds to a 0-mV offset.	0x0	RW
0x0C	i_peak	[31:10]	Reserved.	–	–
		[9:0]	The overcurrent detection threshold register for the overcurrent output. This is a read/write register.	0x0	RW

Table 9. Sigma-Delta ADC Interface Control and Status Registers (1) (Part 2 of 2)

Address	Name	Bit(s)	Description	HW Reset Value	Access
0x10	d	[31:3]	Reserved.	–	–
		[2]	The control register: when DEC_RATE is set to 0, the sinc^3 decimation rate is M=128 for the control loop filter and M=16 for the overcurrent-detection filter; when DEC_RATE is set to 1, the sinc^3 decimation rate isM=64 for the control loop filter and M=8 for the overcurrent-detection filter.	0x0	RW
		[1]	The control register; OVERCURRENT_EN is the enable bit for overcurrent protection.	0x0	RW
		[0]	The control register; OVERVOLT_EN is the enable bit for overvoltage protection.	0x0	RW
0x14	irq_ack	[31:1]	Reserved.	–	–
		[0]	The interrupt request (IRQ) acknowledge register. Write “1” followed by “0” to clear the interrupt request.	0x0	W
0x18	status	[31:5]	Reserved.	–	–
		[4]	The status register; IRQ_L is the IRQ active for low resolution converter channel.	0x0	R
		[3]	The status register; IRQ_H is the IRQ active for high resolution converter channel.	0x0	R
		[2]	The status register; OC_U is the overcurrent status for phase U.	0x0	R
		[1]	The status register; OC_W is the overcurrent status for phase W.	0x0	R
		[0]	The status register; OC is the logical OR of OC_W and OC_U.	0x0	R
0x1C	i_u	[31:16]	Reserved.	–	–
		[15:0]	The current in register for phase U.	0x0	R
0x20	i_w	[31:16]	0. These bits are written as zero and read as zero.	–	–
		[15:0]	The current in register for phase W.	0x0	R
0x24	i_peak	[31:10]	0. These bits are written as zero and read as zero.	–	–
		[9:0]	The overcurrent detection threshold register. This is a read-only register.	0x0	R

Note to Table 9:

(1) Reserved bits must be written as “0” and are read as zero.

Table 10 describes the DC-link monitor control and status registers.

Table 10. DC-Link Monitor Control and Status Registers (1) (Part 1 of 2)

Address	Name	Bit(s)	Description	HW Reset Value	Access
0x00	–	–	Reserved.	–	–

Table 10. DC-Link Monitor Control and Status Registers (1) (Part 2 of 2)

Address	Name	Bit(s)	Description	HW Reset Value	Access
0x04	offset	[31:16]	Reserved.	–	–
		[15:0]	The offset adjustment register for zero balance of $sinc^3$ filter output. A value of 16,384 corresponds to a 0-mV offset.	0x0	RW
0x08	k_64	[31:1]	Reserved.	–	–
		[0]	The $sinc^3$ filter decimation rate register. When set to 0, the $sinc^3$ decimation rate is M=64; when set to 1, the $sinc^3$ decimation rate is M=128.	0x0	RW
0x0C	ref_disable	[31:16]	Reserved.	–	–
		[15:0]	The DC-link voltage disable level register. This register provides the maximum allowable voltage for link voltage. If the maximum value is exceeded the overvoltage output is driven, to shut down the system.	0x0	RW
0x10	link_ref	[31:16]	Reserved.	–	–
		[15:0]	The DC-link chopper voltage level register.This register provides the threshold voltage for chopper operation. The chopper IGBT transistor is turned on when the DC-link voltage exceeds this value.	0x0	RW
0x14	bottom_ref	[31:16]	Reserved.	–	–
		[15:0]	The DC-link undervoltage reference level register. This register provides the minimum allowable value for link voltage. If the link voltage falls below the reference level the undervoltage output is driven.	0x0	RW
0x18	brake_t	[31:11]	Reserved.	–	–
		[10:0]	The thermal time constant of brake resistor register. This register is not used.	0x0	RW
0x1C	brake_max_level	[31:16]	Reserved.	–	–
		[15:0]	The brake resistor maximum I^2T value register. This register is not used.	0x0	RW
0x20	dc_link	[31:16]	0. These bits are written as zero and read as zero.	–	–
		[15:0]	The current link voltage register.	0x0	R
0x24	brake_level	[31:16]	0. These bits are written as zero and read as zero.	–	–
		[15:0]	The current brake resistor I^2T value register. This register is not used.	0x0	R
0x28	status	[31:3]	0. These bits are written as zero and read as zero.	–	–
		[2]	The voltage and chopper status register; OVER is the DC-link overvoltage status bit.	0x0	R
		[1]	The voltage and chopper status register; UNDER is the DC-link undervoltage status bit.	0x0	R
		[0]	The voltage and chopper status register; CHOPPER is the status of the gate signal to chopper.	0x0	R

Note to Table 10:

(1) Reserved bits must be written as zero and are read as zero.

Table 11 describes the 6-channel PWM interface control and status registers.

Table 11. 6-Channel PWM Control and Status Registers (1)

Address	Name	Bit(s)	Description	HW Reset Value	Access
0x00	–	–	Reserved.	–	–
0x04	pwm_u	[31:15]	Reserved.	–	–
		[14:0]	The PWM threshold register for switching phase U.	0x0	RW
0x08	pwm_v	[31:15]	Reserved.	–	–
		[14:0]	The PWM threshold register for switching phase V.	0x0	RW
0x0C	pwm_w	[31:15]	Reserved.	–	–
		[14:0]	The PWM threshold register for switching phase W.	0x0	RW
0x10	max	[31:15]	Reserved.	–	–
		[14:0]	The PWM counter maximum value. This register sets the PWM carrier frequency.	0x0	RW
0x14	block	[31:8]	Reserved.	–	–
		[7:0]	The PWM blocking time register.	0x0	RW
0x18	trigger_up	[31:15]	Reserved.	–	–
		[14:0]	The PWM count value for the ADC trigger when the PWM counter is incrementing.	0x0	RW
0x1C	trigger_down	[31:15]	Reserved.	–	–
		[14:0]	The PWM count value for the ADC trigger when the PWM counter is decrementing.	0x0	RW
0x20	gate	[31:6]	0. These bits are written as zero and read as zero.	–	–
		[5]	The insulated gate bipolar transistor (IGBT) register; U_L is the lower transistor gate signal for phase U.	0x0	R
		[4]	The IGBT gate register; U_H is the upper transistor gate signal for phase U.	0x0	R
		[3]	The IGBT gate register; V_L is the lower transistor gate signal for phase V.	0x0	R
		[2]	The IGBT gate register; V_H is the upper transistor gate signal for phase V.	0x0	R
		[1]	The IGBT gate register; W_L is the lower transistor gate signal for phase W.	0x0	R
		[0]	The IGBT gate register; W_H is the upper transistor gate signal for phase W.	0x0	R
0x28	carrier	[31:17]	0. These bits are written as zero and read as zero.	–	–
		[16:0]	The current PWM count value register.	0x0	R

Note to Table 11:

(1) Reserved bits must be written as zero and are read as zero.

Table 12 describes the drive system monitor control and status registers.

Table 12. Drive System Monitor Control and Status Registers *(1)*

Address	Name	Bit(s)	Description	HW Reset Value	Access
0x00	control	[31:3]	Reserved.	–	–
		[2:0]	The control register. Write to this register to request a change of state in the drive system monitor.	0x0	RW
0x04	status *(2)*	[31:12]	These bits are written as zero and read as zero.	–	–
		[11:9]	The current drive system monitor state bits. "Drive States of the Drive System Monitor" on page 9 describes the five drive states.	0x0	R
		[8]	PWM control; bit 8 is upper IGBT enable.	0x0	R
		[7]	PWM control; bit 7 is lower IGBT enable.	0x0	R
		[6]	PWM control; bit 6 is PWM enable.	0x0	R
		[5]	Reserved.	–	–
		[4]	The IGBT error bit; reflects the state of the IGBT error input.	0x0	R/W1C
		[3]	The DC-link to ADC clock status bit; reflects the state of the dc_link_clk_err input signal.	0x0	R/W1C
		[2]	The undervoltage status bit; indicates an undervoltage condition has occured.	0x0	R/W1C
		[1]	The overvoltage status bit; indicates an overvoltage condition has occured.	0x0	R/W1C
		[0]	The overcurrent status bit; indicates an overcurrent condition has occured.	0x0	R/W1C

Note to Table 12:

(1) Reserved bits must be written as zero and are read as zero.

(2) Write "1" to clear the Status bits.

Document Revision History

Table 13 lists the revision history for this document.

Table 13. Document Revision History

Date	Version	Changes
February 2014	2.0	Added Cyclone V SoC device support.
July 2012	1.0	Initial release.