# Using the JESD204A Reference Design with Analog Devices AD9644

DS-01022-1.0 Data Sheet

The Altera® JESD204A reference design has a JESD204A compatible analog-to-digital controller (ADC). This data sheet describes how to use the reference design to demonstrate high-speed interoperability between an Altera Arria® II GX FPGA development board and an Analog Devices AD9644 evaluation board.

For more information on the Arria II GX FPGA development board, refer to the Arria II GX Development Kit web page.

The AD9644 is a dual 155 million sample per second (MSPS) ADC with two JESD204A output lanes. The demonstration connects the AD9644 evaluation board, with an interposer card, to the high-speed mezzanine card (HSMC) connector on the Arria II GX development board.

The demonstration has the following features:

- Single link of two lanes at 3.0-Gbps per lane
- JESD204A configuration M.L.F. (links bytes per frame)= 2.2.2
- Host control of the Altera JESD204A ADC controller using System Console
- Serial peripheral interface (SPI) control of the AD9644 from within the FPGA
- 150-MHz frame clock supplied to AD9644 from the FPGA

The system runs with a frame clock of 150 MHz to both the AD9644 and the JESD204A controller in the FPGA. You can configure the JES204A reference design at compile time to one of a limited range of JESD204A modes. For this demonstration, the JESD204A mode is fixed at M.L.F. = 2.2.2. This mode represents two ADC converters (M=2) with one JES204A link consisting of two lanes (L=2). The JESD204A controller in the FPGA performs the necessary lane alignment.

The demonstration operates in the following ways:

- PRBS test data from AD9644
- Data capture of digitized analog input.

Using the PRBS test mode, Altera ran the JESD204A link for over 60 hours with no errors, which demonstrates a BER of better than 10 to 14, which is in excess of the JESD204A specification requirements. In data capture mode a signal generator provides analog input to the ADC board and a block of data is captured into RAM from the Avalon® Streaming (Avalon-ST) output of the JESD204a controller. System console then loads this data to the host for analysis.

101 Innovation Drive
San Jose, CA 95134
www.altera.com

The demonstration requires the following hardware:

- Aria II GX FPGA Development Kit
- Analog Devices AD9644-155 Evaluation Board
- Analog Devices AD9644 to HSMC interposer card
- Short SMA cable

The demonstration requires the following software:

- Quartus® II software version 9.1 SP2
- MATLAB 2010a 32-bit

You use MATLAB to analyze the captured data, such as performing FFTs. The PRBS test does not require it.

The reference design does not require the Analog Devices software as the reference design includes the minimum SPI control to configure the AD9644 directly.

For more information, contact your local Altera sales representative.

# Document Revision History

Table 1 shows the revision history for this document.

**Table 1. Document Revision History**

| Date | Version | Changes |
|---|---|---|
| January 2011 | 1.0 | Initial release. |