

The Open Base Station Architecture Initiative (OBSAI) specifications for base transceiver station (BTS) modules support a wide range of wireless communication protocols.

This data sheet introduces and describes the Altera® OBSAI reference design. The reference design demonstrates the features of the Altera OBSAI IP block, which supports the configuration of modules that implement the RP3 and RP3-01 OBSAI specifications on Altera Arria® II GX devices using the Quartus® II software v10.1.

 For more information about the OBSAI specifications, refer to the [OBSAI](#) website.

## OBSAI IP Core

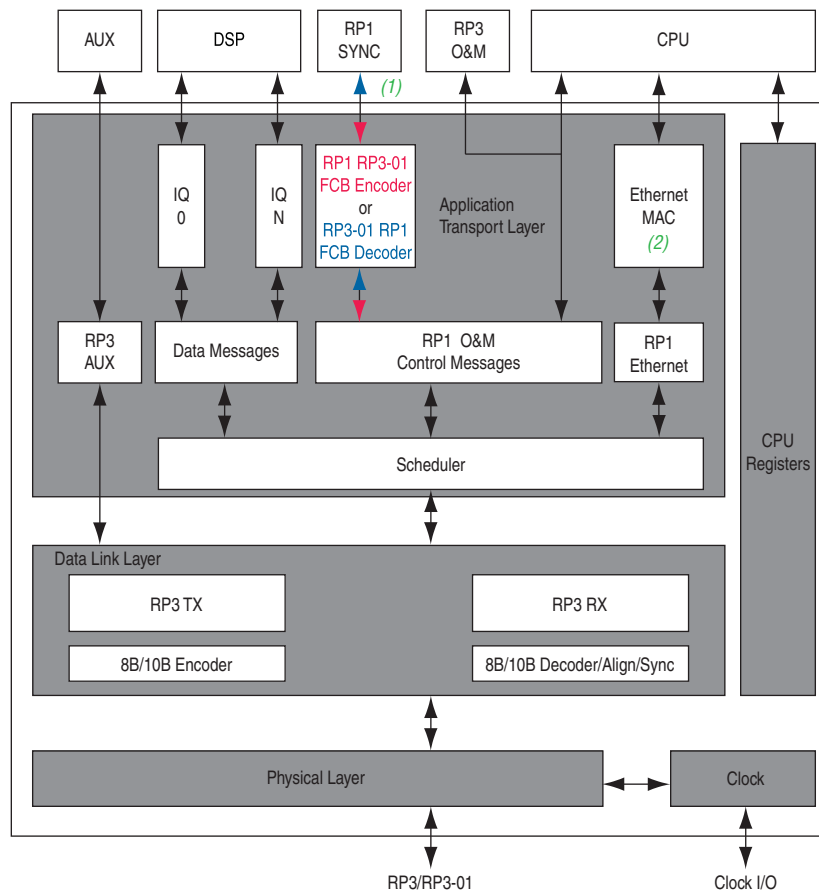
The Altera OBSAI reference design demonstrates the features of the Altera OBSAI IP core. The Altera OBSAI IP block has the following features:

- Complies with the OBSAI RP3 specification v4.1 for wireless base station submodule interconnect supporting the Wideband Code Division Multiple Access (W-CDMA) – frequency division duplexing (FDD), Fixed Worldwide interoperability for Microwave Access (WiMAX) 802.16-2004, Mobile WiMAX 802.16e-2005, Global System for Mobile (GSM)/Enhanced Data rates for GSM Evolution (EDGE), and 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) standards.
- Supports Baseband module (BBM), local converter (LC), and remote radio frequency (RF) unit (RRU) configurations.
- Supports the RP3 Baseband module (BBM) to BBM, RP3 BBM to local converter (LC), and RP3-01 LC to remote radio frequency (RF) unit (RRU) Baseband-to-RF point-to-point interconnect topologies.
- Supports the RP3-01 RRU–RRU tree-and-branch topology, LC–RRU–RRU chain topology, and LC–RRU–LC ring topology.
- Supports the following additional RP3 and RP3-01 interconnect features:
  - Programmable OBSAI communication line rate (to 768, 1536, 3072, or 6144 Mbps) using Altera on-chip high-speed transceivers.
  - Features to support auto-negotiation of line rate.
  - RP3-01 transmission scrambling and descrambling at 6144 Mbps.
  - Accurate OBSAI connection RX delay measurement.
  - Built-in round trip time (RTT) measurement, virtual hardware reset, and loopback messages.

- User-configurable control for encoder and decoder that control system synchronization of RP1 air interface data.
- Test and diagnostic features including loopback Option #1: Serial reverse loopback paths, pseudorandom binary test sequence (PRBS) generation and validation, and all required status signals.
- Includes the following additional interfaces:
  - Interface to external or on-chip processor, using the Altera Avalon<sup>®</sup> Memory-Mapped (Avalon-MM) interconnect specification for bus widths up to 32 bits.
  - Ethernet communication interface that integrates an IEEE 802.3 standard Ethernet media access controller (MAC) 10/100 block with an RP3 Ethernet packet module to support Ethernet communication to and from the RP3-01 connection.
  - Auxiliary interface that allows you to pass RP3 messages or to pass data from slave to master ports to implement switching and routing for RP3 transport layer functionality.
  - Synchronized RP1/RP3 control message interface multiplexed with processor interface.
  - Generic RP3 control message interface multiplexed with processor interface.
  - An IQ data interface with the following features:
    - Implements index-modulo definition of virtual links described in Section 4.4.3 of the OBSAI RP3 specification.
    - Implements optional dual bit map rules described in Section 4.4.3 of the OBSAI RP3 specification.
    - Implements hybrid mapping method to support dual bit map rules for multiple virtual links.
    - Supports up to 43 antenna-carrier interfaces.
    - Supports synchronous buffer mode or simple FIFO mode for antenna-carrier interfaces.
    - Supports up to 16-bit data sample widths at W-CDMA/LTE and WiMAX sample rates on uplink and downlink using the Altera Avalon Streaming (Avalon-ST) interconnect specification.

Figure 1 shows the main submodules of an Altera OBSAI IP block.

**Figure 1. Architecture Overview**



**Notes to Figure 1:**

- (1) An Altera OBSAI IP block configured as an LC includes an input port to an RP1 to RP3-01 encoder and an RP1 to RP3-01 encoder block. An Altera OBSAI IP block configured as an RRU includes an output port from an RP3-01 to RP1 decoder and an RP3-01 to RP1 decoder block. An Altera OBSAI IP block configured as a BBM includes none of these ports or blocks.
- (2) An Altera OBSAI IP block configured as a BBM includes neither an Ethernet MAC nor an RP1 Ethernet block.

An Altera OBSAI IP block configured as an LC includes an RP1 to RP3-01 encoder and an Ethernet MAC. An IP block configured as an RRU includes an RP3-01 to RP1 decoder and an Ethernet MAC. An IP block configured as a BBM includes no encoder, decoder, or Ethernet MAC.

## OBSAI Reference Design

The Altera OBSAI reference design provides a flexible development platform to control, test, and monitor the OBSAI operations. The design configures an SOPC Builder system with a Nios II embedded processor, the OBSAI IP core, and multiple custom test modules to generate stimuli to the OBSAI IP core and check the resulting OBSAI IP core output.

The design performs the following sequence of operations to demonstrate the functionality of the OBSAI IP block:

- Global reset
- Downlink and uplink synchronization
- Basic CPU transactions
- RP1 frame clock burst generation
- IQ data generation and checking
- Ethernet packet transmission and checking through the CPU
- Auxiliary data transmission and checking
- Auto-negotiation of line rate from 3072 Mbps to 1536 Mbps

Altera provides a software package to run the reference design on one or two Arria II GX FPGA development boards. With a single Altera Arria II GX development board and Terasic SFP HSMC card, the reference design configures an LC master in RP3-01 loopback mode. With two Altera Arria II GX development boards and two Terasic SFP HSMC cards, the reference design configures an LC master and RRU slave that communicate through an RP3-01 link. [Figure 2](#) shows the hardware setup for the dual-board reference design. In the single-board reference design, an optical cable connects two SFP transceivers on the same SFP HSMC daughter card.

**Figure 2. Dual Board Reference Design: LC Master to RRU Slave**



 For more information about the Arria II GX FPGA development board, refer to the [Arria II GX FPGA Development Kit web page](#). For more information about the SFP HSMC daughter card, refer to the [Altera Daughter Cards web page](#).

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## Document Revision History

Table 1 shows the revision history for this document.

**Table 1. Document Revision History**

Date	Version	Changes
June 2011	1.0	Initial release.