Digital Channelizer + 2.5Gsps ADC

Reference Design Datasheet

Description

Electronic Warfare Jammers need to analyze wide bandwidths with low signal-to-noise ratios (SNR) to detect critical, time sensitive threats. One way to achieve this is to channelize the wide bandwidth to separate signals of interest from noise and interferers through a filter bank and Fast Fourier Transform (FFT).

To streamline this effort, Altera has developed a highly parameterizable and efficient super-sample rate FFT IP. This allows the designer to select the number of phases and size of the FFT for DSP Builder Advanced Blockset to output an efficient implementation for GHz sample rate Analog to Digital Converters (ADCs). In addition it shows the efficient implementation of FFT for real input, by utilizing half-length transform.

To demonstrate this capability, Altera has incorporated Analog Devices' 2.5Gsps 12-bit ADC AD9625 using JESD204B interface. The reference design displays various channels in Matlab via Altera's system-in-the-loop feature.

For additional information, please contact us at mil@altera.com or contact your local Altera sales representative.

Features

- Programmable super sample rate FFT IP
- Programmable Poly-Phase Filter-Bank IP
- Half-Length FFT Optimization for Real Input Samples
- Altera's System-In-Loop with MATLAB
- JESD204B interface to Analog Devices' 2.5GSps 12-bit ADC AD9625 through FMC
- Altera Arria-10 SoC Development Kit or Reflex Attila Arria-10

Applications

- Digital Electronic Warfare Jammer
- Electronic Intelligence (ELINT)
- Communication Intelligence (COMINT)

Figure 1: General Electronic Warfare System Block Diagram

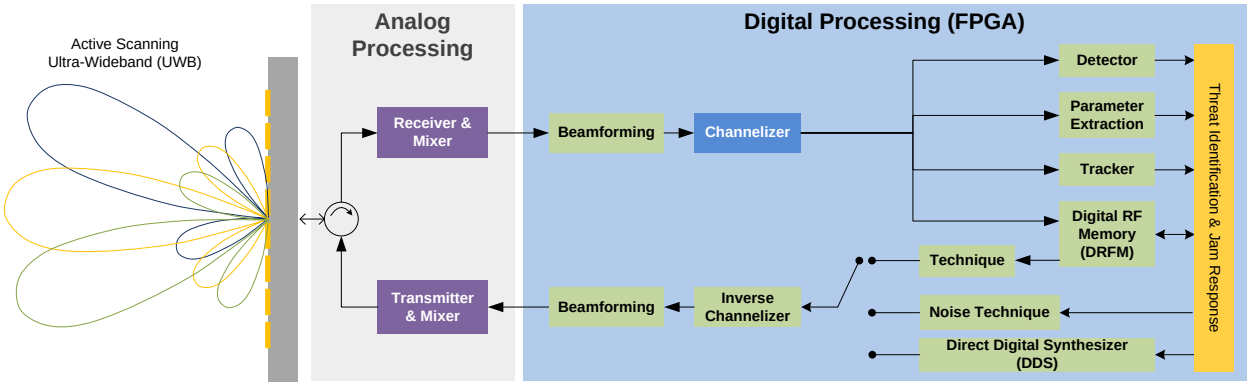


Figure 2: AD9625 Interface with Arria-10 FPGA

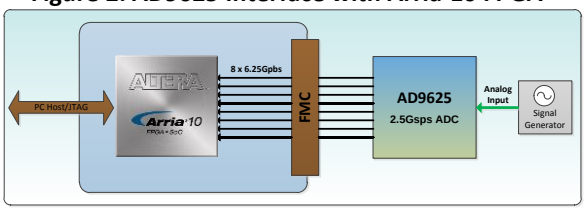
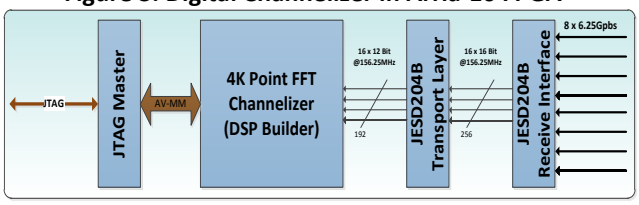


Figure 3: Digital Channelizer in Arria-10 FPGA



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