Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
		NC					D32	E25						
		TDI		TDI			G28	F24						
		TMS		TMS			H28	H22						
		TRST		TRST			J28	D26						
		TCK		TCK			F30	C26						
		TDO		TDO			G29	G24						
1A	VREF1A	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	G31	F26						
1A	VREF1A	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	G30	F25						
1A	VREF1A	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	E32	C28						
1A	VREF1A	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	E31	D27						
1A	VREF1A	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J30	G26	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	J29	G25	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	F32	B28	DQSn1L	DQ1L	DQ1L	DQSn1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	F31	C27	DQS1L	DQ1L/CQn1L	DQ1L	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	K28	H25	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	K27	J24	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	C34	D28	DQSn2L	DQSn1L/DQ1L	DQ1L	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	C33	E28	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREF1A	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	N25	J23	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	M24	J22	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	H32	F28	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	H31	F27	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M27	K21	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	M26	K20	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	D34	G28	DQSn3L	DQ2L	DQSn1L/DQ1L	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREF1A	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D33	G27	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREF1A	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K30	K26	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K29	K25	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J32	J26	DQSn4L	DQSn2L/DQ2L	DQ1L	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J31	J25	DQS4L	DQS2L/CQ2L	DQ1L	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	L29	K24	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	L28	K23	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	E34	H28	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F33	J27	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREF1A	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	M28	L23	DQ5L	DQ3L				
1A	VREF1A	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	N27	L22	DQ5L	DQ3L				
1A	VREF1A	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	F34	J28	DQSn5L	DQ3L				
1A	VREF1A	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	G33	K27	DQS5L	DQ3L/CQn3L				
1A	VREF1A	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	N26		DQ5L	DQ3L				
1A	VREF1A	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	P25		DQ5L	DQ3L				
1A	VREF1A	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	K32		DQSn6L	DQSn3L/DQ3L				
1A	VREF1A	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	K31		DQS6L	DQS3L/CQ3L				
1A	VREF1A	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	L32		DQ6L	DQ3L				
1A	VREF1A	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	L31		DQ6L	DQ3L				
1A	VREF1A	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	G34		DQ6L	DQ3L				
1A	VREF1A	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	H34		DQ6L	DQ3L				
1A	VREF1A	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	N24		DQ7L					
1A	VREF1A	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	P23		DQ7L					
1A	VREF1A	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	J34		DQSn7L					
1A	VREF1A	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	J33		DQS7L					
1A	VREF1A	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	M30		DQ7L					
1A	VREF1A	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	M29		DQ7L					
1A	VREF1A	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	K34							
1A	VREF1A	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	K33							
1C	VREF1C	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	N30		DQ8L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	N29		DQ8L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	N32		DQSn8L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	M31		DQS8L	DQ8L/CQn8L	DQ8L			
1C	VREF1C	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	P29		DQ8L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	P28		DQ8L	DQ8L	DQ8L			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
1C	VREF1C	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	L34		DQSn9L	DQSn8L/DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	M33		DQS9L	DQS8L/CQ8L	DQ8L/CQn8L			
1C	VREF1C	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	R26		DQ9L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	R25		DQ9L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	P32		DQ9L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	N31		DQ9L	DQ8L	DQ8L			
1C	VREF1C	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	R24		DQ10L	DQ9L	DQ8L			
1C	VREF1C	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	T23		DQ10L	DQ9L	DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	M34		DQSn10L	DQ9L	DQSn8L/DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	N33		DQS10L	DQ9L/CQn9L	DQS8L/CQ8L			
1C	VREF1C	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	R28	M23	DQ10L	DQ9L	DQ8L			
1C	VREF1C	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	R27	M22	DQ10L	DQ9L	DQ8L			
1C	VREF1C	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	R32	L26	DQSn11L	DQSn9L/DQ9L	DQ8L	DQSn11L		
1C	VREF1C	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	P31	L25	DQS11L	DQS9L/CQ9L	DQ8L	DQS11L		
1C	VREF1C	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	R30	M21	DQ11L	DQ9L	DQ8L	DQ11L		
1C	VREF1C	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R29	M20	DQ11L	DQ9L	DQ8L	DQ11L		
1C	VREF1C	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	N34	K28	DQ11L	DQ9L	DQ8L	DQ11L		
1C	VREF1C	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	P34	L28	DQ11L	DQ9L	DQ8L	DQ11L		
1C	VREF1C	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	T28	N21	DQ12L	DQ10L		DQ12L	DQ11L	
1C	VREF1C	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	T27	N20	DQ12L	DQ10L		DQ12L	DQ11L	
1C	VREF1C	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	R34	M26	DQSn12L	DQ10L		DQSn12L	DQ11L	
1C	VREF1C	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	R33	M25	DQS12L	DQ10L/CQn10L		DQS12L	DQ11L/CQn11L	
1C	VREF1C	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	T25	N25	DQ12L	DQ10L		DQ12L	DQ11L	
1C	VREF1C	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	T24	M24	DQ12L	DQ10L		DQ12L	DQ11L	
1C	VREF1C	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	T32	M28	DQSn13L	DQSn10L/DQ10L		DQSn13L	DQSn11L/DQ11L	
1C	VREF1C	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	R31	M27	DQS13L	DQS10L/CQ10L		DQS13L	DQS11L/CQ11L	
1C	VREF1C	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	T26	N23	DQ13L	DQ10L		DQ13L	DQ11L	
1C	VREF1C	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	U25	P23	DQ13L	DQ10L		DQ13L	DQ11L	
1C	VREF1C	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	U32	P25	DQ13L	DQ10L		DQ13L	DQ11L	
1C	VREF1C	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	U31	N24	DQ13L	DQ10L		DQ13L	DQ11L	
1C	VREF1C	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	T30	P20						
1C	VREF1C	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	T29	P19						
1C	VREF1C	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	V32	N27						
1C	VREF1C	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	V31	N26						
1C	VREF1C	CLK1n	CLK1n				T34	N28						
1C	VREF1C	CLK1p	CLK1p				T33	P28						
		VCCA_PLL_L2					U28	R22						
		VCCD_PLL_L2					U26	P22						
		VCCD_PLL_L3					V26							
		VCCA_PLL_L3					V28							
2C	VREF2C	CLK3p	CLK3p				V33	R27						
2C	VREF2C	CLK3n	CLK3n				V34	R28						
2C	VREF2C	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	W33	U28						
2C	VREF2C	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	W34	T28						
2C	VREF2C	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	W28	R20						
2C	VREF2C	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	V29	R21						
2C	VREF2C	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AA33	R26	DQ14L	DQ17L		DQ14L	DQ16L	
2C	VREF2C	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	Y34	T27	DQ14L	DQ17L		DQ14L	DQ16L	
2C	VREF2C	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	W26	T25	DQ14L	DQ17L		DQ14L	DQ16L	
2C	VREF2C	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	W27	R25	DQ14L	DQ17L		DQ14L	DQ16L	
2C	VREF2C	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	Y31	V27	DQS14L	DQS17L/CQ17L		DQS14L	DQS16L/CQ16L	
2C	VREF2C	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	Y32	V28	DQSn14L	DQSn17L/DQ17L		DQSn14L	DQSn16L/DQ16L	
2C	VREF2C	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	V24	T20	DQ15L	DQ17L		DQ15L	DQ16L	
2C	VREF2C	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	V25	T21	DQ15L	DQ17L		DQ15L	DQ16L	
2C	VREF2C	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AB33	V26	DQS15L	DQ17L/CQn17L		DQS15L	DQ16L/CQn16L	
2C	VREF2C	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AA34	U26	DQSn15L	DQ17L		DQSn15L	DQ16L	
2C	VREF2C	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	W30	T24	DQ15L	DQ17L		DQ15L	DQ16L	
2C	VREF2C	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	W31	U25	DQ15L	DQ17L		DQ15L	DQ16L	
2C	VREF2C	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AA31	W27	DQ16L	DQ18L	DQ19L	DQ16L		
2C	VREF2C	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AA32	W28	DQ16L	DQ18L	DQ19L	DQ16L		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
2C	VREF2C	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	Y28	T22	DQ16L	DQ18L	DQ19L	DQ16L		
2C	VREF2C	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	Y29	T23	DQ16L	DQ18L	DQ19L	DQ16L		
2C	VREF2C	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	AC34	V24	DQS16L	DQS18L/CQ18L	DQ19L	DQS16L		
2C	VREF2C	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	AB34	V25	DQSn16L	DQSn18L/DQ18L	DQ19L	DQSn16L		
2C	VREF2C	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	Y23	V23	DQ17L	DQ18L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	W24	U23	DQ17L	DQ18L	DQ19L			
2C	VREF2C	IO			DIFFIO_RX_L29p	DIFFOUT_L57p	AB31		DQS17L	DQ18L/CQn18L	DQS19L/CQ19L			
2C	VREF2C	IO			DIFFIO_RX_L29n	DIFFOUT_L57n	AB32		DQSn17L	DQ18L	DQSn19L/DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L29p	DIFFOUT_L58p	AA29		DQ17L	DQ18L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L29n	DIFFOUT_L58n	AA30		DQ17L	DQ18L	DQ19L			
2C	VREF2C	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AD33		DQ18L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_RX_L30n	DIFFOUT_L59n	AD34		DQ18L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	Y25		DQ18L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L30n	DIFFOUT_L60n	Y26		DQ18L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AC31		DQS18L	DQS19L/CQ19L	DQ19L/CQn19L			
2C	VREF2C	IO			DIFFIO_RX_L31n	DIFFOUT_L61n	AC32		DQSn18L	DQSn19L/DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AA27		DQ19L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AA28		DQ19L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	AE33		DQS19L	DQ19L/CQn19L	DQ19L			
2C	VREF2C	IO			DIFFIO_RX_L32n	DIFFOUT_L63n	AE34		DQSn19L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AB29		DQ19L	DQ19L	DQ19L			
2C	VREF2C	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AB30		DQ19L	DQ19L	DQ19L			
2A	VREF2A	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AG33							
2A	VREF2A	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	AF34							
2A	VREF2A	IO			DIFFIO_TX_L33p	DIFFOUT_L66p	AA24		DQ20L					
2A	VREF2A	IO			DIFFIO_TX_L33n	DIFFOUT_L66n	AA25		DQ20L					
2A	VREF2A	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AE31		DQS20L					
2A	VREF2A	IO			DIFFIO_RX_L34n	DIFFOUT_L67n	AE32		DQSn20L					
2A	VREF2A	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AC28		DQ20L					
2A	VREF2A	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AC29		DQ20L					
2A	VREF2A	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AH33		DQ21L	DQ24L				
2A	VREF2A	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AG34		DQ21L	DQ24L				
2A	VREF2A	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AD30		DQ21L	DQ24L				
2A	VREF2A	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AD31		DQ21L	DQ24L				
2A	VREF2A	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AF31		DQS21L	DQS24L/CQ24L				
2A	VREF2A	IO			DIFFIO_RX_L36n	DIFFOUT_L71n	AF32		DQSn21L	DQSn24L/DQ24L				
2A	VREF2A	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AB24		DQ22L	DQ24L				
2A	VREF2A	IO			DIFFIO_TX_L36n	DIFFOUT_L72n	AB25		DQ22L	DQ24L				
2A	VREF2A	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AJ34	AA27	DQS22L	DQ24L/CQn24L				
2A	VREF2A	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	AH34	Y28	DQSn22L	DQ24L				
2A	VREF2A	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AB26	W22	DQ22L	DQ24L				
2A	VREF2A	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AB27	W23	DQ22L	DQ24L				
2A	VREF2A	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AG31	AB27	DQ23L	DQ25L	DQ26L	DQ23L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AG32	AA28	DQ23L	DQ25L	DQ26L	DQ23L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AE29	W24	DQ23L	DQ25L	DQ26L	DQ23L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AE30	W25	DQ23L	DQ25L	DQ26L	DQ23L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	AK33	Y25	DQS23L	DQS25L/CQ25L	DQ26L	DQS23L	DQS25L/CQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	AK34	Y26	DQSn23L	DQSn25L/DQ25L	DQ26L	DQSn23L	DQSn25L/DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	AD28	V20	DQ24L	DQ25L	DQ26L	DQ24L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	AD29	V21	DQ24L	DQ25L	DQ26L	DQ24L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AJ31	AC28	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L
2A	VREF2A	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AJ32	AB28	DQSn24L	DQ25L	DQSn26L/DQ26L	DQSn24L	DQ25L	DQSn26L/DQ26L
2A	VREF2A	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AF28	AA25	DQ24L	DQ25L	DQ26L	DQ24L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AF29	AA26	DQ24L	DQ25L	DQ26L	DQ24L	DQ25L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AM34	AB25	DQ25L	DQ26L	DQ26L	DQ25L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AL34	AB26	DQ25L	DQ26L	DQ26L	DQ25L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AE27	AC25	DQ25L	DQ26L	DQ26L	DQ25L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AE28	AC26	DQ25L	DQ26L	DQ26L	DQ25L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AH30	AD27	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L
2A	VREF2A	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AH31	AD28	DQSn25L	DQSn26L/DQ26L	DQ26L	DQSn25L	DQSn26L/DQ26L	DQ26L

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
2A	VREF2A	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AD26	W20	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	AD27	W21	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AL32	AG28	DQS26L	DQ26L/CQn26L	DQ26L	DQS26L	DQ26L/CQn26L	DQ26L
2A	VREF2A	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AL33	AF28	DQSn26L	DQ26L	DQ26L	DQSn26L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AC25	Y23	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L
2A	VREF2A	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AC26	AA24	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L	DQ26L
2A	VREF2A	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AK31	AE27						
2A	VREF2A	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AK32	AE28						
2A	VREF2A	IO			DIFFIO_TX_L44p	DIFFOUT_L88p	AG29	AA23						
2A	VREF2A	IO			DIFFIO_TX_L44n	DIFFOUT_L88n	AG30	AB24						
		nCONFIG		nCONFIG			AE25	W19						
		nSTATUS		nSTATUS			AH28	AD25						
		CONF_DONE		CONF_DONE			AH29	AE26						
		PORSEL		PORSEL			AF26	AB23						
		nCE		nCE			AE26	Y20						
		NC					AL31	AB22						
3A	VREF3A	IO				DIFFOUT_B1n	AH27	AF26	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREF3A	IO				DIFFOUT_B1p	AJ27	AH27	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREF3A	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AK28	AH25	DQSn1B	DQ1B	DQ1B	DQSn1B	DQ1B	DQ1B
3A	VREF3A	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AJ28	AG25	DQS1B	DQ1B/CQn1B	DQ1B	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREF3A	IO				DIFFOUT_B3n	AJ29	AG27	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREF3A	IO				DIFFOUT_B3p	AJ26	AH26	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AM32	AE22	DQSn2B	DQSn1B/DQ1B	DQ1B	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AM31	AD22	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREF3A	IO				DIFFOUT_B5n	AL29	AB20	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREF3A	IO				DIFFOUT_B5p	AM29	AB21	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AN30	AD21	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AM30	AC21	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREF3A	IO				DIFFOUT_B7n	AH26	AD24	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREF3A	IO				DIFFOUT_B7p	AF24	AE23	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH24	AF24	DQSn3B	DQ2B	DQSn1B/DQ1B	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREF3A	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG24	AE24	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREF3A	IO				DIFFOUT_B9n	AH25	AF23	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREF3A	IO				DIFFOUT_B9p	AF23	AG24	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AP33	AH24	DQSn4B	DQSn2B/DQ2B	DQ1B	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AN33	AH23	DQS4B	DQS2B/CQ2B	DQ1B	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREF3A	IO				DIFFOUT_B11n	AP32	AH20	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREF3A	IO				DIFFOUT_B11p	AP30	AH21	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AP31	AH22	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREF3A	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AN31	AG22	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREF3A	IO				DIFFOUT_B13n	AK27	AC20	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREF3A	IO				DIFFOUT_B13p	AL28	AG21	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREF3A	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AL27	AF21	DQSn5B	DQ3B		DQSn5B	DQ3B	
3A	VREF3A	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AL26	AE21	DQS5B	DQ3B/CQn3B		DQS5B	DQ3B/CQn3B	
3A	VREF3A	IO				DIFFOUT_B15n	AK25	AF20	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREF3A	IO				DIFFOUT_B15p	AM26	AE20	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREF3A	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AP28	AD19	DQSn6B	DQSn3B/DQ3B		DQSn6B	DQSn3B/DQ3B	
3A	VREF3A	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AN28	AC19	DQS6B	DQS3B/CQ3B		DQS6B	DQS3B/CQ3B	
3A	VREF3A	IO				DIFFOUT_B17n	AM28	AB19	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREF3A	IO				DIFFOUT_B17p	AP29	AA19	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREF3A	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AP27	AE19	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREF3A	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AN27	AD18	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREF3A	IO				DIFFOUT_B19n	AE24	Y19						
3A	VREF3A	IO				DIFFOUT_B19p	AE23	AA18						
3A	VREF3A	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AD22	Y18						
3A	VREF3A	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AC22	Y17						
3B	VREF3B	IO				DIFFOUT_B21n	AH23		DQ7B	DQ7B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B21p	AJ24		DQ7B	DQ7B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AJ22		DQSn7B	DQ7B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AH22		DQS7B	DQ7B/CQn7B	DQ7B			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
3B	VREF3B	IO				DIFFOUT_B23n	AJ23		DQ7B	DQ7B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B23p	AK22		DQ7B	DQ7B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AM24		DQSn8B	DQSn7B/DQ7B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AL24		DQS8B	DQS7B/CQ7B	DQ7B/CQn7B			
3B	VREF3B	IO				DIFFOUT_B25n	AK24		DQ8B	DQ7B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B25p	AL25		DQ8B	DQ7B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AM23		DQ8B	DQ7B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AL23		DQ8B	DQ7B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B27n	AE22		DQ9B	DQ8B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B27p	AE21		DQ9B	DQ8B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AG21		DQSn9B	DQ8B	DQSn7B/DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AF21		DQS9B	DQ8B/CQn8B	DQS7B/CQ7B			
3B	VREF3B	IO				DIFFOUT_B29n	AD21		DQ9B	DQ8B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B29p	AE20		DQ9B	DQ8B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AP25		DQSn10B	DQSn8B/DQ8B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AN25		DQS10B	DQS8B/CQ8B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B31n	AP26		DQ10B	DQ8B	DQ7B			
3B	VREF3B	IO				DIFFOUT_B31p	AP23		DQ10B	DQ8B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AP24		DQ10B	DQ8B	DQ7B			
3B	VREF3B	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AN24		DQ10B	DQ8B	DQ7B			
3C	VREF3C	IO				DIFFOUT_B33n	AL22	AF19	DQ11B	DQ11B		DQ11B	DQ11B	
3C	VREF3C	IO				DIFFOUT_B33p	AM22	AG19	DQ11B	DQ11B		DQ11B	DQ11B	
3C	VREF3C	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AL21	AH19	DQSn11B	DQ11B		DQSn11B	DQ11B	
3C	VREF3C	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AK21	AG18	DQS11B	DQ11B/CQn11B		DQS11B	DQ11B/CQn11B	
3C	VREF3C	IO				DIFFOUT_B35n	AJ20	AH17	DQ11B	DQ11B		DQ11B	DQ11B	
3C	VREF3C	IO				DIFFOUT_B35p	AJ21	AH18	DQ11B	DQ11B		DQ11B	DQ11B	
3C	VREF3C	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AP22	AF17	DQSn12B	DQSn11B/DQ11B		DQSn12B	DQSn11B/DQ11B	
3C	VREF3C	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AN22	AE18	DQS12B	DQS11B/CQ11B		DQS12B	DQS11B/CQ11B	
3C	VREF3C	IO				DIFFOUT_B37n	AM21	AE16	DQ12B	DQ11B		DQ12B	DQ11B	
3C	VREF3C	IO				DIFFOUT_B37p	AP20	AD16	DQ12B	DQ11B		DQ12B	DQ11B	
3C	VREF3C	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AP21	AF16	DQ12B	DQ11B		DQ12B	DQ11B	
3C	VREF3C	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AN21	AE17	DQ12B	DQ11B		DQ12B	DQ11B	
3C	VREF3C	IO				DIFFOUT_B39n	AL20		DQ13B					
3C	VREF3C	IO				DIFFOUT_B39p	AM18		DQ13B					
3C	VREF3C	IO			DIFFIO_RX_B20n	DIFFOUT_B40n	AM19		DQSn13B					
3C	VREF3C	IO			DIFFIO_RX_B20p	DIFFOUT_B40p	AL19		DQS13B					
3C	VREF3C	IO				DIFFOUT_B41n	AK18		DQ13B					
3C	VREF3C	IO				DIFFOUT_B41p	AL18		DQ13B					
3C	VREF3C	IO			DIFFIO_RX_B21n	DIFFOUT_B42n	AF20							
3C	VREF3C	IO			DIFFIO_RX_B21p	DIFFOUT_B42p	AF19							
3C	VREF3C	IO	PLL_B1_CLKOUT4			DIFFOUT_B43n	AE19	AC17						
3C	VREF3C	IO	PLL_B1_CLKOUT3			DIFFOUT_B43p	AD19	AB17						
3C	VREF3C	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AH19	AC16						
3C	VREF3C	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AG19	AB16						
3C	VREF3C	IO	PLL_B1_CLKOUT0n			DIFFOUT_B45n	AE18	AA15						
3C	VREF3C	IO	PLL_B1_CLKOUT0p			DIFFOUT_B45p	AD18	Y15						
3C	VREF3C	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B23n	DIFFOUT_B46n	AK19	AH16						
3C	VREF3C	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B23p	DIFFOUT_B46p	AJ19	AG16						
3C	VREF3C	IO	CLK5n			DIFFOUT_B47n	AP19	AH15						
3C	VREF3C	IO	CLK5p			DIFFOUT_B47p	AN19	AG15						
3C	VREF3C	IO	CLK4n		DIFFIO_RX_B24n	DIFFOUT_B48n	AP18	AF15						
3C	VREF3C	IO	CLK4p		DIFFIO_RX_B24p	DIFFOUT_B48p	AN18	AE15						
		VCC_CLKIN3C					AG18	AB14						
		VCCA_PLL_B1					AH18	AC14						
		VCCD_PLL_B1					AF18	AB15						
		VCCD_PLL_B2					AF17							
		VCCA_PLL_B2					AH17							
		VCC_CLKIN4C					AE17	AC13						
4C	VREF4C	IO	CLK6p		DIFFIO_RX_B25p	DIFFOUT_B49p	AN16	AE14						
4C	VREF4C	IO	CLK6n		DIFFIO_RX_B25n	DIFFOUT_B49n	AP16	AF14						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
4C	VREF4C	IO	CLK7p			DIFFOUT_B50p	AN15	AG13						
4C	VREF4C	IO	CLK7n			DIFFOUT_B50n	AP15	AH14						
4C	VREF4C	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B26p	DIFFOUT_B51p	AL17							
4C	VREF4C	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B26n	DIFFOUT_B51n	AM17							
4C	VREF4C	IO	PLL_B2_CLKOUT0p			DIFFOUT_B52p	AE16							
4C	VREF4C	IO	PLL_B2_CLKOUT0n			DIFFOUT_B52n	AF16							
4C	VREF4C	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AL16							
4C	VREF4C	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AM16							
4C	VREF4C	IO	PLL_B2_CLKOUT3			DIFFOUT_B54p	AD15							
4C	VREF4C	IO	PLL_B2_CLKOUT4			DIFFOUT_B54n	AD16							
4C	VREF4C	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AJ16	AG12						
4C	VREF4C	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AK16	AH13						
4C	VREF4C	IO				DIFFOUT_B56p	AL15	Y13	DQ14B			DQ14B		
4C	VREF4C	IO				DIFFOUT_B56n	AM15	Y14	DQ14B			DQ14B		
4C	VREF4C	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AL14	AD13	DQS14B			DQS14B		
4C	VREF4C	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AM14	AE13	DQSn14B			DQSn14B		
4C	VREF4C	IO				DIFFOUT_B58p	AK13	AA13	DQ14B			DQ14B		
4C	VREF4C	IO				DIFFOUT_B58n	AL13	AB13	DQ14B			DQ14B		
4C	VREF4C	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AH15	AG10	DQ15B	DQ16B		DQ15B	DQ16B	
4C	VREF4C	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AJ15	AH10	DQ15B	DQ16B		DQ15B	DQ16B	
4C	VREF4C	IO				DIFFOUT_B60p	AG15	AH11	DQ15B	DQ16B		DQ15B	DQ16B	
4C	VREF4C	IO				DIFFOUT_B60n	AK15	AH12	DQ15B	DQ16B		DQ15B	DQ16B	
4C	VREF4C	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AH14	AF10	DQS15B	DQS16B/CQ16B		DQS15B	DQS16B/CQ16B	
4C	VREF4C	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AJ14	AF11	DQSn15B	DQSn16B/DQ16B		DQSn15B	DQSn16B/DQ16B	
4C	VREF4C	IO				DIFFOUT_B62p	AP14	AF12	DQ16B	DQ16B		DQ16B	DQ16B	
4C	VREF4C	IO				DIFFOUT_B62n	AN13	AC12	DQ16B	DQ16B		DQ16B	DQ16B	
4C	VREF4C	IO			DIFFIO_RX_B32p	DIFFOUT_B63p	AN12	AD12	DQS16B	DQ16B/CQn16B		DQS16B	DQ16B/CQn16B	
4C	VREF4C	IO			DIFFIO_RX_B32n	DIFFOUT_B63n	AP12	AE12	DQSn16B	DQ16B		DQSn16B	DQ16B	
4C	VREF4C	IO				DIFFOUT_B64p	AM12	AC11	DQ16B	DQ16B		DQ16B	DQ16B	
4C	VREF4C	IO				DIFFOUT_B64n	AP13	AE11	DQ16B	DQ16B		DQ16B	DQ16B	
4B	VREF4B	IO			DIFFIO_RX_B33p	DIFFOUT_B65p	AN10		DQ17B	DQ19B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B33n	DIFFOUT_B65n	AP10		DQ17B	DQ19B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B66p	AP9		DQ17B	DQ19B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B66n	AP11		DQ17B	DQ19B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B34p	DIFFOUT_B67p	AM9		DQS17B	DQS19B/CQ19B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B34n	DIFFOUT_B67n	AN9		DQSn17B	DQSn19B/DQ19B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B68p	AE15		DQ18B	DQ19B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B68n	AF15		DQ18B	DQ19B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AF13		DQS18B	DQ19B/CQn19B	DQS20B/CQ20B			
4B	VREF4B	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AF14		DQSn18B	DQ19B	DQSn20B/DQ20B			
4B	VREF4B	IO				DIFFOUT_B70p	AE13		DQ18B	DQ19B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B70n	AE14		DQ18B	DQ19B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AK12		DQ19B	DQ20B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AL12		DQ19B	DQ20B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B72p	AK10		DQ19B	DQ20B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B72n	AM11		DQ19B	DQ20B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AL10		DQS19B	DQS20B/CQ20B	DQ20B/CQn20B			
4B	VREF4B	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AL11		DQSn19B	DQSn20B/DQ20B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B74p	AM8		DQ20B	DQ20B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B74n	AP8		DQ20B	DQ20B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AN7		DQS20B	DQ20B/CQn20B	DQ20B			
4B	VREF4B	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AP7		DQSn20B	DQ20B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B76p	AP6		DQ20B	DQ20B	DQ20B			
4B	VREF4B	IO				DIFFOUT_B76n	AM7		DQ20B	DQ20B	DQ20B			
4A	VREF4A	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AC12	AB11						
4A	VREF4A	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AD12	AC10						
4A	VREF4A	IO				DIFFOUT_B78p	AE12	Y10						
4A	VREF4A	IO				DIFFOUT_B78n	AD13	Y11						
4A	VREF4A	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AH12	AG9	DQ21B	DQ24B		DQ21B	DQ24B	
4A	VREF4A	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AJ12	AH8	DQ21B	DQ24B		DQ21B	DQ24B	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
4A	VREF4A	IO				DIFFOUT_B80p	AG12	AE10	DQ21B	DQ24B		DQ21B	DQ24B	
4A	VREF4A	IO				DIFFOUT_B80n	AJ13	AH9	DQ21B	DQ24B		DQ21B	DQ24B	
4A	VREF4A	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AH11	AE9	DQS21B	DQS24B/CQ24B		DQS21B	DQS24B/CQ24B	
4A	VREF4A	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AJ11	AF9	DQSn21B	DQSn24B/DQ24B		DQSn21B	DQSn24B/DQ24B	
4A	VREF4A	IO				DIFFOUT_B82p	AJ10	AF8	DQ22B	DQ24B		DQ22B	DQ24B	
4A	VREF4A	IO				DIFFOUT_B82n	AL8	AE8	DQ22B	DQ24B		DQ22B	DQ24B	
4A	VREF4A	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AK9	AG7	DQS22B	DQ24B/CQn24B		DQS22B	DQ24B/CQn24B	
4A	VREF4A	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AL9	AH7	DQSn22B	DQ24B		DQSn22B	DQ24B	
4A	VREF4A	IO				DIFFOUT_B84p	AL7	AG6	DQ22B	DQ24B		DQ22B	DQ24B	
4A	VREF4A	IO				DIFFOUT_B84n	AJ9	AH6	DQ22B	DQ24B		DQ22B	DQ24B	
4A	VREF4A	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AN4	AG4	DQ23B	DQ25B	DQ26B	DQ23B	DQ25B	DQ26B
4A	VREF4A	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AP4	AH3	DQ23B	DQ25B	DQ26B	DQ23B	DQ25B	DQ26B
4A	VREF4A	IO				DIFFOUT_B86p	AP2	AH4	DQ23B	DQ25B	DQ26B	DQ23B	DQ25B	DQ26B
4A	VREF4A	IO				DIFFOUT_B86n	AP5	AH5	DQ23B	DQ25B	DQ26B	DQ23B	DQ25B	DQ26B
4A	VREF4A	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AN3	AG3	DQS23B	DQS25B/CQ25B	DQ26B	DQS23B	DQS25B/CQ25B	DQ26B
4A	VREF4A	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AP3	AH2	DQSn23B	DQSn25B/DQ25B	DQ26B	DQSn23B	DQSn25B/DQ25B	DQ26B
4A	VREF4A	IO				DIFFOUT_B88p	AM6	AD9	DQ24B	DQ25B	DQ26B	DQ24B	DQ25B	DQ26B
4A	VREF4A	IO				DIFFOUT_B88n	AN6	AC9	DQ24B	DQ25B	DQ26B	DQ24B	DQ25B	DQ26B
4A	VREF4A	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AL5	AA9	DQS24B	DQ25B/CQn25B	DQS26B/CQ26B	DQS24B	DQ25B/CQn25B	DQS26B/CQ26B
4A	VREF4A	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AM5	AB9	DQSn24B	DQ25B	DQSn26B/DQ26B	DQSn24B	DQ25B	DQSn26B/DQ26B
4A	VREF4A	IO				DIFFOUT_B90p	AL4	Y9	DQ24B	DQ25B	DQ26B	DQ24B	DQ25B	DQ26B
4A	VREF4A	IO				DIFFOUT_B90n	AM4	AA10	DQ24B	DQ25B	DQ26B	DQ24B	DQ25B	DQ26B
4A	VREF4A	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AJ7	AE6	DQ25B	DQ26B	DQ26B	DQ25B	DQ26B	DQ26B
4A	VREF4A	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AK7	AF6	DQ25B	DQ26B	DQ26B	DQ25B	DQ26B	DQ26B
4A	VREF4A	IO				DIFFOUT_B92p	AJ6	AE4	DQ25B	DQ26B	DQ26B	DQ25B	DQ26B	DQ26B
4A	VREF4A	IO				DIFFOUT_B92n	AK6	AE7	DQ25B	DQ26B	DQ26B	DQ25B	DQ26B	DQ26B
4A	VREF4A	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AH8	AE5	DQS25B	DQS26B/CQ26B	DQ26B/CQn26B	DQS25B	DQS26B/CQ26B	DQ26B/CQn26B
4A	VREF4A	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AJ8	AF5	DQSn25B	DQSn26B/DQ26B	DQ26B	DQSn25B	DQSn26B/DQ26B	DQ26B
4A	VREF4A	IO				DIFFOUT_B94p	AE11	AB8	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B
4A	VREF4A	IO				DIFFOUT_B94n	AF11	AC8	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B
4A	VREF4A	IO	RUP4A		DIFFIO_RX_B48p	DIFFOUT_B95p	AG9	AC7	DQS26B	DQ26B/CQn26B	DQ26B	DQS26B	DQ26B/CQn26B	DQ26B
4A	VREF4A	IO	RDN4A		DIFFIO_RX_B48n	DIFFOUT_B95n	AH9	AD7	DQSn26B	DQ26B	DQ26B	DQSn26B	DQ26B	DQ26B
4A	VREF4A	IO				DIFFOUT_B96p	AE10	AB7	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B
4A	VREF4A	IO				DIFFOUT_B96n	AF10	AD6	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B	DQ26B
		NC					AH7	W10						
		GND					AF9	AF3						
		nIO_PULLUP		nIO_PULLUP			AF8	AE3						
		nCEO		nCEO			AJ5	AB5						
		DCLK		DCLK			AL3	AC5						
		nCSO		nCSO			AE9	AD4						
		ASDO		ASDO			AH6	AA6						
5A	VREF5A	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AH4	AC3						
5A	VREF5A	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AH5	AC4						
5A	VREF5A	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AK3	AF1						
5A	VREF5A	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AK4	AE2						
5A	VREF5A	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AE7	AB3	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AE8	AB4	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AM1	AG1	DQSn1R	DQ1R	DQ1R	DQSn1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AM2	AF2	DQS1R	DQ1R/CQn1R	DQ1R	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AF5	Y6	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AF6	Y7	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AJ3	AE1	DQSn2R	DQSn1R/DQ1R	DQ1R	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AJ4	AD1	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREF5A	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AC8	AA4	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AC9	Y5	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AL1	AC1	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AL2	AC2	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AE5	Y3	DQ3R	DQ2R	DQ1R	DQ3R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AE6	Y4	DQ3R	DQ2R	DQ1R	DQ3R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AG3	AB1	DQSn3R	DQ2R	DQSn1R/DQ1R	DQSn3R	DQ2R	DQSn1R/DQ1R

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
5A	VREF5A	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AG4	AB2	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREF5A	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AB10	W8	DQ3R	DQ2R	DQ1R	DQ3R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AC11	W9	DQ3R	DQ2R	DQ1R	DQ3R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AK1	AA1	DQSn4R	DQSn2R/DQ2R	DQ1R	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AJ2	Y2	DQS4R	DQS2R/CQ2R	DQ1R	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AD6	W5	DQ4R	DQ2R	DQ1R	DQ4R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AD7	W6	DQ4R	DQ2R	DQ1R	DQ4R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AJ1	Y1	DQ4R	DQ2R	DQ1R	DQ4R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AH2	W2	DQ4R	DQ2R	DQ1R	DQ4R	DQ2R	DQ1R
5A	VREF5A	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AC7	V6	DQ5R	DQ3R				
5A	VREF5A	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AB8	V7	DQ5R	DQ3R				
5A	VREF5A	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AF3	W3	DQSn5R	DQ3R				
5A	VREF5A	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AF4	W4	DQS5R	DQ3R/CQn3R				
5A	VREF5A	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AB9		DQ5R	DQ3R				
5A	VREF5A	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AA10		DQ5R	DQ3R				
5A	VREF5A	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AH1		DQSn6R	DQSn3R/DQ3R				
5A	VREF5A	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AG1		DQS6R	DQS3R/CQ3R				
5A	VREF5A	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AC5		DQ6R	DQ3R				
5A	VREF5A	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AC6		DQ6R	DQ3R				
5A	VREF5A	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AF1		DQ6R	DQ3R				
5A	VREF5A	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AF2		DQ6R	DQ3R				
5A	VREF5A	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AB11		DQ7R					
5A	VREF5A	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AA12		DQ7R					
5A	VREF5A	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AE3		DQSn7R					
5A	VREF5A	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AE4		DQS7R					
5A	VREF5A	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AD3		DQ7R					
5A	VREF5A	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AD4		DQ7R					
5A	VREF5A	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AE1							
5A	VREF5A	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AE2							
5C	VREF5C	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AB5		DQ8R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AB6		DQ8R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	AB3		DQSn8R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AC4		DQS8R	DQ8R/CQn8R	DQ8R			
5C	VREF5C	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AA6		DQ8R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AA7		DQ8R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R14n	DIFFOUT_R28n	AD1		DQSn9R	DQSn8R/DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AC2		DQS9R	DQS8R/CQ8R	DQ8R/CQn8R			
5C	VREF5C	IO			DIFFIO_TX_R15n	DIFFOUT_R29n	Y9		DQ9R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	Y10		DQ9R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R15n	DIFFOUT_R30n	AA3		DQ9R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AB4		DQ9R	DQ8R	DQ8R			
5C	VREF5C	IO			DIFFIO_TX_R16n	DIFFOUT_R31n	Y7		DQ10R	DQ9R	DQ8R			
5C	VREF5C	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	Y8		DQ10R	DQ9R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R16n	DIFFOUT_R32n	AC1		DQSn10R	DQ9R	DQSn8R/DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AB2		DQS10R	DQ9R/CQn9R	DQS8R/CQ8R			
5C	VREF5C	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	Y11	U6	DQ10R	DQ9R	DQ8R			
5C	VREF5C	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	W12	U7	DQ10R	DQ9R	DQ8R			
5C	VREF5C	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	Y3	V3	DQSn11R	DQSn9R/DQ9R	DQ8R	DQSn11R		
5C	VREF5C	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	AA4	V4	DQS11R	DQS9R/CQ9R	DQ8R	DQS11R		
5C	VREF5C	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	Y5	U8	DQ11R	DQ9R	DQ8R	DQ11R		
5C	VREF5C	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	Y6	U9	DQ11R	DQ9R	DQ8R	DQ11R		
5C	VREF5C	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	AB1	W1	DQ11R	DQ9R	DQ8R	DQ11R		
5C	VREF5C	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	AA1	V1	DQ11R	DQ9R	DQ8R	DQ11R		
5C	VREF5C	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	W7	T4	DQ12R	DQ10R		DQ12R	DQ11R	
5C	VREF5C	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	W8	U5	DQ12R	DQ10R		DQ12R	DQ11R	
5C	VREF5C	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	W3	U3	DQSn12R	DQ10R		DQSn12R	DQ11R	
5C	VREF5C	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	Y4	U4	DQS12R	DQ10R/CQn10R		DQS12R	DQ11R/CQn11R	
5C	VREF5C	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	W10	T8	DQ12R	DQ10R		DQ12R	DQ11R	
5C	VREF5C	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	W11	T9	DQ12R	DQ10R		DQ12R	DQ11R	
5C	VREF5C	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	Y1	T2	DQSn13R	DQSn10R/DQ10R		DQSn13R	DQSn11R/DQ11R	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
5C	VREF5C	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	Y2	T3	DQS13R	DQS10R/CQ10R		DQS13R	DQS11R/CQ11R	
5C	VREF5C	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	W5	T6	DQ13R	DQ10R		DQ13R	DQ11R	
5C	VREF5C	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	W6	R6	DQ13R	DQ10R		DQ13R	DQ11R	
5C	VREF5C	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	V3	R4	DQ13R	DQ10R		DQ13R	DQ11R	
5C	VREF5C	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	V4	T5	DQ13R	DQ10R		DQ13R	DQ11R	
5C	VREF5C	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	W9	R9						
5C	VREF5C	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	V10	R10						
5C	VREF5C	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	U3	U1						
5C	VREF5C	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	U4	U2						
5C	VREF5C	CLK8n	CLK8n				W1	T1						
5C	VREF5C	CLK8p	CLK8p				W2	R1						
		VCCA_PLL_R3					V7							
		VCCD_PLL_R3					V9							
		VCCD_PLL_R2					U9	P7						
		VCCA_PLL_R2					U7	R7						
6C	VREF6C	CLK10p	CLK10p				U2	P2						
6C	VREF6C	CLK10n	CLK10n				U1	P1						
6C	VREF6C	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	T2	M1						
6C	VREF6C	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	T1	N1						
6C	VREF6C	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	U11	P9						
6C	VREF6C	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	U10	P8						
6C	VREF6C	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	P2	N4	DQ14R	DQ17R		DQ14R	DQ16R	
6C	VREF6C	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	R1	P4	DQ14R	DQ17R		DQ14R	DQ16R	
6C	VREF6C	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	T7	N7	DQ14R	DQ17R		DQ14R	DQ16R	
6C	VREF6C	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	U6	N6	DQ14R	DQ17R		DQ14R	DQ16R	
6C	VREF6C	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	R4	P3	DQS14R	DQS17R/CQ17R		DQS14R	DQS16R/CQ16R	
6C	VREF6C	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	R3	N2	DQSn14R	DQSn17R/DQ17R		DQSn14R	DQSn16R/DQ16R	
6C	VREF6C	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	T9	N5	DQ15R	DQ17R		DQ15R	DQ16R	
6C	VREF6C	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	T8	M4	DQ15R	DQ17R		DQ15R	DQ16R	
6C	VREF6C	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	N2	L2	DQS15R	DQ17R/CQn17R		DQS15R	DQ16R/CQn16R	
6C	VREF6C	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	P1	L1	DQSn15R	DQ17R		DQSn15R	DQ16R	
6C	VREF6C	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	T5	N9	DQ15R	DQ17R		DQ15R	DQ16R	
6C	VREF6C	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	T4	N8	DQ15R	DQ17R		DQ15R	DQ16R	
6C	VREF6C	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	P4	L3	DQ16R	DQ18R	DQ19R	DQ16R		
6C	VREF6C	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	P3	M3	DQ16R	DQ18R	DQ19R	DQ16R		
6C	VREF6C	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	R7	L5	DQ16R	DQ18R	DQ19R	DQ16R		
6C	VREF6C	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	R6	L4	DQ16R	DQ18R	DQ19R	DQ16R		
6C	VREF6C	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	M1	K2	DQS16R	DQS18R/CQ18R	DQ19R	DQS16R		
6C	VREF6C	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	N1	K1	DQSn16R	DQSn18R/DQ18R	DQ19R	DQSn16R		
6C	VREF6C	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	P6	L6	DQ17R	DQ18R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	P5	M6	DQ17R	DQ18R	DQ19R			
6C	VREF6C	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	N4		DQS17R	DQ18R/CQn18R	DQS19R/CQ19R			
6C	VREF6C	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	N3		DQSn17R	DQ18R	DQSn19R/DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	R12		DQ17R	DQ18R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	T11		DQ17R	DQ18R	DQ19R			
6C	VREF6C	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	L2		DQ18R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	L1		DQ18R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	R10		DQ18R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	R9		DQ18R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	M4		DQS18R	DQS19R/CQ19R	DQ19R/CQn19R			
6C	VREF6C	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	M3		DQSn18R	DQSn19R/DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	P8		DQ19R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	P7		DQ19R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	K2		DQS19R	DQ19R/CQn19R	DQ19R			
6C	VREF6C	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	K1		DQSn19R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	N6		DQ19R	DQ19R	DQ19R			
6C	VREF6C	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	N5		DQ19R	DQ19R	DQ19R			
6A	VREF6A	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	H2							
6A	VREF6A	IO			DIFFIO_RX_R33n	DIFFOUT_R65n	J1							
6A	VREF6A	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	P11		DQ20R					

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
6A	VREF6A	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	P10		DQ20R					
6A	VREF6A	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	K4		DQS20R					
6A	VREF6A	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	K3		DQSn20R					
6A	VREF6A	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	M7		DQ20R					
6A	VREF6A	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	M6		DQ20R					
6A	VREF6A	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	G2		DQ21R	DQ24R				
6A	VREF6A	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	H1		DQ21R	DQ24R				
6A	VREF6A	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	L5		DQ21R	DQ24R				
6A	VREF6A	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	L4		DQ21R	DQ24R				
6A	VREF6A	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	J4		DQS21R	DQS24R/CQ24R				
6A	VREF6A	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	J3		DQSn21R	DQSn24R/DQ24R				
6A	VREF6A	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	L7		DQ22R	DQ24R				
6A	VREF6A	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	L6		DQ22R	DQ24R				
6A	VREF6A	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	F1	H2	DQS22R	DQ24R/CQn24R				
6A	VREF6A	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	G1	J1	DQSn22R	DQ24R				
6A	VREF6A	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	N9	K7	DQ22R	DQ24R				
6A	VREF6A	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	N8	K6	DQ22R	DQ24R				
6A	VREF6A	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	H4	G2	DQ23R	DQ25R	DQ26R	DQ23R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	H3	H1	DQ23R	DQ25R	DQ26R	DQ23R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	K6	K5	DQ23R	DQ25R	DQ26R	DQ23R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	K5	K4	DQ23R	DQ25R	DQ26R	DQ23R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	E2	F1	DQS23R	DQS25R/CQ25R	DQ26R	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	E1	G1	DQSn23R	DQSn25R/DQ25R	DQ26R	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	N11	J4	DQ24R	DQ25R	DQ26R	DQ24R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	N10	J3	DQ24R	DQ25R	DQ26R	DQ24R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	F4	E2	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREF6A	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	F3	E1	DQSn24R	DQ25R	DQSn26R/DQ26R	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREF6A	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	J7	L9	DQ24R	DQ25R	DQ26R	DQ24R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J6	L8	DQ24R	DQ25R	DQ26R	DQ24R	DQ25R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	G5	H4	DQ25R	DQ26R	DQ26R	DQ25R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	G4	H3	DQ25R	DQ26R	DQ26R	DQ25R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	K8	K9	DQ25R	DQ26R	DQ26R	DQ25R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	K7	K8	DQ25R	DQ26R	DQ26R	DQ25R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	C1	D2	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREF6A	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	D1	D1	DQSn25R	DQSn26R/DQ26R	DQ26R	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	M10	J6	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	M9	H5	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D3	F4	DQS26R	DQ26R/CQn26R	DQ26R	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREF6A	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	D2	F3	DQSn26R	DQ26R	DQ26R	DQSn26R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	L9	G4	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R
6A	VREF6A	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	L8	G3	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R	DQ26R
6A	VREF6A	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	E4	B1						
6A	VREF6A	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	E3	C1						
6A	VREF6A	IO			DIFFIO_TX_R44p	DIFFOUT_R88p	H6	H6						
6A	VREF6A	IO			DIFFIO_TX_R44n	DIFFOUT_R88n	H5	G5						
		MSEL2		MSEL2			K9	G7						
		MSEL1		MSEL1			J9	J9						
		MSEL0		MSEL0			K10	H8						
		TEMPDIODEn					D4	D4						
		TEMPDIODEp					E5	D3						
		NC					G7	E4						
7A	VREF7A	IO				DIFFOUT_T1n	F8	A2	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREF7A	IO				DIFFOUT_T1p	F6	C3	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREF7A	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	E7	A4	DQSn1T	DQ1T	DQ1T	DQSn1T	DQ1T	DQ1T
7A	VREF7A	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	F7	B4	DQS1T	DQ1T/CQn1T	DQ1T	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREF7A	IO				DIFFOUT_T3n	F9	A3	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREF7A	IO				DIFFOUT_T3p	G8	B2	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	C3	D7	DQSn2T	DQSn1T/DQ1T	DQ1T	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	C4	E7	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREF7A	IO				DIFFOUT_T5n	C6	G8	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
7A	VREF7A	IO				DIFFOUT_T5p	D6	G9	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	B5	E8	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	C5	F8	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T
7A	VREF7A	IO				DIFFOUT_T7n	J11	D6	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREF7A	IO				DIFFOUT_T7p	G9	E5	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	G11	C5	DQSn3T	DQ2T	DQSn1T/DQ1T	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREF7A	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	H11	D5	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREF7A	IO				DIFFOUT_T9n	J12	B5	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREF7A	IO				DIFFOUT_T9p	G10	C6	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A2	A5	DQSn4T	DQSn2T/DQ2T	DQ1T	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	B2	A6	DQS4T	DQS2T/CQ2T	DQ1T	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREF7A	IO				DIFFOUT_T11n	A5	A8	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREF7A	IO				DIFFOUT_T11p	A3	A9	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A4	A7	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREF7A	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B4	B7	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREF7A	IO				DIFFOUT_T13n	D7	B8	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREF7A	IO				DIFFOUT_T13p	E8	F9	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREF7A	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C9	C8	DQSn5T	DQ3T		DQSn5T	DQ3T	
7A	VREF7A	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D9	D8	DQS5T	DQ3T/CQn3T		DQS5T	DQ3T/CQn3T	
7A	VREF7A	IO				DIFFOUT_T15n	E10	D9	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREF7A	IO				DIFFOUT_T15p	D8	C9	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREF7A	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	A7	E10	DQSn6T	DQSn3T/DQ3T		DQSn6T	DQSn3T/DQ3T	
7A	VREF7A	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	B7	F10	DQS6T	DQS3T/CQ3T		DQS6T	DQS3T/CQ3T	
7A	VREF7A	IO				DIFFOUT_T17n	A6	H10	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREF7A	IO				DIFFOUT_T17p	C7	G10	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREF7A	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A8	D10	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREF7A	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B8	E11	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREF7A	IO				DIFFOUT_T19n	M13	H11						
7A	VREF7A	IO				DIFFOUT_T19p	L13	J10						
7A	VREF7A	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	K11	J11						
7A	VREF7A	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	K12	J12						
7B	VREF7B	IO				DIFFOUT_T21n	G12		DQ7T	DQ7T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T21p	F11		DQ7T	DQ7T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	F12		DQSn7T	DQ7T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	F13		DQS7T	DQ7T/CQn7T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T23n	G13		DQ7T	DQ7T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T23p	E11		DQ7T	DQ7T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	C11		DQSn8T	DQSn7T/DQ7T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	D11		DQS8T	DQS7T/CQ7T	DQ7T/CQn7T			
7B	VREF7B	IO				DIFFOUT_T25n	D13		DQ8T	DQ7T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T25p	D10		DQ8T	DQ7T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C12		DQ8T	DQ7T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D12		DQ8T	DQ7T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T27n	K14		DQ9T	DQ8T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T27p	K13		DQ9T	DQ8T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	H14		DQSn9T	DQ8T	DQSn7T/DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	J14		DQS9T	DQ8T/CQn8T	DQS7T/CQ7T			
7B	VREF7B	IO				DIFFOUT_T29n	K15		DQ9T	DQ8T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T29p	L14		DQ9T	DQ8T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	A10		DQSn10T	DQSn8T/DQ8T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	B10		DQS10T	DQS8T/CQ8T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T31n	A12		DQ10T	DQ8T	DQ7T			
7B	VREF7B	IO				DIFFOUT_T31p	A9		DQ10T	DQ8T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	A11		DQ10T	DQ8T	DQ7T			
7B	VREF7B	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	B11		DQ10T	DQ8T	DQ7T			
7C	VREF7C	IO				DIFFOUT_T33n	D14	B10	DQ11T	DQ11T		DQ11T	DQ11T	
7C	VREF7C	IO				DIFFOUT_T33p	E13	C10	DQ11T	DQ11T		DQ11T	DQ11T	
7C	VREF7C	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	E14	A10	DQSn11T	DQ11T		DQSn11T	DQ11T	
7C	VREF7C	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	F14	B11	DQS11T	DQ11T/CQn11T		DQS11T	DQ11T/CQn11T	
7C	VREF7C	IO				DIFFOUT_T35n	F15	A11	DQ11T	DQ11T		DQ11T	DQ11T	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
7C	VREF7C	IO				DIFFOUT_T35p	D15	A12	DQ11T	DQ11T		DQ11T	DQ11T	
7C	VREF7C	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	A13	C12	DQSn12T	DQSn11T/DQ11T		DQSn12T	DQSn11T/DQ11T	
7C	VREF7C	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	B13	D11	DQS12T	DQS11T/CQ11T		DQS12T	DQS11T/CQ11T	
7C	VREF7C	IO				DIFFOUT_T37n	A15	E13	DQ12T	DQ11T		DQ12T	DQ11T	
7C	VREF7C	IO				DIFFOUT_T37p	C14	D13	DQ12T	DQ11T		DQ12T	DQ11T	
7C	VREF7C	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	A14	C13	DQ12T	DQ11T		DQ12T	DQ11T	
7C	VREF7C	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	B14	D12	DQ12T	DQ11T		DQ12T	DQ11T	
7C	VREF7C	IO				DIFFOUT_T39n	C17	G12	DQ13T			DQ13T		
7C	VREF7C	IO				DIFFOUT_T39p	C15	F12	DQ13T			DQ13T		
7C	VREF7C	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	C16	F13	DQSn13T			DQSn13T		
7C	VREF7C	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	D16	G13	DQS13T			DQS13T		
7C	VREF7C	IO				DIFFOUT_T41n	D17	H14	DQ13T			DQ13T		
7C	VREF7C	IO				DIFFOUT_T41p	E17	J14	DQ13T			DQ13T		
7C	VREF7C	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	J16	A13						
7C	VREF7C	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	J15	B13						
7C	VREF7C	IO	PLL_T2_CLKOUT4			DIFFOUT_T43n	L16							
7C	VREF7C	IO	PLL_T2_CLKOUT3			DIFFOUT_T43p	K16							
7C	VREF7C	IO			DIFFIO_RX_T22n	DIFFOUT_T44n	G16							
7C	VREF7C	IO			DIFFIO_RX_T22p	DIFFOUT_T44p	H16							
7C	VREF7C	IO	PLL_T2_CLKOUT0n			DIFFOUT_T45n	K17							
7C	VREF7C	IO	PLL_T2_CLKOUT0p			DIFFOUT_T45p	L17							
7C	VREF7C	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T23n	DIFFOUT_T46n	E16							
7C	VREF7C	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T23p	DIFFOUT_T46p	F16							
7C	VREF7C	IO	CLK13n			DIFFOUT_T47n	A16	A14						
7C	VREF7C	IO	CLK13p			DIFFOUT_T47p	B16	B14						
7C	VREF7C	IO	CLK12n		DIFFIO_RX_T24n	DIFFOUT_T48n	A17	C14						
7C	VREF7C	IO	CLK12p		DIFFIO_RX_T24p	DIFFOUT_T48p	B17	D14						
		VCC_CLKIN7C					H17	F14						
		VCCA_PLL_T2					G17							
		VCCD_PLL_T2					J17							
		VCCD_PLL_T1					J18	G15						
		VCCA_PLL_T1					G18	F15						
		VCC_CLKIN8C					K18	F16						
8C	VREF8C	IO	CLK14p		DIFFIO_RX_T25p	DIFFOUT_T49p	B19	D15						
8C	VREF8C	IO	CLK14n		DIFFIO_RX_T25n	DIFFOUT_T49n	A19	C15						
8C	VREF8C	IO	CLK15p			DIFFOUT_T50p	B20	B16						
8C	VREF8C	IO	CLK15n			DIFFOUT_T50n	A20	A15						
8C	VREF8C	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T26p	DIFFOUT_T51p	D18	B17						
8C	VREF8C	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T26n	DIFFOUT_T51n	C18	A16						
8C	VREF8C	IO	PLL_T1_CLKOUT0p			DIFFOUT_T52p	K19	J16						
8C	VREF8C	IO	PLL_T1_CLKOUT0n			DIFFOUT_T52n	J19	J15						
8C	VREF8C	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	D19	E16						
8C	VREF8C	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	C19	D16						
8C	VREF8C	IO	PLL_T1_CLKOUT3			DIFFOUT_T54p	L19	G16						
8C	VREF8C	IO	PLL_T1_CLKOUT4			DIFFOUT_T54n	L20	H16						
8C	VREF8C	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	F19							
8C	VREF8C	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	E19							
8C	VREF8C	IO				DIFFOUT_T56p	C20		DQ14T					
8C	VREF8C	IO				DIFFOUT_T56n	D20		DQ14T					
8C	VREF8C	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	D21		DQS14T					
8C	VREF8C	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	C21		DQSn14T					
8C	VREF8C	IO				DIFFOUT_T58p	D22		DQ14T					
8C	VREF8C	IO				DIFFOUT_T58n	E22		DQ14T					
8C	VREF8C	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	G20	B19	DQ15T	DQ16T		DQ15T	DQ16T	
8C	VREF8C	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	F20	A19	DQ15T	DQ16T		DQ15T	DQ16T	
8C	VREF8C	IO				DIFFOUT_T60p	E20	A17	DQ15T	DQ16T		DQ15T	DQ16T	
8C	VREF8C	IO				DIFFOUT_T60n	H20	A18	DQ15T	DQ16T		DQ15T	DQ16T	
8C	VREF8C	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	G21	C19	DQS15T	DQS16T/CQ16T		DQS15T	DQS16T/CQ16T	
8C	VREF8C	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	F21	C18	DQSn15T	DQSn16T/DQ16T		DQSn15T	DQSn16T/DQ16T	
8C	VREF8C	IO				DIFFOUT_T62p	A22	F17	DQ16T	DQ16T		DQ16T	DQ16T	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
8C	VREF8C	IO				DIFFOUT_T62n	A21	C17	DQ16T	DQ16T		DQ16T	DQ16T	
8C	VREF8C	IO			DIFFIO_RX_T32p	DIFFOUT_T63p	B23	E17	DQS16T	DQ16T/CQn16T		DQS16T	DQ16T/CQn16T	
8C	VREF8C	IO			DIFFIO_RX_T32n	DIFFOUT_T63n	A23	D17	DQSn16T	DQ16T		DQSn16T	DQ16T	
8C	VREF8C	IO				DIFFOUT_T64p	B22	D18	DQ16T	DQ16T		DQ16T	DQ16T	
8C	VREF8C	IO				DIFFOUT_T64n	C23	F18	DQ16T	DQ16T		DQ16T	DQ16T	
8B	VREF8B	IO			DIFFIO_RX_T33p	DIFFOUT_T65p	B25		DQ17T	DQ19T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T33n	DIFFOUT_T65n	A25		DQ17T	DQ19T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T66p	A24		DQ17T	DQ19T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T66n	A26		DQ17T	DQ19T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T34p	DIFFOUT_T67p	C26		DQS17T	DQS19T/CQ19T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T34n	DIFFOUT_T67n	B26		DQSn17T	DQSn19T/DQ19T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T68p	K20		DQ18T	DQ19T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T68n	J20		DQ18T	DQ19T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	J22		DQS18T	DQ19T/CQn19T	DQS20T/CQ20T			
8B	VREF8B	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	J21		DQSn18T	DQ19T	DQSn20T/DQ20T			
8B	VREF8B	IO				DIFFOUT_T70p	K21		DQ18T	DQ19T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T70n	K22		DQ18T	DQ19T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	D25		DQ19T	DQ20T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	D24		DQ19T	DQ20T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T72p	C24		DQ19T	DQ20T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T72n	E25		DQ19T	DQ20T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	E23		DQS19T	DQS20T/CQ20T	DQ20T/CQn20T			
8B	VREF8B	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	D23		DQSn19T	DQSn20T/DQ20T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T74p	A27		DQ20T	DQ20T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T74n	C27		DQ20T	DQ20T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	B28		DQS20T	DQ20T/CQn20T	DQ20T			
8B	VREF8B	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	A28		DQSn20T	DQ20T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T76p	C28		DQ20T	DQ20T	DQ20T			
8B	VREF8B	IO				DIFFOUT_T76n	A29		DQ20T	DQ20T	DQ20T			
8A	VREF8A	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	M23	G18						
8A	VREF8A	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	L23	F19						
8A	VREF8A	IO				DIFFOUT_T78p	L22	J18						
8A	VREF8A	IO				DIFFOUT_T78n	K23	J19						
8A	VREF8A	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	G23	B20	DQ21T	DQ24T		DQ21T	DQ24T	
8A	VREF8A	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	F23	A21	DQ21T	DQ24T		DQ21T	DQ24T	
8A	VREF8A	IO				DIFFOUT_T80p	F22	A20	DQ21T	DQ24T		DQ21T	DQ24T	
8A	VREF8A	IO				DIFFOUT_T80n	H23	D19	DQ21T	DQ24T		DQ21T	DQ24T	
8A	VREF8A	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	G24	D20	DQS21T	DQS24T/CQ24T		DQS21T	DQS24T/CQ24T	
8A	VREF8A	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	F24	C20	DQSn21T	DQSn24T/DQ24T		DQSn21T	DQSn24T/DQ24T	
8A	VREF8A	IO				DIFFOUT_T82p	F25	D21	DQ22T	DQ24T		DQ22T	DQ24T	
8A	VREF8A	IO				DIFFOUT_T82n	D27	C21	DQ22T	DQ24T		DQ22T	DQ24T	
8A	VREF8A	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	E26	B22	DQS22T	DQ24T/CQn24T		DQS22T	DQ24T/CQn24T	
8A	VREF8A	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	D26	A22	DQSn22T	DQ24T		DQSn22T	DQ24T	
8A	VREF8A	IO				DIFFOUT_T84p	F26	A23	DQ22T	DQ24T		DQ22T	DQ24T	
8A	VREF8A	IO				DIFFOUT_T84n	D28	B23	DQ22T	DQ24T		DQ22T	DQ24T	
8A	VREF8A	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	B31	B25	DQ23T	DQ25T	DQ26T	DQ23T	DQ25T	DQ26T
8A	VREF8A	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	A31	A26	DQ23T	DQ25T	DQ26T	DQ23T	DQ25T	DQ26T
8A	VREF8A	IO				DIFFOUT_T86p	A30	A24	DQ23T	DQ25T	DQ26T	DQ23T	DQ25T	DQ26T
8A	VREF8A	IO				DIFFOUT_T86n	A33	A25	DQ23T	DQ25T	DQ26T	DQ23T	DQ25T	DQ26T
8A	VREF8A	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	B32	B26	DQS23T	DQS25T/CQ25T	DQ26T	DQS23T	DQS25T/CQ25T	DQ26T
8A	VREF8A	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	A32	A27	DQSn23T	DQSn25T/DQ25T	DQ26T	DQSn23T	DQSn25T/DQ25T	DQ26T
8A	VREF8A	IO				DIFFOUT_T88p	C29	F20	DQ24T	DQ25T	DQ26T	DQ24T	DQ25T	DQ26T
8A	VREF8A	IO				DIFFOUT_T88n	B29	E20	DQ24T	DQ25T	DQ26T	DQ24T	DQ25T	DQ26T
8A	VREF8A	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	D30	H20	DQS24T	DQ25T/CQn25T	DQS26T/CQ26T	DQS24T	DQ25T/CQn25T	DQS26T/CQ26T
8A	VREF8A	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	C30	G20	DQSn24T	DQ25T	DQSn26T/DQ26T	DQSn24T	DQ25T	DQSn26T/DQ26T
8A	VREF8A	IO				DIFFOUT_T90p	C31	H19	DQ24T	DQ25T	DQ26T	DQ24T	DQ25T	DQ26T
8A	VREF8A	IO				DIFFOUT_T90n	D31	J20	DQ24T	DQ25T	DQ26T	DQ24T	DQ25T	DQ26T
8A	VREF8A	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	F28	D23	DQ25T	DQ26T	DQ26T	DQ25T	DQ26T	DQ26T
8A	VREF8A	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	E28	C23	DQ25T	DQ26T	DQ26T	DQ25T	DQ26T	DQ26T
8A	VREF8A	IO				DIFFOUT_T92p	F27	D22	DQ25T	DQ26T	DQ26T	DQ25T	DQ26T	DQ26T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
8A	VREF8A	IO				DIFFOUT_T92n	G27	D25	DQ25T	DQ26T	DQ26T	DQ25T	DQ26T	DQ26T
8A	VREF8A	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	F29	D24	DQS25T	DQS26T/CQ26T	DQ26T/CQn26T	DQS25T	DQS26T/CQ26T	DQ26T/CQn26T
8A	VREF8A	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	E29	C24	DQSn25T	DQSn26T/DQ26T	DQ26T	DQSn25T	DQSn26T/DQ26T	DQ26T
8A	VREF8A	IO				DIFFOUT_T94p	J24	F21	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T
8A	VREF8A	IO				DIFFOUT_T94n	K24	G21	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T
8A	VREF8A	IO	RUP8A		DIFFIO_RX_T48p	DIFFOUT_T95p	H26	F22	DQS26T	DQ26T/CQn26T	DQ26T	DQS26T	DQ26T/CQn26T	DQ26T
8A	VREF8A	IO	RDN8A		DIFFIO_RX_T48n	DIFFOUT_T95n	G26	E22	DQSn26T	DQ26T	DQ26T	DQSn26T	DQ26T	DQ26T
8A	VREF8A	IO				DIFFOUT_T96p	J25	E23	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T
8A	VREF8A	IO				DIFFOUT_T96n	K25	G22	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T	DQ26T
		VCCIO1A					L26	H23						
		VCCIO1A					N28	H26						
		VCCIO1A					H29	E26						
		VCCIO1A					G32							
		VCCIO1A					B34							
		VCCIO1C					M32	P26						
		VCCIO1C					V30	R23						
		VCCIO1C					U34							
		VCCIO1C					T31							
		VCCIO2C					W25	T26						
		VCCIO2C					AD32	V22						
		VCCIO2C					W29							
		VCCIO2C					W32							
		VCCIO2A					AB28	AD26						
		VCCIO2A					AN34	AA22						
		VCCIO2A					AH32	W26						
		VCCIO2A					AG28							
		VCCIO2A					AD25							
		VCCIO3A					AM27	AC22						
		VCCIO3A					AL30	AF22						
		VCCIO3A					AJ25	AF25						
		VCCIO3A					AF25	AC18						
		VCCIO3B					AF22							
		VCCIO3B					AM25							
		VCCIO3C					AH21	AC15						
		VCCIO3C					AM20	AF18						
		VCCIO3C					AJ18							
		VCCIO4C					AG16	AB12						
		VCCIO4C					AP17	AF13						
		VCCIO4C					AM13							
		VCCIO4B					AH13							
		VCCIO4B					AM10							
		VCCIO4A					AF12	AD10						
		VCCIO4A					AM3	AF4						
		VCCIO4A					AL6	AF7						
		VCCIO4A					AH10	AC6						
		VCCIO5A					AD9	AD3						
		VCCIO5A					AN1	AA3						
		VCCIO5A					AH3	AA7						
		VCCIO5A					AG6							
		VCCIO5A					AB7							
		VCCIO5C					W4	R3						
		VCCIO5C					AC3	P6						
		VCCIO5C					V1							
		VCCIO5C					U5							
		VCCIO6C					T10	L7						
		VCCIO6C					T3	N3						
		VCCIO6C					T6							
		VCCIO6C					L3							
		VCCIO6A					L10	K3						
		VCCIO6A					N7	H7						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
		VCCIO6A					H7	E3						
		VCCIO6A					G3							
		VCCIO6A					B1							
		VCCIO7A					F10	F11						
		VCCIO7A					J10	F7						
		VCCIO7A					D5	C4						
		VCCIO7A					C8	C7						
		VCCIO7B					C10							
		VCCIO7B					J13							
		VCCIO7C					C13	C11						
		VCCIO7C					G14	G14						
		VCCIO7C					F17							
		VCCIO8C					C22	C16						
		VCCIO8C					H19	G17						
		VCCIO8C					A18							
		VCCIO8B					C25							
		VCCIO8B					G22							
		VCCIO8A					C32	C22						
		VCCIO8A					J23	F23						
		VCCIO8A					G25	E19						
		VCCIO8A					D29	C25						
		VCCL					U17	R15						
		VCCL					AB14	N17						
		VCCL					AB22	V14						
		VCCL					AA13	V18						
		VCCL					AA15	U11						
		VCCL					AA17	U13						
		VCCL					AA19	U15						
		VCCL					AA21	U17						
		VCCL					Y14	T12						
		VCCL					Y16	T14						
		VCCL					Y18	T16						
		VCCL					Y20	R13						
		VCCL					W15	R17						
		VCCL					W17	P12						
		VCCL					W19	P14						
		VCCL					W21	P16						
		VCCL					V14	P18						
		VCCL					V16	N13						
		VCCL					V18	N15						
		VCCL					V20	M12						
		VCCL					U15	M14						
		VCCL					U19	M16						
		VCCL					U21	L11						
		VCCL					T14	L17						
		VCCL					T16							
		VCCL					T18							
		VCCL					T20							
		VCCL					R15							
		VCCL					R17							
		VCCL					R19							
		VCCL					R21							
		VCCL					P14							
		VCCL					P16							
		VCCL					P18							
		VCCL					P20							
		VCCL					P22							
		VCCL					N13							
		VCCL					N21							
		VCC					N19	M18						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
		VCC					AB16	V12						
		VCC					AB18	V16						
		VCC					AB20	T18						
		VCC					Y22	R11						
		VCC					W13	N11						
		VCC					V22	L13						
		VCC					U13	L15						
		VCC					T22							
		VCC					R13							
		VCC					N15							
		VCC					N17							
		GND					V17	R14						
		DNU					U18	P15						
		GND					E21	K11						
		GND					AN2	B27						
		GND					AN5	AG2						
		GND					AN8	AG5						
		GND					AN11	AG8						
		GND					AN14	AG11						
		GND					AN17	AG14						
		GND					AN20	AG17						
		GND					AN23	AG20						
		GND					AN26	AG23						
		GND					AN29	AG26						
		GND					AN32	AF27						
		GND					AM33	AD2						
		GND					AK2	AD5						
		GND					AK5	AD8						
		GND					AK8	AD11						
		GND					AK11	AD14						
		GND					AK14	AD17						
		GND					AK17	AD20						
		GND					AK20	AD23						
		GND					AK23	AC24						
		GND					AK26	AC27						
		GND					AK29	AA2						
		GND					AJ30	AA5						
		GND					AJ33	AA8						
		GND					AG2	AA11						
		GND					AG5	AA14						
		GND					AG8	AA17						
		GND					AG11	AA20						
		GND					AG14	Y12						
		GND					AG17	Y16						
		GND					AG20	Y21						
		GND					AG23	Y24						
		GND					AG26	Y27						
		GND					AF27	W12						
		GND					AF30	W14						
		GND					AF33	W16						
		GND					AD2	W18						
		GND					AD5	V2						
		GND					AD8	V5						
		GND					AD11	V8						
		GND					AD14	V11						
		GND					AD17	V13						
		GND					AD20	V15						
		GND					AD23	V17						
		GND					AC14	V19						
		GND					AC16	U10						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
		GND					AC18	U12						
		GND					AC20	U14						
		GND					AC24	U16						
		GND					AC27	U18						
		GND					AC30	U21						
		GND					AC33	U24						
		GND					AB13	U27						
		GND					AB15	T11						
		GND					AB17	T13						
		GND					AB19	T15						
		GND					AB21	T17						
		GND					AB23	T19						
		GND					AA2	R2						
		GND					AA5	R5						
		GND					AA8	R8						
		GND					AA11	R12						
		GND					AA14	R16						
		GND					AA16	R18						
		GND					AA18	P11						
		GND					AA20	P13						
		GND					AA22	P17						
		GND					Y13	P21						
		GND					Y15	P24						
		GND					Y17	P27						
		GND					Y19	N10						
		GND					Y21	N12						
		GND					Y24	N14						
		GND					Y27	N16						
		GND					Y30	N18						
		GND					Y33	M2						
		GND					W14	M5						
		GND					W16	M8						
		GND					W18	M11						
		GND					W20	M13						
		GND					W22	M15						
		GND					V2	M17						
		GND					V5	M19						
		GND					V8	L10						
		GND					V11	L12						
		GND					V12	L14						
		GND					V13	L16						
		GND					V15	L18						
		GND					V19	L21						
		GND					V21	L24						
		GND					V23	L27						
		GND					U12	K13						
		GND					U14	K15						
		GND					U16	K17						
		GND					U20	K19						
		GND					U22	J2						
		GND					U23	J5						
		GND					U24	J8						
		GND					U27	J13						
		GND					U30	J17						
		GND					U33	H9						
		GND					T13	H12						
		GND					T15	H15						
		GND					T17	H18						
		GND					T19	H21						
		GND					T21	H24						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
		GND					R2	H27						
		GND					R5	F2						
		GND					R8	F5						
		GND					R11	E6						
		GND					R14	E9						
		GND					R16	E12						
		GND					R18	E15						
		GND					R20	E18						
		GND					R22	E21						
		GND					P13	E24						
		GND					P15	E27						
		GND					P17	C2						
		GND					P19	B3						
		GND					P21	B6						
		GND					P24	B9						
		GND					P27	B12						
		GND					P30	B15						
		GND					P33	B18						
		GND					N12	B21						
		GND					N14	B24						
		GND					N16							
		GND					N18							
		GND					N20							
		GND					N22							
		GND					M2							
		GND					M5							
		GND					M8							
		GND					M11							
		GND					M15							
		GND					M17							
		GND					M19							
		GND					M21							
		GND					L12							
		GND					L15							
		GND					L18							
		GND					L21							
		GND					L24							
		GND					L27							
		GND					L30							
		GND					L33							
		GND					J2							
		GND					J5							
		GND					J8							
		GND					H9							
		GND					H12							
		GND					H15							
		GND					H18							
		GND					H21							
		GND					H24							
		GND					H27							
		GND					H30							
		GND					H33							
		GND					F2							
		GND					F5							
		GND					E6							
		GND					E9							
		GND					E12							
		GND					E15							
		GND					E18							
		GND					E24							

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
		GND					E27							
		GND					E30							
		GND					E33							
		GND					C2							
		GND					B3							
		GND					B6							
		GND					B9							
		GND					B12							
		GND					B15							
		GND					B18							
		GND					B21							
		GND					B24							
		GND					B27							
		GND					B30							
		GND					B33							
		VCCPD1A					N23	L19						
		VCCPD1C					R23	N19						
		VCCPD2C					W23	R19						
		VCCPD2A					AA23	U19						
		VCCPD3A					AC23	W17						
		VCCPD3B					AC21							
		VCCPD3C					AC19	W15						
		VCCPD4C					AC17	W13						
		VCCPD4B					AC15							
		VCCPD4A					AC13	W11						
		VCCPD5A					AB12	V10						
		VCCPD5C					Y12	T10						
		VCCPD6C					T12	P10						
		VCCPD6A					P12	M10						
		VCCPD7A					M12	K12						
		VCCPD7B					M14							
		VCCPD7C					M16	K14						
		VCCPD8C					M18	K16						
		VCCPD8B					M20							
		VCCPD8A					M22	K18						
	VREF1A	VREF1A	VREF1A				J26	K22						
	VREF1C	VREF1C	VREF1C				P26	N22						
	VREF2C	VREF2C	VREF2C				V27	U22						
	VREF2A	VREF2A	VREF2A				AA26	Y22						
	VREF3A	VREF3A	VREF3A				AG25	AB18						
	VREF3B	VREF3B	VREF3B				AG22							
	VREF3C	VREF3C	VREF3C				AH20	AA16						
	VREF4C	VREF4C	VREF4C				AH16	AA12						
	VREF4B	VREF4B	VREF4B				AG13							
	VREF4A	VREF4A	VREF4A				AG10	AB10						
	VREF5A	VREF5A	VREF5A				AF7	W7						
	VREF5C	VREF5C	VREF5C				AA9	T7						
	VREF6C	VREF6C	VREF6C				U8	M7						
	VREF6A	VREF6A	VREF6A				P9	J7						
	VREF7A	VREF7A	VREF7A				H10	G11						
	VREF7B	VREF7B	VREF7B				H13							
	VREF7C	VREF7C	VREF7C				G15	H13						
	VREF8C	VREF8C	VREF8C				G19	H17						
	VREF8B	VREF8B	VREF8B				H22							
	VREF8A	VREF8A	VREF8A				H25	G19						
		VCCPT					J27	G23						
		VCCPT					U29	R24						
		VCCPT					AG27	AC23						
		VCCPT					AJ17	AD15						
		VCCPT					AG7	AB6						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	F780	DQS for X4 for F1152	DQS for X8/X9 for F1152 (Note 1)	DQS for 16/X18 for F1152 (Note 1)	DQS for X4 for F780	DQS for X8/X9 for F780 (Note 1)	DQS for 16/X18 for F780 (Note 1)
		VCCPT					V6	P5						
		VCCPT					H8	G6						
		VCCPT					F18	E14						
		VCCPGM					AD24	AA21						
		VCCPGM					AD10	Y8						
		VCCBAT					G6	F6						
		NC					AK30	AE25						
		NC					AC10	V9						
		NC					M25	U20						
		NC					L11	M9						
		NC					L25	L20						
		NC					K26	K10						
		NC						J21						

Note:
(1) When not used as clocks, the CQn and DQSn pins can be used as DQ pins.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Supply and Reference Pins
VCCL	Power	VCCL supplies power to the core voltage power supply pins.
VCC	Power	VCC supplies power to the peripheral circuitry.
RUP[1..8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1..8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
VCCIO[1..8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0-V PCI/PCI-X I/O, and LVTTL(3.0 V, 3.3 V) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V), 3.0-V PCI/PCI-X and LVTTL(3.0 V, 3.3 V) I/O standards.
VREF[1..8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, these pins are used as the voltage-referenced pins for the bank.
VCCA_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Analog power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must connect these pins to 2.5 V, even if the PLL is not used. You are advised to keep this pin isolated from other VCC for better jitter performance.
VCCD_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Digital power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must connect these pins to 1.1 V, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology. Connect to 2.5 V.
VCCPGM	Power	Power supply for configuration pins. Can be connected to 1.8 V, 2.5 V, 3.0 V, or 3.3 V depending on the particular design.
VCCPD[1..8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.3 V, 3.0 V, or 2.5 V. VCCPD for 3.3-V I/O standard is 3.3 V, VCCPD for 3.0-V I/O standard is 3.0 V, and VCCPD for 2.5-V/1.8-V/1.2-V I/O standards is 2.5 V.
VCCBAT	Power	Battery back-up power supply for design security volatile key register. Connect to 2.5 V.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O banks. Connect to 2.5 V.
GND	Ground	Device ground pins.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3V) turns off the weak pull-up, while a logic low turns them on.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the Stratix III device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the Stratix III device.
MSEL[3..0]	Input	Configuration input pins that set the Stratix III device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V,3.0 V, 3.3 V) selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin. Connect TCK to GND if the JTAG circuitry is not used.
TMS	Input	Dedicated JTAG input pin. Connect TMS to VCCPD if the JTAG circuitry is not used.
TDI	Input	Dedicated JTAG input pin. Connect TDI to VCCPD if the JTAG circuitry is not used.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Clock and PLL Pins		
CLK[1,3,8,10]p	Clock, Input	Dedicated high-speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4..7,12..15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4..7,12..15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for dfferential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L2,L3,R2,R3]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single-ended I/O or one differential I/O pair. When using both pins as single-ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L2,L3,R2,R3]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual-purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.

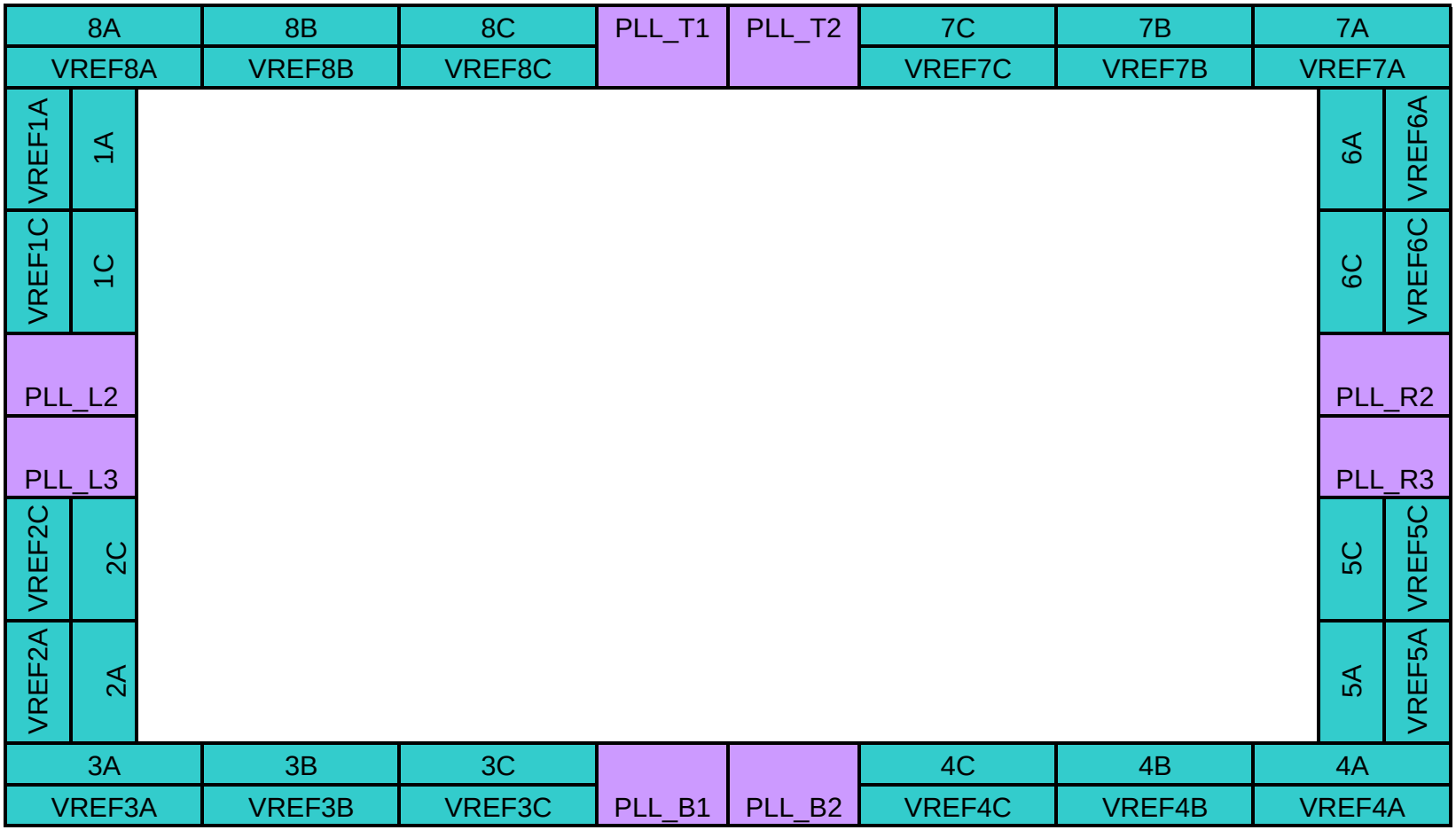
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock ouput pins.
PLL_[T1,T2,B1,B2]_CLKOUT0[p,n]	I/O, Clock	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.
Optional/Dual-Purpose Configuration Pins		
nCSO	I/O Output	Dedicated output control signal from the Stratix III FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	I/O Output	Control signal from the Stratix III FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration modes, DCLK is used to clock configuration data from an external source into the Stratix III device. In AS mode, DCLK is an output from the Stratix III device that provides timing for the configuration interface.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[7..0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[1..44][T,B], DQS[1..40][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
DQSn[1..44][T,B], DQSn[1..40][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase-shift circuitry.
DQ[1..44][T,B],DQ[1..40][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1..44][T,B], CQ[1..40][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1..44][T,B], CQ[1..40][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, EP3SL340. Refer to the pin list for the availability of pins in each density.

(2) Some of the pull-up or pull-down resistors mentioned in the table above may not be required, depending on the exact device configuration scheme. Should you be required to use a different configuration scheme, the ability to NC or short them may be valuable during the debug phase. Refer to the *Configuring Stratix III Devices* chapter in the *Stratix III Device Handbook* for more information.



Note:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	11/16/2007	Initial release.
1.1	4/11/2008	Updated naming convention of x4 DQ/DQS group to match pin planner in Quartus II software and ORCAD symbol files.