Pin Information for the Stratix® IV E EP4SE230 Device
Version 1.2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
1A		TDI		TDI			F24	No			
1A		TMS		TMS			H22	No			
1A		TRST		TRST			D26	No			
1A		TCK		TCK			C26	No			
1A		TDO		TDO			G24	No			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	F26	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	F25	Yes			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C28	Yes			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G26	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G25	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	Yes	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C27	Yes	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	H25	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	J24	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	D28	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E28	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	J23	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J22	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	F28	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	F27	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K21	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K20	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	G28	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G27	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K26	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K25	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25	Yes	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	K24	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	K23	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	H28	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	J27	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	L23	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L22	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	J28	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	K27	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	M23	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	M22	Yes			
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	L26	Yes	DQSn8L		
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	L25	Yes	DQS8L		
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	M21	Yes	DQ8L		
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	M20	Yes	DQ8L		
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	K28	Yes	DQ8L		
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	L28	Yes	DQ8L		
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	N21	Yes	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	N20	Yes	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	M26	Yes	DQSn9L	DQ8L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	M25	Yes	DQS9L	DQ8L/CQn8L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	N25	Yes	DQ9L	DQ8L	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	M24	Yes	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	M28	Yes	DQSn10L	DQSn8L/DQ8L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	M27	Yes	DQS10L	DQS8L/CQ8L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	N23	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	P23	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	P25	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	N24	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	P20	No			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	P19	No			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	N27	No			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	N26	No			
1C	VREFB1CN0	CLK1n	CLK1n				N28	No			
1C	VREFB1CN0	CLK1p	CLK1p				P28	No			
2C	VREFB2CN0	CLK3p	CLK3p				R27	No			
2C	VREFB2CN0	CLK3n	CLK3n				R28	No			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	U28	No			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	T28	No			
2C	VREFB2CN0	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	R20	No			
2C	VREFB2CN0	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	R21	No			
2C	VREFB2CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	R26	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	T27	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	T25	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	R25	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	V27	Yes	DQS17L	DQS19L/CQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	V28	Yes	DQSn17L	DQSn19L/DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	T20	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	T21	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	V26	Yes	DQS18L	DQ19L/CQn19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	U26	Yes	DQSn18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	T24	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	U25	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	W27	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	W28	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	T22	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	T23	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	V24	Yes	DQS19L		
2C	VREFB2CN0	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	V25	Yes	DQSn19L		
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	V23	Yes			
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	U23	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AA27	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	Y28	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	W22	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	W23	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AB27	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AA28	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	W24	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	W25	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	Y25	Yes	DQS23L	DQS25L/CQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	Y26	Yes	DQSn23L	DQSn25L/DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	V20	Yes	DQ24L	DQ25L	DQ26L

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	V21	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AC28	Yes	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AB28	Yes	DQSn24L	DQ25L	DQSn26L/DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AA25	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AA26	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AB25	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AB26	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AC25	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AC26	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AD27	Yes	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AD28	Yes	DQSn25L	DQSn26L/DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	W20	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	W21	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AG28	Yes	DQS26L	DQ26L/CQn26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AF28	Yes	DQSn26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	Y23	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AA24	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AE27	Yes			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AE28	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L44p	DIFFOUT_L88p	AA23	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L44n	DIFFOUT_L88n	AB24	Yes			
		nCONFIG		nCONFIG			W19	No			
		nSTATUS		nSTATUS			AD25	No			
		CONF_DONE		CONF_DONE			AE26	No			
		PORSEL					AB23	No			
		nCE		nCE			Y20	No			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AF26	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AH27	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AH25	Yes	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AG25	Yes	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AG27	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AH26	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE22	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD22	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AB20	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AB21	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AD21	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AC21	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AD24	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AE23	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AF24	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AE24	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AF23	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AG24	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH24	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH23	Yes	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AH20	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AH21	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AH22	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AG22	Yes	DQ4B	DQ2B	DQ1B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
3A	VREFB3AN0	IO				DIFFOUT_B13n	AC20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AG21	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21	Yes	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21	Yes	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AF20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AE20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AD19	Yes	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AC19	Yes	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AB19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AA19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD18	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	Y19	Yes			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AA18	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y18	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y17	Yes			
3C	VREFB3CN0	IO				DIFFOUT_B33n	AF19	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B33p	AG19	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AH19	Yes	DQSn11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AG18	Yes	DQS11B	DQ11B/CQn11B	
3C	VREFB3CN0	IO				DIFFOUT_B35n	AH17	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B35p	AH18	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AF17	Yes	DQSn12B	DQSn11B/DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AE18	Yes	DQS12B	DQS11B/CQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37n	AE16	Yes	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37p	AD16	Yes	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AF16	Yes	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AE17	Yes	DQ12B	DQ11B	
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B43n	AC17	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B43p	AB17	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AC16	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AB16	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B45n	AA15	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B45p	Y15	No			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B23n	DIFFOUT_B46n	AH16	No			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B23p	DIFFOUT_B46p	AG16	No			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B47n	AH15	No			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B47p	AG15	No			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B24n	DIFFOUT_B48n	AF15	No			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B24p	DIFFOUT_B48p	AE15	No			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B25p	DIFFOUT_B49p	AE14	No			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B25n	DIFFOUT_B49n	AF14	No			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B50p	AG13	No			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B50n	AH14	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AG12	Yes			
4C	VREFB4CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AH13	Yes			
4C	VREFB4CN0	IO				DIFFOUT_B56p	Y13	Yes	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B56n	Y14	Yes	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AD13	Yes	DQS14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AE13	Yes	DQSn14B		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
4C	VREFB4CN0	IO				DIFFOUT_B58p	AA13	Yes	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B58n	AB13	Yes	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AG10	Yes	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AH10	Yes	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60p	AH11	Yes	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60n	AH12	Yes	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AF10	Yes	DQS15B	DQS16B/CQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AF11	Yes	DQSn15B	DQSn16B/DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62p	AF12	Yes	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62n	AC12	Yes	DQ16B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32p	DIFFOUT_B63p	AD12	Yes	DQS16B	DQ16B/CQn16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32n	DIFFOUT_B63n	AE12	Yes	DQSn16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64p	AC11	Yes	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64n	AE11	Yes	DQ16B	DQ16B	
4A	VREFB4AN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AB11	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AC10	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B78p	Y10	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B78n	Y11	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AG9	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AH8	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80p	AE10	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80n	AH9	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AE9	Yes	DQS21B	DQS24B/CQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AF9	Yes	DQSn21B	DQSn24B/DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82p	AF8	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82n	AE8	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AG7	Yes	DQS22B	DQ24B/CQn24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AH7	Yes	DQSn22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84p	AG6	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84n	AH6	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AG4	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AH3	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86p	AH4	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86n	AH5	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AG3	Yes	DQS23B	DQS25B/CQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AH2	Yes	DQSn23B	DQSn25B/DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88p	AD9	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88n	AC9	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AA9	Yes	DQS24B	DQ25B/CQn25B	DQS26B/CQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AB9	Yes	DQSn24B	DQ25B	DQSn26B/DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90p	Y9	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90n	AA10	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AE6	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AF6	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92p	AE4	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92n	AE7	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AE5	Yes	DQS25B	DQS26B/CQ26B	DQ26B/CQn26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AF5	Yes	DQSn25B	DQSn26B/DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94p	AB8	Yes	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94n	AC8	Yes	DQ26B	DQ26B	DQ26B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B48p	DIFFOUT_B95p	AC7	Yes	DQS26B	DQ26B/CQn26B	DQ26B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B48n	DIFFOUT_B95n	AD7	Yes	DQSn26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96p	AB7	Yes	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96n	AD6	Yes	DQ26B	DQ26B	DQ26B
		nIO_PULLUP		nIO_PULLUP			AE3	No			
		nCEO		nCEO			AB5	No			
		DCLK		DCLK			AC5	No			
		nCSO		nCSO			AD4	No			
		ASDO		ASDO			AA6	No			
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AC3	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AC4	Yes			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AF1	Yes			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AE2	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AB3	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AB4	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AG1	Yes	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AF2	Yes	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	Y6	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	Y7	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AE1	Yes	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AD1	Yes	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AA4	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	Y5	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AC1	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AC2	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	Y3	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	Y4	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AB1	Yes	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AB2	Yes	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	W8	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	W9	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AA1	Yes	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	Y2	Yes	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	W5	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	W6	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	Y1	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	W2	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	V6	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	V7	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	W3	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	W4	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	U6	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	U7	Yes			
5C	VREFB5CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	V3	Yes	DQSn8R		
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	V4	Yes	DQS8R		
5C	VREFB5CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	U8	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	U9	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	W1	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	V1	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	T4	Yes	DQ9R	DQ8R	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	U5	Yes	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	U3	Yes	DQSn9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	U4	Yes	DQS9R	DQ8R/CQn8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	T8	Yes	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	T9	Yes	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	T2	Yes	DQSn10R	DQSn8R/DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	T3	Yes	DQS10R	DQS8R/CQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	T6	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	R6	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	R4	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	T5	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	R9	No			
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	R10	No			
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	U1	No			
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	U2	No			
5C	VREFB5CN0	CLK8n	CLK8n				T1	No			
5C	VREFB5CN0	CLK8p	CLK8p				R1	No			
6C	VREFB6CN0	CLK10p	CLK10p				P2	No			
6C	VREFB6CN0	CLK10n	CLK10n				P1	No			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	M1	No			
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	N1	No			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	P9	No			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	P8	No			
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	N4	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	P4	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	N7	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	N6	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	P3	Yes	DQS17R	DQS19R/CQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	N2	Yes	DQSn17R	DQSn19R/DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	N5	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	M4	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	L2	Yes	DQS18R	DQ19R/CQn19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	L1	Yes	DQSn18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	N9	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	N8	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	L3	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	M3	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	L5	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	L4	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	K2	Yes	DQS19R		
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	K1	Yes	DQSn19R		
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	L6	Yes			
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	M6	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	H2	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	J1	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	K7	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	K6	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	G2	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	H1	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	K5	Yes	DQ23R	DQ25R	DQ26R

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	K4	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	F1	Yes	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	G1	Yes	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	J4	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	J3	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	E2	Yes	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	E1	Yes	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	L9	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	L8	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	H4	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	H3	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	K9	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	K8	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	D2	Yes	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	D1	Yes	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	J6	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	H5	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	F4	Yes	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	F3	Yes	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	G4	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	G3	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	B1	Yes			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	C1	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R44p	DIFFOUT_R88p	H6	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R44n	DIFFOUT_R88n	G5	Yes			
		MSEL2		MSEL2			G7	No			
		MSEL1		MSEL1			J9	No			
		MSEL0		MSEL0			H8	No			
7A	VREFB7AN0	IO				DIFFOUT_T1n	A2	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C3	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A4	Yes	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B4	Yes	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	A3	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B2	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D7	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E7	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	G8	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	G9	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	E8	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	F8	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	D6	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	E5	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	C5	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	D5	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	B5	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	C6	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A5	Yes	DQSn4T	DQS2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	A6	Yes	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A8	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	A9	Yes	DQ4T	DQ2T	DQ1T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B8	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	F9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	Yes	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	Yes	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	D9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	C9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	E10	Yes	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	F10	Yes	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	H10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	G10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	D10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	E11	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	H11	Yes			
7A	VREFB7AN0	IO				DIFFOUT_T19p	J10	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	J11	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	J12	Yes			
7C	VREFB7CN0	IO				DIFFOUT_T33n	B10	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T33p	C10	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	A10	Yes	DQSn11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	B11	Yes	DQS11T	DQ11T/CQn11T	
7C	VREFB7CN0	IO				DIFFOUT_T35n	A11	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T35p	A12	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	C12	Yes	DQSn12T	DQSn11T/DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	D11	Yes	DQS12T	DQS11T/CQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37n	E13	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37p	D13	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	C13	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	D12	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T39n	G12	Yes	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T39p	F12	Yes	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	F13	Yes	DQSn13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	G13	Yes	DQS13T		
7C	VREFB7CN0	IO				DIFFOUT_T41n	H14	Yes	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T41p	J14	Yes	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	A13	Yes			
7C	VREFB7CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	B13	Yes			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T47n	A14	No			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T47p	B14	No			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T24n	DIFFOUT_T48n	C14	No			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T24p	DIFFOUT_T48p	D14	No			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T25p	DIFFOUT_T49p	D15	No			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T25n	DIFFOUT_T49n	C15	No			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T50p	B16	No			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T50n	A15	No			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T26p	DIFFOUT_T51p	B17	No			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T26n	DIFFOUT_T51n	A16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T52p	J16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T52n	J15	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
8C	VREFB8CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	E16	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	D16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T54p	G16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T54n	H16	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	B19	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	A19	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60p	A17	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60n	A18	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	C19	Yes	DQS15T	DQS16T/CQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C18	Yes	DQSn15T	DQSn16T/DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62p	F17	Yes	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62n	C17	Yes	DQ16T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32p	DIFFOUT_T63p	E17	Yes	DQS16T	DQ16T/CQn16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32n	DIFFOUT_T63n	D17	Yes	DQSn16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64p	D18	Yes	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64n	F18	Yes	DQ16T	DQ16T	
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	G18	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	F19	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T78p	J18	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T78n	J19	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	B20	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	A21	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80p	A20	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80n	D19	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	D20	Yes	DQS21T	DQS24T/CQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	C20	Yes	DQSn21T	DQSn24T/DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82p	D21	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82n	C21	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	B22	Yes	DQS22T	DQ24T/CQn24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	A22	Yes	DQSn22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84p	A23	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84n	B23	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	B25	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	A26	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86p	A24	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86n	A25	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	B26	Yes	DQS23T	DQS25T/CQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	A27	Yes	DQSn23T	DQSn25T/DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88p	F20	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88n	E20	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	H20	Yes	DQS24T	DQ25T/CQn25T	DQS26T/CQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	G20	Yes	DQSn24T	DQ25T	DQSn26T/DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90p	H19	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90n	J20	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	D23	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	C23	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92p	D22	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92n	D25	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	D24	Yes	DQS25T	DQS26T/CQ26T	DQ26T/CQn26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	C24	Yes	DQSn25T	DQSn26T/DQ26T	DQ26T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
8A	VREFB8AN0	IO				DIFFOUT_T94p	F21	Yes	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94n	G21	Yes	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T48p	DIFFOUT_T95p	F22	Yes	DQS26T	DQ26T/CQn26T	DQ26T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T48n	DIFFOUT_T95n	E22	Yes	DQSn26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96p	E23	Yes	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96n	G22	Yes	DQ26T	DQ26T	DQ26T
		GND					AF3	No			
		GND					R14	No			
		GND					AG2	No			
		GND					AG5	No			
		GND					AG8	No			
		GND					AG11	No			
		GND					AG14	No			
		GND					AG17	No			
		GND					AG20	No			
		GND					AG23	No			
		GND					AG26	No			
		GND					AF27	No			
		GND					AD2	No			
		GND					AD5	No			
		GND					AD8	No			
		GND					AD11	No			
		GND					AD14	No			
		GND					AD17	No			
		GND					AD20	No			
		GND					AD23	No			
		GND					AC24	No			
		GND					AC27	No			
		GND					AA2	No			
		GND					AA5	No			
		GND					AA8	No			
		GND					AA11	No			
		GND					AA14	No			
		GND					AA17	No			
		GND					AA20	No			
		GND					Y12	No			
		GND					Y16	No			
		GND					Y21	No			
		GND					Y24	No			
		GND					Y27	No			
		GND					W12	No			
		GND					W14	No			
		GND					W16	No			
		GND					W18	No			
		GND					V2	No			
		GND					V5	No			
		GND					V8	No			
		GND					V11	No			
		GND					V13	No			
		GND					V15	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					V17	No			
		GND					V19	No			
		GND					U10	No			
		GND					U12	No			
		GND					U14	No			
		GND					U16	No			
		GND					U18	No			
		GND					U21	No			
		GND					U24	No			
		GND					U27	No			
		GND					T11	No			
		GND					T13	No			
		GND					T15	No			
		GND					T17	No			
		GND					T19	No			
		GND					R2	No			
		GND					R5	No			
		GND					R8	No			
		GND					R12	No			
		GND					R16	No			
		GND					R18	No			
		GND					P11	No			
		GND					P13	No			
		GND					P17	No			
		GND					P21	No			
		GND					P24	No			
		GND					P27	No			
		GND					N10	No			
		GND					N12	No			
		GND					N14	No			
		GND					N16	No			
		GND					N18	No			
		GND					M2	No			
		GND					M5	No			
		GND					M8	No			
		GND					M11	No			
		GND					M13	No			
		GND					M15	No			
		GND					M17	No			
		GND					M19	No			
		GND					L10	No			
		GND					L12	No			
		GND					L14	No			
		GND					L16	No			
		GND					L18	No			
		GND					L21	No			
		GND					L24	No			
		GND					L27	No			
		GND					K11	No			
		GND					K13	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					K15	No			
		GND					K17	No			
		GND					K19	No			
		GND					J2	No			
		GND					J5	No			
		GND					J8	No			
		GND					J13	No			
		GND					J17	No			
		GND					H9	No			
		GND					H12	No			
		GND					H15	No			
		GND					H18	No			
		GND					H21	No			
		GND					H24	No			
		GND					H27	No			
		GND					F2	No			
		GND					F5	No			
		GND					E6	No			
		GND					E9	No			
		GND					E12	No			
		GND					E15	No			
		GND					E18	No			
		GND					E21	No			
		GND					E24	No			
		GND					E27	No			
		GND					C2	No			
		GND					B3	No			
		GND					B6	No			
		GND					B9	No			
		GND					B12	No			
		GND					B15	No			
		GND					B18	No			
		GND					B21	No			
		GND					B24	No			
		GND					B27	No			
		VCC					R15	No			
		VCC					N17	No			
		VCC					V14	No			
		VCC					V18	No			
		VCC					U11	No			
		VCC					U13	No			
		VCC					U15	No			
		VCC					U17	No			
		VCC					T12	No			
		VCC					T14	No			
		VCC					T16	No			
		VCC					R13	No			
		VCC					R17	No			
		VCC					P12	No			
		VCC					P14	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCC					P16	No			
		VCC					P18	No			
		VCC					N13	No			
		VCC					N15	No			
		VCC					M12	No			
		VCC					M14	No			
		VCC					M16	No			
		VCC					L11	No			
		VCC					L17	No			
		VCC					M18	No			
		VCC					V12	No			
		VCC					V16	No			
		VCC					T18	No			
		VCC					R11	No			
		VCC					N11	No			
		VCC					L13	No			
		VCC					L15	No			
		VCCPT					U20	No			
		VCCPT					R24	No			
		VCCPT					AD15	No			
		VCCPT					P5	No			
		VCCPT					M9	No			
		VCCPT					E14	No			
		DNU					P15	No			
		VCCPGM					AA21	No			
		VCCPGM					Y8	No			
		TEMPDIODEn					D4	No			
		TEMPDIODEp					D3	No			
		VCC_CLKIN3C					AB14	No			
		VCC_CLKIN4C					AC13	No			
		VCC_CLKIN7C					F14	No			
		VCC_CLKIN8C					F16	No			
		VCCBAT					F6	No			
		VCCA_PLL_B1					AC14	No			
		VCCA_PLL_L2					R22	No			
		VCCA_PLL_R2					R7	No			
		VCCA_PLL_T1					F15	No			
		VCCD_PLL_B1					AB15	No			
		VCCD_PLL_L2					P22	No			
		VCCD_PLL_R2					P7	No			
		VCCD_PLL_T1					G15	No			
		VCCIO1A					H23	No			
		VCCIO1A					H26	No			
		VCCIO1A					E26	No			
		VCCIO1C					R23	No			
		VCCIO1C					P26	No			
		VCCIO2A					AD26	No			
		VCCIO2A					AA22	No			
		VCCIO2A					W26	No			
		VCCIO2C					V22	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCCIO2C					T26	No			
		VCCIO3A					AF22	No			
		VCCIO3A					AF25	No			
		VCCIO3A					AC18	No			
		VCCIO3A					AC22	No			
		VCCIO3C					AF18	No			
		VCCIO3C					AC15	No			
		VCCIO4A					AF4	No			
		VCCIO4A					AF7	No			
		VCCIO4A					AD10	No			
		VCCIO4A					AC6	No			
		VCCIO4C					AF13	No			
		VCCIO4C					AB12	No			
		VCCIO5A					AD3	No			
		VCCIO5A					AA3	No			
		VCCIO5A					AA7	No			
		VCCIO5C					R3	No			
		VCCIO5C					P6	No			
		VCCIO6A					K3	No			
		VCCIO6A					H7	No			
		VCCIO6A					E3	No			
		VCCIO6C					N3	No			
		VCCIO6C					L7	No			
		VCCIO7A					F7	No			
		VCCIO7A					F11	No			
		VCCIO7A					C4	No			
		VCCIO7A					C7	No			
		VCCIO7C					G14	No			
		VCCIO7C					C11	No			
		VCCIO8A					F23	No			
		VCCIO8A					E19	No			
		VCCIO8A					C22	No			
		VCCIO8A					C25	No			
		VCCIO8C					G17	No			
		VCCIO8C					C16	No			
		VCCPD1A					L19	No			
		VCCPD1C					N19	No			
		VCCPD2A					U19	No			
		VCCPD2C					R19	No			
		VCCPD3A					W17	No			
		VCCPD3C					W15	No			
		VCCPD4A					W11	No			
		VCCPD4C					W13	No			
		VCCPD5A					V10	No			
		VCCPD5C					T10	No			
		VCCPD6A					M10	No			
		VCCPD6C					P10	No			
		VCCPD7A					K12	No			
		VCCPD7C					K14	No			
		VCCPD8A					K18	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCCPD8C					K16	No			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				K22	No			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				N22	No			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				Y22	No			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				U22	No			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB18	No			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AA16	No			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB10	No			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AA12	No			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				W7	No			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				T7	No			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				J7	No			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				M7	No			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G11	No			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				H13	No			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G19	No			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				H17	No			
		NC					E25	No			
		NC					AB22	No			
		NC					W10	No			
		NC					E4	No			
		NC					AE25	No			
		NC					V9	No			
		NC					L20	No			
		NC					K10	No			
		NC					J21	No			
		VCCAUX					G23	No			
		VCCAUX					AC23	No			
		VCCAUX					AB6	No			
		VCCAUX					G6	No			

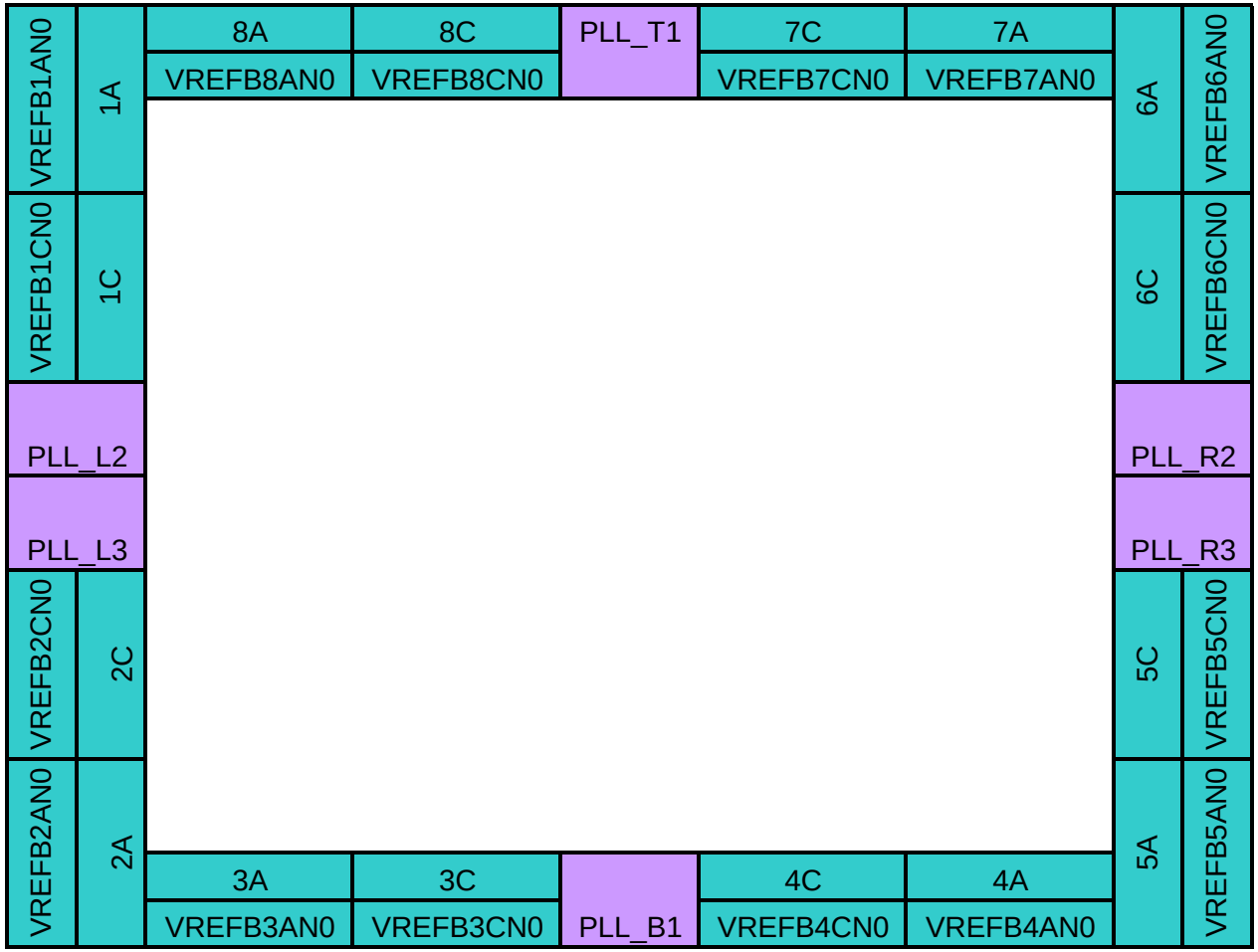
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[7..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Optional/Dual-Purpose Configuration Pins
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
		Differential I/O Pins
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side row and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
		External Memory Interface Pins
DQS[1:44][T,B], DQS[1:40][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:44][T,B], DQSn[1:40][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:44][T,B], DQ[1:40][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:44][T,B], CQ[1:40][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1:44][T,B], CQn[1:40][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
		Reference Pins
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
		Supply Pins
VCC	Power	VCC supplies power to the core and periphery.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[1:8][A,B,C]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.

Notes:

1. This pin definition is prepared based on the largest density, that is EP4SE820. Refer to pin list for the availability of the pins in each density.
2. Some of the pull-up/pull down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
Refer to the Configuring Stratix IV E Devices chapter in the Stratix IV E Device Handbook for more information.
3. Refer to Pin Connections Guidelines and data sheet for the recommended operating voltage.



Note:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	6/15/2009	Initial release.
1.1	12/3/2009	Added bank number for JTAG pins.
		Updated largest density in Note (1) of Pin Definitions.
		Updated DQS, DQSn, DQ, CQ, and CQn count in Pin Definitions.
		Grouped nCSO, ASDO, and DCLK into dedicated configuration/JTAG pins in Pin Definitions.
1.2	2/4/2015	Added the Dynamic OCT Support column in Pin List.