Pin Information for the Stratix® IV GT EP4S100G4 Device
Version 1.3
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
1A		TDI		TDI			A36	No				
1A		TMS		TMS			B36	No				
1A		TRST		TRST			F36	No				
1A		TCK		TCK			G35	No				
1A		TDO		TDO			E36	No				
1A	VREFB1AN0	IO	PLL_L1_CLKOUT0n		DIFFIO_TX_L1n	DIFFOUT_L1n	G34	Yes				
1A	VREFB1AN0	IO	PLL_L1_FB_CLKOUT0p		DIFFIO_TX_L1p	DIFFOUT_L1p	H34	Yes				
1A	VREFB1AN0	IO	RDN1A				E37	Yes				
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	F37	Yes				
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	M33	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	N33	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	J34	Yes	DQSn1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	K34	Yes	DQS1L	DQ1L/CQn1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	R31	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	T31	Yes	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	J35	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	K35	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	P31	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	R30	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	H36	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	J36	Yes	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M35	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	N35	Yes	DQ3L	DQ2L	DQ1L	
		NC					E38	Yes				
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	F38	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	L36	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	M36	Yes	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	G37	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	H37	Yes	DQS4L	DQS2L/CQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	T30	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	U30	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	J37	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	K37	Yes	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	W31	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	W30	Yes	DQ5L	DQ3L		
		NC					H40	Yes				
		NC					J40	Yes				
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	L35	Yes	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	L34	Yes	DQ5L	DQ3L		
		NC					F40	Yes				
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	F39	Yes	DQS6L	DQS3L/CQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	N34	Yes	DQ6L	DQ3L		
		NC					P34	Yes				
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	H38	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	J38	Yes	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	V31	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	V30	Yes	DQ7L			
		NC					G40	Yes				
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	G39	Yes	DQS7L			
		NC					R33	Yes				
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	P32	Yes	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	J39	Yes				

Pin Information for the Stratix® IV GT EP4S100G4 Device
Version 1.3
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	K39	Yes				
		NC					P36	Yes				
		NC					P35	Yes				
1C	VREFB1CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L38n	M38	Yes	DQSn12L	DQ12L	DQ12L	
1C	VREFB1CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L38p	M37	Yes	DQS12L	DQ12L/CQn12L	DQ12L	
1C	VREFB1CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L39n	U32	Yes	DQ12L	DQ12L	DQ12L	
1C	VREFB1CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L39p	V32	Yes	DQ12L	DQ12L	DQ12L	
1C	VREFB1CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L40n	L39	Yes	DQSn13L	DQSn12L/DQ12L	DQ12L	
1C	VREFB1CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L40p	L38	Yes	DQS13L	DQS12L/CQ12L	DQ12L/CQn12L	
		NC					T33	Yes				
		NC					U33	Yes				
		NC					M40	Yes				
1C	VREFB1CN0	IO			DIFFIO_RX_L21p	DIFFOUT_L42p	M39	Yes	DQ13L	DQ12L	DQ12L	
		NC					V34	Yes				
		NC					W33	Yes				
		NC					K40	Yes				
		NC					L40	Yes				
		NC					U36	Yes				
		NC					V35	Yes				
1C	VREFB1CN0	IO			DIFFIO_RX_L23n	DIFFOUT_L46n	R38	Yes	DQSn15L	DQSn13L/DQ13L	DQ12L	
		NC					R37	Yes				
1C	VREFB1CN0	IO		CLKUSR			V37	Yes				
		NC					V36	Yes				
		NC					N40	Yes				
1C	VREFB1CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L48p	N39	Yes	DQ15L	DQ13L	DQ12L	
1C	VREFB1CN0	IO		DATA0			AA33	Yes				
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L25p	DIFFOUT_L49p	Y32	Yes	DQ16L	DQ14L		
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L25n	DIFFOUT_L50n	P38	Yes	DQSn16L	DQ14L		
1C	VREFB1CN0	IO		DATA3			P37	Yes				
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L26n	DIFFOUT_L51n	U38	Yes	DQ16L	DQ14L		
1C	VREFB1CN0	IO		DATA5			U37	Yes				
1C	VREFB1CN0	IO		DATA6			R40	Yes				
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L26p	DIFFOUT_L52p	P39	Yes	DQS17L	DQS14L/CQ14L		
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L27n	DIFFOUT_L53n	Y31	Yes	DQ17L	DQ14L		
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L27p	DIFFOUT_L53p	AA31	Yes	DQ17L	DQ14L		
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L27n	DIFFOUT_L54n	R39	Yes	DQ17L	DQ14L		
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L27p	DIFFOUT_L54p	T39	Yes	DQ17L	DQ14L		
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L28n	DIFFOUT_L55n	AA30	No				
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L28p	DIFFOUT_L55p	AB30	No				
1C	VREFB1CN0	CLK1n	CLK1n				U39	No				
1C	VREFB1CN0	CLK1p	CLK1p				V39	No				
2C	VREFB2CN0	CLK3p	CLK3p				AD39	No				
2C	VREFB2CN0	CLK3n	CLK3n				AC39	No				
2C	VREFB2CN0	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AA38	Yes	DQ18L	DQ21L		
2C	VREFB2CN0	IO			DIFFIO_RX_L30n	DIFFOUT_L59n	Y38	Yes	DQ18L	DQ21L		
2C	VREFB2CN0	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AB39	Yes	DQS18L	DQS21L/CQ21L		
2C	VREFB2CN0	IO			DIFFIO_RX_L31n	DIFFOUT_L61n	AA39	Yes	DQSn18L	DQSn21L/DQ21L		
2C	VREFB2CN0	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	Y39	Yes	DQS19L	DQ21L/CQn21L		
2C	VREFB2CN0	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AF38	Yes	DQ19L	DQ21L		
2C	VREFB2CN0	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	W38	Yes	DQ20L	DQ22L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AE39	Yes	DQS20L	DQS22L/CQ22L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AD38	Yes	DQS21L	DQ22L/CQn22L	DQS23L/CQ23L	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
2C	VREFB2CN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AC38	Yes	DQSn21L	DQ22L	DQSn23L/DQ23L	
2C	VREFB2CN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AF32	Yes	DQ21L	DQ22L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AH39	Yes	DQ22L	DQ23L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AG39	Yes	DQS22L	DQS23L/CQ23L	DQ23L/CQn23L	
2C	VREFB2CN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	AF39	Yes	DQSn22L	DQSn23L/DQ23L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AD29	Yes	DQ23L	DQ23L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AD30	Yes	DQ23L	DQ23L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AG38	Yes	DQSn23L	DQ23L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AE30	Yes	DQ23L	DQ23L	DQ23L	
2C	VREFB2CN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AE31	Yes	DQ23L	DQ23L	DQ23L	
2B	VREFB2BN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AJ39	Yes				
2B	VREFB2BN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AL39	Yes	DQS25L			
2B	VREFB2BN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AM38	Yes	DQ26L	DQ27L		
2B	VREFB2BN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AM39	Yes	DQ26L	DQ27L		
2B	VREFB2BN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AL35	Yes	DQ26L	DQ27L		
2B	VREFB2BN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AK38	Yes	DQS26L	DQS27L/CQ27L		
2B	VREFB2BN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AK39	Yes	DQSn26L	DQSn27L/DQ27L		
2B	VREFB2BN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AH31	Yes	DQ27L	DQ27L		
2B	VREFB2BN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AG32	Yes	DQ27L	DQ27L		
2B	VREFB2BN0	IO			DIFFIO_RX_L44p	DIFFOUT_L87p	AL36	Yes	DQS27L	DQ27L/CQn27L		
2B	VREFB2BN0	IO			DIFFIO_RX_L44n	DIFFOUT_L87n	AM37	Yes	DQSn27L	DQ27L		
2B	VREFB2BN0	IO			DIFFIO_TX_L44p	DIFFOUT_L88p	AF30	Yes	DQ27L	DQ27L		
2B	VREFB2BN0	IO			DIFFIO_TX_L44n	DIFFOUT_L88n	AG31	Yes	DQ27L	DQ27L		
2A	VREFB2AN0	IO			DIFFIO_RX_L45p	DIFFOUT_L89p	AN39	Yes				
2A	VREFB2AN0	IO			DIFFIO_RX_L46p	DIFFOUT_L91p	AR39	Yes	DQS28L			
2A	VREFB2AN0	IO			DIFFIO_RX_L46n	DIFFOUT_L91n	AP39	Yes	DQSn28L			
2A	VREFB2AN0	IO			DIFFIO_TX_L46p	DIFFOUT_L92p	AN35	Yes	DQ28L			
2A	VREFB2AN0	IO			DIFFIO_TX_L46n	DIFFOUT_L92n	AM35	Yes	DQ28L			
2A	VREFB2AN0	IO			DIFFIO_RX_L47p	DIFFOUT_L93p	AN37	Yes	DQ29L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_RX_L47n	DIFFOUT_L93n	AN38	Yes	DQ29L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_TX_L47p	DIFFOUT_L94p	AP35	Yes	DQ29L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_TX_L47n	DIFFOUT_L94n	AP36	Yes	DQ29L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_TX_L48p	DIFFOUT_L96p	AM33	Yes	DQ30L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_TX_L48n	DIFFOUT_L96n	AL34	Yes	DQ30L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_RX_L49p	DIFFOUT_L97p	AU39	Yes	DQS30L	DQ32L/CQn32L		
2A	VREFB2AN0	IO			DIFFIO_RX_L49n	DIFFOUT_L97n	AT39	Yes	DQSn30L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_TX_L49p	DIFFOUT_L98p	AN33	Yes	DQ30L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_TX_L49n	DIFFOUT_L98n	AN34	Yes	DQ30L	DQ32L		
2A	VREFB2AN0	IO			DIFFIO_RX_L50p	DIFFOUT_L99p	AR37	Yes	DQ31L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L50n	DIFFOUT_L99n	AP37	Yes	DQ31L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L50p	DIFFOUT_L100p	AJ31	Yes	DQ31L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L50n	DIFFOUT_L100n	AJ32	Yes	DQ31L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L51p	DIFFOUT_L101p	AT37	Yes	DQS31L	DQS33L/CQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L51n	DIFFOUT_L101n	AT38	Yes	DQSn31L	DQSn33L/DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L51p	DIFFOUT_L102p	AR34	Yes	DQ32L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L51n	DIFFOUT_L102n	AP34	Yes	DQ32L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L52p	DIFFOUT_L103p	AU36	Yes	DQS32L	DQ33L/CQn33L	DQS34L/CQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L52n	DIFFOUT_L103n	AU37	Yes	DQSn32L	DQ33L	DQSn34L/DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L52p	DIFFOUT_L104p	AK31	Yes	DQ32L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L52n	DIFFOUT_L104n	AK32	Yes	DQ32L	DQ33L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L53p	DIFFOUT_L105p	AW36	Yes	DQ33L	DQ34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L53n	DIFFOUT_L105n	AW37	Yes	DQ33L	DQ34L	DQ34L	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
2A	VREFB2AN0	IO			DIFFIO_TX_L53p	DIFFOUT_L106p	AR35	Yes	DQ33L	DQ34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L53n	DIFFOUT_L106n	AT36	Yes	DQ33L	DQ34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L54p	DIFFOUT_L108p	AU34	Yes	DQ34L	DQ34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L54n	DIFFOUT_L108n	AT34	Yes	DQ34L	DQ34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L55p	DIFFOUT_L109p	AV37	Yes	DQS34L	DQ34L/CQn34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_RX_L55n	DIFFOUT_L109n	AV38	Yes	DQSn34L	DQ34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L55p	DIFFOUT_L110p	AV35	Yes	DQ34L	DQ34L	DQ34L	
2A	VREFB2AN0	IO			DIFFIO_TX_L55n	DIFFOUT_L110n	AU35	Yes	DQ34L	DQ34L	DQ34L	
2A	VREFB2AN0	IO	RUP2A				AY37	Yes				
2A	VREFB2AN0	IO	RDN2A				AY38	Yes				
2A	VREFB2AN0	IO	PLL_L4_FB_CLKOUT0p		DIFFIO_TX_L56p	DIFFOUT_L112p	AJ30	Yes				
2A	VREFB2AN0	IO	PLL_L4_CLKOUT0n		DIFFIO_TX_L56n	DIFFOUT_L112n	AH30	Yes				
2A	VREFB2AN0	PLL_L4_CLKp	PLL_L4_CLKp				AY39	No				
2A	VREFB2AN0	PLL_L4_CLKn	PLL_L4_CLKn				AY40	No				
		nCONFIG		nCONFIG			BA36	No				
		nSTATUS		nSTATUS			AY36	No				
		CONF_DONE		CONF_DONE			AW38	No				
		PORSEL					AY35	No				
		nCE		nCE			AW35	No				
3A	VREFB3AN0	IO				DIFFOUT_B1n	BB35	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	BC35	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	BD35	Yes	DQSn1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	BC34	Yes	DQS1B	DQ1B/CQn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	BD34	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	BD33	Yes	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	BD32	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	BC32	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	BB32	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	BB31	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	BD31	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	BC31	Yes	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AW34	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	BA33	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	BA34	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AY34	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AW33	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	BB33	Yes	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	BA31	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AY31	Yes	DQS4B	DQS2B/CQ2B	DQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	BA32	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AY32	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AW31	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AV31	Yes	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AT33	Yes	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13p	AT32	Yes	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AV34	Yes	DQSn5B	DQ3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AV33	Yes	DQS5B	DQ3B/CQn3B	DQ2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15n	AU32	Yes	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15p	AV32	Yes	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AR32	Yes	DQSn6B	DQSn3B/DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AR31	Yes	DQS6B	DQS3B/CQ3B	DQ2B/CQn2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B17n	AT31	Yes	DQ6B	DQ3B	DQ2B	DQ1B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
3A	VREFB3AN0	IO				DIFFOUT_B17p	AU31	Yes	DQ6B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AT30	Yes	DQ6B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AR30	Yes	DQ6B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19n	AM30	Yes	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19p	AM31	Yes	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AN31	Yes	DQSn7B	DQ4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AN30	Yes	DQS7B	DQ4B/CQn4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B21n	AL32	Yes	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B21p	AN29	Yes	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AM29	Yes	DQSn8B	DQSn4B/DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AL29	Yes	DQS8B	DQS4B/CQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B23n	AK29	Yes	DQ8B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B23p	AK30	Yes	DQ8B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AL28	Yes	DQ8B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AK28	Yes	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO				DIFFOUT_B25n	BD30	Yes	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B25p	BD29	Yes	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	BC29	Yes	DQSn9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	BB30	Yes	DQS9B	DQ9B/CQn9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27n	BD28	Yes	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27p	BC28	Yes	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	BD27	Yes	DQSn10B	DQSn9B/DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	BD26	Yes	DQS10B	DQS9B/CQ9B	DQ9B/CQn9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B29n	BC26	Yes	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B29p	BB26	Yes	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	BD25	Yes	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	BC25	Yes	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AY29	Yes	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AY28	Yes	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	BA30	Yes	DQSn11B	DQ10B	DQSn9B/DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	BA29	Yes	DQS11B	DQ10B/CQn10B	DQS9B/CQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33n	AW29	Yes	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33p	AW30	Yes	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	BB28	Yes	DQSn12B	DQSn10B/DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	BA28	Yes	DQS12B	DQS10B/CQ10B	DQ9B	DQ9B/CQn9B
3B	VREFB3BN0	IO				DIFFOUT_B35n	AY26	Yes	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B35p	AW26	Yes	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	BA27	Yes	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	BA26	Yes	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B37n	AT29	Yes	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B37p	AR29	Yes	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AV29	Yes	DQSn13B	DQ11B	DQ10B	DQSn9B/DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AU29	Yes	DQS13B	DQ11B/CQn11B	DQ10B	DQS9B/CQ9B
3B	VREFB3BN0	IO				DIFFOUT_B39n	AU28	Yes	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B39p	AV28	Yes	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B20n	DIFFOUT_B40n	AW28	Yes	DQSn14B	DQSn11B/DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B20p	DIFFOUT_B40p	AV27	Yes	DQS14B	DQS11B/CQ11B	DQ10B/CQn10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B41n	AU27	Yes	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B41p	AT26	Yes	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B21n	DIFFOUT_B42n	AV26	Yes	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B21p	DIFFOUT_B42p	AU26	Yes	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B43n	AN28	Yes	DQ15B	DQ12B	DQ10B	DQ9B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
3B	VREFB3BN0	IO				DIFFOUT_B43p	AR27	Yes	DQ15B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AR28	Yes	DQSn15B	DQ12B	DQSn10B/DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AP28	Yes	DQS15B	DQ12B/CQn12B	DQS10B/CQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B45n	AM28	Yes	DQ15B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B45p	AR26	Yes	DQ15B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B23n	DIFFOUT_B46n	AK27	Yes	DQSn16B	DQSn12B/DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B23p	DIFFOUT_B46p	AK26	Yes	DQS16B	DQS12B/CQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B47n	AM27	Yes	DQ16B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B47p	AL26	Yes	DQ16B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B24n	DIFFOUT_B48n	AN26	Yes	DQ16B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B24p	DIFFOUT_B48p	AM26	Yes	DQ16B	DQ12B	DQ10B	DQ9B
3C	VREFB3CN0	IO				DIFFOUT_B49n	BB25	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B49p	AW25	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO	RDN3C		DIFFIO_RX_B25n	DIFFOUT_B50n	BA25	Yes	DQSn17B	DQ17B		
3C	VREFB3CN0	IO	RUP3C		DIFFIO_RX_B25p	DIFFOUT_B50p	AY25	Yes	DQS17B	DQ17B/CQn17B		
3C	VREFB3CN0	IO				DIFFOUT_B51n	BA24	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B51p	AW24	Yes	DQ17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	BD24	Yes	DQSn18B	DQSn17B/DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	BD23	Yes	DQS18B	DQS17B/CQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53n	BA23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53p	AY23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	BC23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	BB23	Yes	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B55n	AW23	Yes	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B55p	AV23	Yes	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AV25	Yes	DQSn19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AV24	Yes	DQS19B			
3C	VREFB3CN0	IO				DIFFOUT_B57n	AT23	Yes	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B57p	AU23	Yes	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B58n	AR25	Yes				
3C	VREFB3CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B58p	AP25	Yes				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AM25	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AN24	No				
3C	VREFB3CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B60n	AT25	No				
3C	VREFB3CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B60p	AT24	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AM24	No				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	AL23	No				
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AN23	No				
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AM23	No				
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AK23	No				
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AJ24	No				
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AL25	No				
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AK24	No				
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AK21	No				
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AL22	No				
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AJ22	No				
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AK22	No				
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AM21	No				
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AM22	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	AU22	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AV22	No				
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AT20	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AU20	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AT21	No				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	AR20	No				
4C	VREFB4CN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AN20	Yes				
4C	VREFB4CN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AP20	Yes				
4C	VREFB4CN0	IO				DIFFOUT_B72p	BA22	Yes	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B72n	BB22	Yes	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	BD21	Yes	DQS20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	BD22	Yes	DQSn20B			
4C	VREFB4CN0	IO				DIFFOUT_B74p	BB21	Yes	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B74n	BC22	Yes	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	BC20	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	BD20	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76p	BA20	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76n	BB20	Yes	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	BC19	Yes	DQS21B	DQS22B/CQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	BD19	Yes	DQSn21B	DQSn22B/DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78p	AY22	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78n	AW22	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AW20	Yes	DQS22B	DQ22B/CQn22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AY20	Yes	DQSn22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80p	AV20	Yes	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80n	AW21	Yes	DQ22B	DQ22B		
4B	VREFB4BN0	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AN19	Yes	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AP19	Yes	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B82p	AM18	Yes	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B82n	AN18	Yes	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AN17	Yes	DQS23B	DQS27B/CQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AP17	Yes	DQSn23B	DQSn27B/DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B84p	AK20	Yes	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B84n	AL20	Yes	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AM19	Yes	DQS24B	DQ27B/CQn27B	DQS29B/CQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AM20	Yes	DQSn24B	DQ27B	DQSn29B/DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B86p	AL19	Yes	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B86n	AJ20	Yes	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AV18	Yes	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AV19	Yes	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B88p	AT19	Yes	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B88n	AU19	Yes	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AR19	Yes	DQS25B	DQS28B/CQ28B	DQ29B/CQn29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AT18	Yes	DQSn25B	DQSn28B/DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B90p	AT17	Yes	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B90n	AU17	Yes	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AU16	Yes	DQS26B	DQ28B/CQn28B	DQ29B	DQS30B/CQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AV16	Yes	DQSn26B	DQ28B	DQ29B	DQSn30B/DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B92p	AR16	Yes	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B92n	AT16	Yes	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	BA18	Yes	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	BA19	Yes	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94p	AW19	Yes	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94n	AY19	Yes	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B95p	AW17	Yes	DQS27B	DQS29B/CQ29B	DQ30B	DQ30B/CQn30B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
4B	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B95n	AW18	Yes	DQSn27B	DQSn29B/DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96p	BA15	Yes	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96n	BA16	Yes	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B97p	AY16	Yes	DQS28B	DQ29B/CQn29B	DQS30B/CQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B97n	AY17	Yes	DQSn28B	DQ29B	DQSn30B/DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98p	AW15	Yes	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98n	AW16	Yes	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50p	DIFFOUT_B99p	BB18	Yes	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50n	DIFFOUT_B99n	BC17	Yes	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100p	BB17	Yes	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100n	BA17	Yes	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51p	DIFFOUT_B101p	BD17	Yes	DQS29B	DQS30B/CQ30B	DQ30B/CQn30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51n	DIFFOUT_B101n	BD18	Yes	DQSn29B	DQSn30B/DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102p	BB15	Yes	DQ30B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102n	BC16	Yes	DQ30B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52p	DIFFOUT_B103p	BD15	Yes	DQS30B	DQ30B/CQn30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52n	DIFFOUT_B103n	BD16	Yes	DQSn30B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104p	BC14	Yes	DQ30B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104n	BD14	Yes	DQ30B	DQ30B	DQ30B	DQ30B
4A	VREFB4AN0	IO			DIFFIO_RX_B53p	DIFFOUT_B105p	AJ18	Yes	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B53n	DIFFOUT_B105n	AK18	Yes	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B106p	AM16	Yes	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B106n	AM17	Yes	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B107p	AK17	Yes	DQS31B	DQS35B/CQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B107n	AL17	Yes	DQSn31B	DQSn35B/DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B108p	AK16	Yes	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B108n	AJ16	Yes	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	AM14	Yes	DQS32B	DQ35B/CQn35B	DQS37B/CQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AM15	Yes	DQSn32B	DQ35B	DQSn37B/DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110p	AL14	Yes	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110n	AK15	Yes	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AU14	Yes	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AV15	Yes	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112p	AT14	Yes	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112n	AU13	Yes	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AT12	Yes	DQS33B	DQS36B/CQ36B	DQ37B/CQn37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AT13	Yes	DQSn33B	DQSn36B/DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114p	AR14	Yes	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114n	AR13	Yes	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AP16	Yes	DQS34B	DQ36B/CQn36B	DQ37B	DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AR15	Yes	DQSn34B	DQ36B	DQ37B	DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116p	AN15	Yes	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116n	AN14	Yes	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AY14	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	BA14	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118p	AV14	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AW14	Yes	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AY13	Yes	DQS35B	DQS37B/CQ37B	DQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	BA13	Yes	DQSn35B	DQSn37B/DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AV13	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	BA12	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AW12	Yes	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B	DQ38B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AY11	Yes	DQSn36B	DQ37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AV12	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	BA11	Yes	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	BB14	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	BC13	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	BB12	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	BB13	Yes	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	BD12	Yes	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	BD13	Yes	DQSn37B	DQSn38B/DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	BD10	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	BD11	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	BC10	Yes	DQS38B	DQ38B/CQn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	BC11	Yes	DQSn38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	BA10	Yes	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	BB10	Yes	DQ38B	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AV11	No				
		nCEO		nCEO			AW7	No				
		DCLK		DCLK			AY9	No				
		nCSO		nCSO			BA9	No				
		ASDO		ASDO			AW10	No				
5A	VREFB5AN0	PLL_R4_CLKn	PLL_R4_CLKn				AY5	No				
5A	VREFB5AN0	PLL_R4_CLKp	PLL_R4_CLKp				AY6	No				
5A	VREFB5AN0	IO	PLL_R4_CLKOUT0n		DIFFIO_TX_R1n	DIFFOUT_R1n	AR10	Yes				
5A	VREFB5AN0	IO	PLL_R4_FB_CLKOUT0p		DIFFIO_TX_R1p	DIFFOUT_R1p	AP10	Yes				
5A	VREFB5AN0	IO	RDN5A				AY7	Yes				
5A	VREFB5AN0	IO	RUP5A				AY8	Yes				
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AR8	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AP9	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AV7	Yes	DQSn1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AV8	Yes	DQS1R	DQ1R/CQn1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AK14	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AJ14	Yes	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AV10	Yes	DQSn2R	DQSn1R/DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AU10	Yes	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AU11	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AT11	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AW8	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AW9	Yes	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AN11	Yes	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AM11	Yes	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AU8	Yes	DQSn3R	DQ2R	DQSn1R/DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AU9	Yes	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AN12	Yes	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AM12	Yes	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AR7	Yes	DQSn4R	DQSn2R/DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AT8	Yes	DQS4R	DQS2R/CQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AH14	Yes	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AG15	Yes	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AV6	Yes	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AR11	Yes	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AP11	Yes	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AT6	Yes	DQSn5R	DQ3R		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AT7	Yes	DQS5R	DQ3R/CQn3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AL13	Yes	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AT9	Yes	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AT10	Yes	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AR6	Yes	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AN8	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AN9	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AP6	Yes	DQSn7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AN7	Yes	DQS7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AL10	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AL11	Yes	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AN6	Yes				
5B	VREFB5BN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AF15	Yes	DQ8R	DQ8R		
5B	VREFB5BN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AE16	Yes	DQ8R	DQ8R		
5B	VREFB5BN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AG13	Yes	DQ8R	DQ8R		
5B	VREFB5BN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AG14	Yes	DQ8R	DQ8R		
5B	VREFB5BN0	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AL6	Yes	DQS9R	DQS8R/CQ8R		
5B	VREFB5BN0	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	AJ13	Yes	DQ9R	DQ8R		
5B	VREFB5BN0	IO			DIFFIO_RX_R15n	DIFFOUT_R30n	AL8	Yes	DQ9R	DQ8R		
5B	VREFB5BN0	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AL9	Yes	DQ9R	DQ8R		
5B	VREFB5BN0	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	AF13	Yes	DQ10R			
5B	VREFB5BN0	IO			DIFFIO_RX_R16n	DIFFOUT_R32n	AM6	Yes	DQSn10R			
5B	VREFB5BN0	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AM7	Yes	DQS10R			
5B	VREFB5BN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	AK7	Yes				
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	AK6	Yes	DQSn12R	DQ12R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	AJ7	Yes	DQS12R	DQ12R/CQn12R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	AD15	Yes	DQ12R	DQ12R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	AC15	Yes	DQ12R	DQ12R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	AH6	Yes	DQS13R	DQS12R/CQ12R	DQ12R/CQn12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	AJ6	Yes	DQ13R	DQ12R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_TX_R22n	DIFFOUT_R43n	AE14	Yes	DQ14R	DQ13R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_TX_R22p	DIFFOUT_R43p	AD14	Yes	DQ14R	DQ13R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R22n	DIFFOUT_R44n	AG6	Yes	DQSn14R	DQ13R	DQSn12R/DQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R22p	DIFFOUT_R44p	AF6	Yes	DQS14R	DQ13R/CQn13R	DQS12R/CQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R23n	DIFFOUT_R46n	AG7	Yes	DQSn15R	DQSn13R/DQ13R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R48n	AA6	Yes	DQ15R	DQ13R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R48p	Y6	Yes	DQ15R	DQ13R	DQ12R	
5C	VREFB5CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R50n	AD7	Yes	DQSn16R	DQ14R		
5C	VREFB5CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R51n	AA7	Yes	DQ16R	DQ14R		
5C	VREFB5CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R52p	AE6	Yes	DQS17R	DQS14R/CQ14R		
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R28p	DIFFOUT_R56p	AB6	No				
5C	VREFB5CN0	CLK8n	CLK8n				AC6	No				
5C	VREFB5CN0	CLK8p	CLK8p				AD6	No				
6C	VREFB6CN0	CLK10p	CLK10p				W6	No				
6C	VREFB6CN0	CLK10n	CLK10n				V6	No				
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R29p	DIFFOUT_R57p	V7	No				
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R29p	DIFFOUT_R58p	Y14	No				
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R29n	DIFFOUT_R58n	AA14	No				
		NC					U8	Yes				
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	U7	Yes	DQ18R	DQ21R		
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	U6	Yes	DQS18R	DQS21R/CQ21R		
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	Y15	Yes	DQ19R	DQ21R		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	AA15	Yes	DQ19R	DQ21R		
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	N6	Yes	DQS19R	DQ21R/CQn21R		
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	P6	Yes	DQSn19R	DQ21R		
		NC					Y12	Yes				
		NC					AA12	Yes				
6C	VREFB6CN0	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	T6	Yes	DQ20R	DQ22R	DQ23R	
		NC					R5	Yes				
		NC					V10	Yes				
		NC					V9	Yes				
6C	VREFB6CN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	P7	Yes	DQS20R	DQS22R/CQ22R	DQ23R	
6C	VREFB6CN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	R6	Yes	DQSn20R	DQSn22R/DQ22R	DQ23R	
		NC					W12	Yes				
		NC					V11	Yes				
6C	VREFB6CN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	L6	Yes	DQS21R	DQ22R/CQn22R	DQS23R/CQ23R	
		NC					L5	Yes				
		NC					U12	Yes				
		NC					V12	Yes				
		NC					M5	Yes				
		NC					N5	Yes				
		NC					P8	Yes				
		NC					R8	Yes				
6C	VREFB6CN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	L7	Yes	DQS22R	DQS23R/CQ23R	DQ23R/CQn23R	
6C	VREFB6CN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	M6	Yes	DQSn22R	DQSn23R/DQ23R	DQ23R	
6C	VREFB6CN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	W14	Yes	DQ23R	DQ23R	DQ23R	
6C	VREFB6CN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	V13	Yes	DQ23R	DQ23R	DQ23R	
6C	VREFB6CN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	K6	Yes	DQS23R	DQ23R/CQn23R	DQ23R	
6C	VREFB6CN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	M8	Yes	DQ23R	DQ23R	DQ23R	
6C	VREFB6CN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	N8	Yes	DQ23R	DQ23R	DQ23R	
6A	VREFB6AN0	IO			DIFFIO_RX_R45p	DIFFOUT_R89p	J6	Yes				
		NC					J5	Yes				
6A	VREFB6AN0	IO			DIFFIO_TX_R45p	DIFFOUT_R90p	U14	Yes	DQ28R			
6A	VREFB6AN0	IO			DIFFIO_TX_R45n	DIFFOUT_R90n	U13	Yes	DQ28R			
6A	VREFB6AN0	IO			DIFFIO_RX_R46p	DIFFOUT_R91p	J8	Yes	DQS28R			
6A	VREFB6AN0	IO			DIFFIO_RX_R46n	DIFFOUT_R91n	J7	Yes	DQSn28R			
6A	VREFB6AN0	IO			DIFFIO_TX_R46p	DIFFOUT_R92p	V15	Yes	DQ28R			
6A	VREFB6AN0	IO			DIFFIO_TX_R46n	DIFFOUT_R92n	V14	Yes	DQ28R			
6A	VREFB6AN0	IO			DIFFIO_RX_R47p	DIFFOUT_R93p	L9	Yes	DQ29R	DQ32R		
6A	VREFB6AN0	IO			DIFFIO_RX_R47n	DIFFOUT_R93n	K8	Yes	DQ29R	DQ32R		
		NC					P10	Yes				
		NC					P9	Yes				
6A	VREFB6AN0	IO			DIFFIO_RX_R48p	DIFFOUT_R95p	H8	Yes	DQS29R	DQS32R/CQ32R		
6A	VREFB6AN0	IO			DIFFIO_RX_R48n	DIFFOUT_R95n	H7	Yes	DQSn29R	DQSn32R/DQ32R		
6A	VREFB6AN0	IO			DIFFIO_TX_R48p	DIFFOUT_R96p	M12	Yes	DQ30R	DQ32R		
6A	VREFB6AN0	IO			DIFFIO_TX_R48n	DIFFOUT_R96n	M11	Yes	DQ30R	DQ32R		
6A	VREFB6AN0	IO			DIFFIO_RX_R49p	DIFFOUT_R97p	H6	Yes	DQS30R	DQ32R/CQn32R		
		NC					H5	Yes				
6A	VREFB6AN0	IO			DIFFIO_TX_R49p	DIFFOUT_R98p	R13	Yes	DQ30R	DQ32R		
		NC					R12	Yes				
6A	VREFB6AN0	IO			DIFFIO_RX_R50p	DIFFOUT_R99p	F8	Yes	DQ31R	DQ33R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_RX_R50n	DIFFOUT_R99n	F7	Yes	DQ31R	DQ33R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R50p	DIFFOUT_R100p	N12	Yes	DQ31R	DQ33R	DQ34R	
		NC					P11	Yes				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
6A	VREFB6AN0	IO			DIFFIO_RX_R51p	DIFFOUT_R101p	G6	Yes	DQS31R	DQS33R/CQ33R	DQ34R	
		NC					G5	Yes				
6A	VREFB6AN0	IO			DIFFIO_TX_R51p	DIFFOUT_R102p	M10	Yes	DQ32R	DQ33R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R51n	DIFFOUT_R102n	N10	Yes	DQ32R	DQ33R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_RX_R52p	DIFFOUT_R103p	H9	Yes	DQS32R	DQ33R/CQn33R	DQS34R/CQ34R	
6A	VREFB6AN0	IO			DIFFIO_RX_R52n	DIFFOUT_R103n	J9	Yes	DQSn32R	DQ33R	DQSn34R/DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R52p	DIFFOUT_R104p	L10	Yes	DQ32R	DQ33R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R52n	DIFFOUT_R104n	M9	Yes	DQ32R	DQ33R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_RX_R53p	DIFFOUT_R105p	G10	Yes	DQ33R	DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_RX_R53n	DIFFOUT_R105n	H10	Yes	DQ33R	DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R53p	DIFFOUT_R106p	R14	Yes	DQ33R	DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R53n	DIFFOUT_R106n	P13	Yes	DQ33R	DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_RX_R54p	DIFFOUT_R107p	F9	Yes	DQS33R	DQS34R/CQ34R	DQ34R/CQn34R	
6A	VREFB6AN0	IO			DIFFIO_RX_R54n	DIFFOUT_R107n	G8	Yes	DQSn33R	DQSn34R/DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R54p	DIFFOUT_R108p	T15	Yes	DQ34R	DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R54n	DIFFOUT_R108n	U15	Yes	DQ34R	DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R55p	DIFFOUT_R110p	H11	Yes	DQ34R	DQ34R	DQ34R	
6A	VREFB6AN0	IO			DIFFIO_TX_R55n	DIFFOUT_R110n	J11	Yes	DQ34R	DQ34R	DQ34R	
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R56p	DIFFOUT_R111p	F6	Yes				
6A	VREFB6AN0	IO	RDN6A				F5	Yes				
6A	VREFB6AN0	IO	PLL_R1_FB_CLKOUT0p		DIFFIO_TX_R56p	DIFFOUT_R112p	K11	Yes				
6A	VREFB6AN0	IO	PLL_R1_CLKOUT0n		DIFFIO_TX_R56n	DIFFOUT_R112n	L11	Yes				
		MSEL2		MSEL2			F10	No				
		MSEL1		MSEL1			E9	No				
		MSEL0		MSEL0			A9	No				
7A	VREFB7AN0	IO				DIFFOUT_T1n	B10	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C10	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A11	Yes	DQSn1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	A12	Yes	DQS1T	DQ1T/CQn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	C12	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B11	Yes	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	A13	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	B13	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	B14	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	C13	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	C14	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	D14	Yes	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	E11	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	F11	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	D10	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	D11	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	D12	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	F12	Yes	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	E14	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	F14	Yes	DQS4T	DQS2T/CQ2T	DQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	F13	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	E13	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	G14	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	G15	Yes	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	L14	Yes	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13p	K13	Yes	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	J12	Yes	DQSn5T	DQ3T	DQ2T	DQSn1T/DQ1T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	J13	Yes	DQS5T	DQ3T/CQn3T	DQ2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15n	H13	Yes	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15p	G12	Yes	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	J15	Yes	DQSn6T	DQSn3T/DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	K15	Yes	DQS6T	DQS3T/CQ3T	DQ2T/CQn2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17n	H14	Yes	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17p	J14	Yes	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	L16	Yes	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	M16	Yes	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19n	N16	Yes	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19p	N15	Yes	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	M14	Yes	DQSn7T	DQ4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	N14	Yes	DQS7T	DQ4T/CQn4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T21n	R15	Yes	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T21p	P14	Yes	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	P16	Yes	DQSn8T	DQSn4T/DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	R16	Yes	DQS8T	DQS4T/CQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T23n	N17	Yes	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T23p	P17	Yes	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	R17	Yes	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	T17	Yes	DQ8T	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO				DIFFOUT_T25n	A15	Yes	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T25p	A14	Yes	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	A16	Yes	DQSn9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	B16	Yes	DQS9T	DQ9T/CQn9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27n	A17	Yes	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27p	B17	Yes	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	A18	Yes	DQSn10T	DQSn9T/DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	A19	Yes	DQS10T	DQS9T/CQ9T	DQ9T/CQn9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T29n	B19	Yes	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T29p	A20	Yes	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C18	Yes	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	C19	Yes	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31n	F16	Yes	DQ11T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31p	F15	Yes	DQ11T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	C15	Yes	DQSn11T	DQ10T	DQSn9T/DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	D15	Yes	DQS11T	DQ10T/CQn10T	DQS9T/CQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33n	D16	Yes	DQ11T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33p	E16	Yes	DQ11T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	D17	Yes	DQSn12T	DQSn10T/DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	E17	Yes	DQS12T	DQS10T/CQ10T	DQ9T	DQ9T/CQn9T
7B	VREFB7BN0	IO				DIFFOUT_T35n	D18	Yes	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35p	C17	Yes	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	D19	Yes	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	E19	Yes	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T37n	H17	Yes	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T37p	H16	Yes	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	J16	Yes	DQSn13T	DQ11T	DQ10T	DQSn9T/DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	K16	Yes	DQS13T	DQ11T/CQn11T	DQ10T	DQS9T/CQ9T
7B	VREFB7BN0	IO				DIFFOUT_T39n	F17	Yes	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T39p	G17	Yes	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	G18	Yes	DQSn14T	DQSn11T/DQ11T	DQ10T	DQ9T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
7B	VREFB7BN0	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	H19	Yes	DQS14T	DQS11T/CQ11T	DQ10T/CQn10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T41n	J19	Yes	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T41p	J18	Yes	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	F19	Yes	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	G19	Yes	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T43n	K18	Yes	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T43p	M17	Yes	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T22n	DIFFOUT_T44n	K17	Yes	DQSn15T	DQ12T	DQSn10T/DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T22p	DIFFOUT_T44p	L17	Yes	DQS15T	DQ12T/CQn12T	DQS10T/CQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T45n	K19	Yes	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T45p	N18	Yes	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T23n	DIFFOUT_T46n	M19	Yes	DQSn16T	DQSn12T/DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T23p	DIFFOUT_T46p	N19	Yes	DQS16T	DQS12T/CQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T47n	R19	Yes	DQ16T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T47p	T19	Yes	DQ16T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T24n	DIFFOUT_T48n	P19	Yes	DQ16T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T24p	DIFFOUT_T48p	R18	Yes	DQ16T	DQ12T	DQ10T	DQ9T
7C	VREFB7CN0	IO				DIFFOUT_T49n	B22	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T49p	A21	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	B20	Yes	DQSn17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	C20	Yes	DQS17T	DQ17T/CQn17T		
7C	VREFB7CN0	IO				DIFFOUT_T51n	D22	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T51p	C22	Yes	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	D20	Yes	DQSn18T	DQSn17T/DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	D21	Yes	DQS18T	DQS17T/CQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53n	F22	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53p	E22	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	E20	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	F21	Yes	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T55n	G21	Yes	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T55p	F20	Yes	DQ19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	G20	Yes	DQSn19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	H20	Yes	DQS19T			
7C	VREFB7CN0	IO				DIFFOUT_T57n	H22	Yes	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T57p	J22	Yes	DQ19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T58n	R21	Yes				
7C	VREFB7CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T58p	T21	Yes				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	P20	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	N20	No				
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	P22	No				
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	R22	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	N22	No				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	N21	No				
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	K20	No				
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	L20	No				
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	M21	No				
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	M22	No				
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	J20	No				
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	J21	No				
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	R23	No				
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	P23	No				
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	N24	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	N23	No				
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	J24	No				
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	H23	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	T23	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	R24	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	G25	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	G24	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	M25	No				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	L25	No				
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	K25	Yes				
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	J25	Yes				
8C	VREFB8CN0	IO				DIFFOUT_T72p	G23	Yes	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T72n	F23	Yes	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	E25	Yes	DQS20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	D25	Yes	DQSn20T			
8C	VREFB8CN0	IO				DIFFOUT_T74p	F24	Yes	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T74n	F25	Yes	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	D24	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	D23	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76p	A22	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76n	A23	Yes	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	C23	Yes	DQS21T	DQS22T/CQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	B23	Yes	DQSn21T	DQSn22T/DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78p	A24	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78n	C24	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO	RUP8C		DIFFIO_RX_T40p	DIFFOUT_T79p	B25	Yes	DQS22T	DQ22T/CQn22T		
8C	VREFB8CN0	IO	RDN8C		DIFFIO_RX_T40n	DIFFOUT_T79n	A26	Yes	DQSn22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80p	C25	Yes	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80n	A25	Yes	DQ22T	DQ22T		
8B	VREFB8BN0	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	P25	Yes	DQ23T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	N25	Yes	DQ23T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T82p	R25	Yes	DQ23T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T82n	T25	Yes	DQ23T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	P26	Yes	DQS23T	DQS27T/CQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	N26	Yes	DQSn23T	DQSn27T/DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T84p	K26	Yes	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T84n	N27	Yes	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	M28	Yes	DQS24T	DQ27T/CQn27T	DQS29T/CQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	M27	Yes	DQSn24T	DQ27T	DQSn29T/DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T86p	L26	Yes	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T86n	M26	Yes	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	H26	Yes	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	G26	Yes	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T88p	J26	Yes	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T88n	J27	Yes	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	H28	Yes	DQS25T	DQS28T/CQ28T	DQ29T/CQn29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	G28	Yes	DQSn25T	DQSn28T/DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T90p	F29	Yes	DQ26T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T90n	G29	Yes	DQ26T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	J29	Yes	DQS26T	DQ28T/CQn28T	DQ29T	DQS30T/CQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	H29	Yes	DQSn26T	DQ28T	DQ29T	DQSn30T/DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T92p	J28	Yes	DQ26T	DQ28T	DQ29T	DQ30T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
8B	VREFB8BN0	IO				DIFFOUT_T92n	K28	Yes	DQ26T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	D27	Yes	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	D26	Yes	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94p	F26	Yes	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94n	E26	Yes	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T95p	F28	Yes	DQS27T	DQS29T/CQ29T	DQ30T	DQ30T/CQn30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T95n	F27	Yes	DQSn27T	DQSn29T/DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96p	D28	Yes	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96n	E28	Yes	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49p	DIFFOUT_T97p	D29	Yes	DQS28T	DQ29T/CQn29T	DQS30T/CQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49n	DIFFOUT_T97n	C29	Yes	DQSn28T	DQ29T	DQSn30T/DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98p	E29	Yes	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98n	D30	Yes	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50p	DIFFOUT_T99p	C26	Yes	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50n	DIFFOUT_T99n	B26	Yes	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100p	A27	Yes	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100n	A28	Yes	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51p	DIFFOUT_T101p	C28	Yes	DQS29T	DQS30T/CQ30T	DQ30T/CQn30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51n	DIFFOUT_T101n	B28	Yes	DQSn29T	DQSn30T/DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102p	A29	Yes	DQ30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102n	B29	Yes	DQ30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52p	DIFFOUT_T103p	A31	Yes	DQS30T	DQ30T/CQn30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52n	DIFFOUT_T103n	A30	Yes	DQSn30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104p	C30	Yes	DQ30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104n	B31	Yes	DQ30T	DQ30T	DQ30T	DQ30T
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T105p	T27	Yes	DQ31T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T105n	R27	Yes	DQ31T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T106p	N28	Yes	DQ31T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T106n	P28	Yes	DQ31T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T54p	DIFFOUT_T107p	R28	Yes	DQS31T	DQS35T/CQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T54n	DIFFOUT_T107n	P29	Yes	DQSn31T	DQSn35T/DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T108p	N29	Yes	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T108n	N30	Yes	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	N31	Yes	DQS32T	DQ35T/CQn35T	DQS37T/CQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	M30	Yes	DQSn32T	DQ35T	DQSn37T/DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110p	L29	Yes	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110n	M29	Yes	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	J30	Yes	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	H31	Yes	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112p	K29	Yes	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112n	K30	Yes	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	G31	Yes	DQS33T	DQS36T/CQ36T	DQ37T/CQn37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	G30	Yes	DQSn33T	DQSn36T/DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114p	J32	Yes	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114n	H32	Yes	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	L32	Yes	DQS34T	DQ36T/CQn36T	DQ37T	DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	K31	Yes	DQSn34T	DQ36T	DQ37T	DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116p	J33	Yes	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116n	K32	Yes	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	F31	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	E31	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	D31	Yes	DQ35T	DQ37T	DQ38T	DQ38T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
8A	VREFB8AN0	IO				DIFFOUT_T118n	C31	Yes	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	F32	Yes	DQS35T	DQS37T/CQ37T	DQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	E32	Yes	DQSn35T	DQSn37T/DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	E35	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	G33	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	F34	Yes	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	E34	Yes	DQSn36T	DQ37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	F35	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	F33	Yes	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	D33	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	C33	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	D32	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	C32	Yes	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	B32	Yes	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	A32	Yes	DQSn37T	DQSn38T/DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	A34	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	B34	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	C34	Yes	DQS38T	DQ38T/CQn38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	B35	Yes	DQSn38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128p	C35	Yes	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	D35	Yes	DQ38T	DQ38T	DQ38T	DQ38T
QL3		GXB_TX_L15p					D37	No				
QL3		GXB_TX_L15n					C37	No				
QL3		GXB_RX_L15p					B38	No				
QL3		GXB_RX_L15n					A38	No				
QL3		GXB_TX_L14p					D39	No				
QL3		GXB_TX_L14n					C39	No				
QL3		GXB_RX_L14p					B40	No				
QL3		GXB_RX_L14n					A40	No				
QL3		GXB_CMUTX_L7p					B42	No				
QL3		GXB_CMUTX_L7n					A42	No				
QL3		REFCLK_L7p,GXB_CMURX_L7p					D43	No				
QL3		REFCLK_L7n,GXB_CMURX_L7n					D44	No				
QL3		GXB_CMUTX_L6p					E41	No				
QL3		GXB_CMUTX_L6n					E42	No				
QL3		REFCLK_L6p,GXB_CMURX_L6p					F43	No				
QL3		REFCLK_L6n,GXB_CMURX_L6n					F44	No				
QL3		GXB_TX_L13p					G41	No				
QL3		GXB_TX_L13n					G42	No				
QL3		GXB_RX_L13p					H43	No				
QL3		GXB_RX_L13n					H44	No				
QL3		GXB_TX_L12p					J41	No				
QL3		GXB_TX_L12n					J42	No				
QL3		GXB_RX_L12p					K43	No				
QL3		GXB_RX_L12n					K44	No				
QL2		GXB_TX_L11p					L41	No				
QL2		GXB_TX_L11n					L42	No				
QL2		GXB_RX_L11p					M43	No				
QL2		GXB_RX_L11n					M44	No				
QL2		GXB_TX_L10p					N41	No				
QL2		GXB_TX_L10n					N42	No				
QL2		GXB_RX_L10p					P43	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
QL2		GXB_RX_L10n					P44	No				
QL2		GXB_CMUTX_L5p					R41	No				
QL2		GXB_CMUTX_L5n					R42	No				
QL2		REFCLK_L5p,GXB_CMURX_L5p					T43	No				
QL2		REFCLK_L5n,GXB_CMURX_L5n					T44	No				
QL2		GXB_CMUTX_L4p					U41	No				
QL2		GXB_CMUTX_L4n					U42	No				
QL2		REFCLK_L4p,GXB_CMURX_L4p					V43	No				
QL2		REFCLK_L4n,GXB_CMURX_L4n					V44	No				
QL2		GXB_TX_L9p					W41	No				
QL2		GXB_TX_L9n					W42	No				
QL2		GXB_RX_L9p					Y43	No				
QL2		GXB_RX_L9n					Y44	No				
QL2		GXB_TX_L8p					AA41	No				
QL2		GXB_TX_L8n					AA42	No				
QL2		GXB_RX_L8p					AB43	No				
QL2		GXB_RX_L8n					AB44	No				
QL1		GXB_TX_L7p					AC41	No				
QL1		GXB_TX_L7n					AC42	No				
QL1		GXB_RX_L7p					AD43	No				
QL1		GXB_RX_L7n					AD44	No				
QL1		GXB_TX_L6p					AE41	No				
QL1		GXB_TX_L6n					AE42	No				
QL1		GXB_RX_L6p					AF43	No				
QL1		GXB_RX_L6n					AF44	No				
QL1		GXB_CMUTX_L3p					AG41	No				
QL1		GXB_CMUTX_L3n					AG42	No				
QL1		REFCLK_L3p,GXB_CMURX_L3p					AH43	No				
QL1		REFCLK_L3n,GXB_CMURX_L3n					AH44	No				
QL1		GXB_CMUTX_L2p					AJ41	No				
QL1		GXB_CMUTX_L2n					AJ42	No				
QL1		REFCLK_L2p,GXB_CMURX_L2p					AK43	No				
QL1		REFCLK_L2n,GXB_CMURX_L2n					AK44	No				
QL1		GXB_TX_L5p					AL41	No				
QL1		GXB_TX_L5n					AL42	No				
QL1		GXB_RX_L5p					AM43	No				
QL1		GXB_RX_L5n					AM44	No				
QL1		GXB_TX_L4p					AN41	No				
QL1		GXB_TX_L4n					AN42	No				
QL1		GXB_RX_L4p					AP43	No				
QL1		GXB_RX_L4n					AP44	No				
QL0		GXB_TX_L3p					AR41	No				
QL0		GXB_TX_L3n					AR42	No				
QL0		GXB_RX_L3p					AT43	No				
QL0		GXB_RX_L3n					AT44	No				
QL0		GXB_TX_L2p					AU41	No				
QL0		GXB_TX_L2n					AU42	No				
QL0		GXB_RX_L2p					AV43	No				
QL0		GXB_RX_L2n					AV44	No				
QL0		GXB_CMUTX_L1p					AW41	No				
QL0		GXB_CMUTX_L1n					AW42	No				
QL0		REFCLK_L1p,GXB_CMURX_L1p					AY43	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
QL0		REFCLK_L1n,GXB_CMURX_L1n					AY44	No				
QL0		GXB_CMUTX_L0p					BB43	No				
QL0		GXB_CMUTX_L0n					BB44	No				
QL0		REFCLK_L0p,GXB_CMURX_L0p					BC41	No				
QL0		REFCLK_L0n,GXB_CMURX_L0n					BD41	No				
QL0		GXB_TX_L1p					BA40	No				
QL0		GXB_TX_L1n					BB40	No				
QL0		GXB_RX_L1p					BC39	No				
QL0		GXB_RX_L1n					BD39	No				
QL0		GXB_TX_L0p					BA38	No				
QL0		GXB_TX_L0n					BB38	No				
QL0		GXB_RX_L0p					BC37	No				
QL0		GXB_RX_L0n					BD37	No				
QR0		GXB_RX_R0n					BD8	No				
QR0		GXB_RX_R0p					BC8	No				
QR0		GXB_TX_R0n					BB7	No				
QR0		GXB_TX_R0p					BA7	No				
QR0		GXB_RX_R1n					BD6	No				
QR0		GXB_RX_R1p					BC6	No				
QR0		GXB_TX_R1n					BB5	No				
QR0		GXB_TX_R1p					BA5	No				
QR0		REFCLK_R0n,GXB_CMURX_R0n					BB1	No				
QR0		REFCLK_R0p,GXB_CMURX_R0p					BB2	No				
QR0		GXB_CMUTX_R0n					BD4	No				
QR0		GXB_CMUTX_R0p					BC4	No				
QR0		REFCLK_R1n,GXB_CMURX_R1n					AY1	No				
QR0		REFCLK_R1p,GXB_CMURX_R1p					AY2	No				
QR0		GXB_CMUTX_R1n					AW3	No				
QR0		GXB_CMUTX_R1p					AW4	No				
QR0		GXB_RX_R2n					AV1	No				
QR0		GXB_RX_R2p					AV2	No				
QR0		GXB_TX_R2n					AU3	No				
QR0		GXB_TX_R2p					AU4	No				
QR0		GXB_RX_R3n					AT1	No				
QR0		GXB_RX_R3p					AT2	No				
QR0		GXB_TX_R3n					AR3	No				
QR0		GXB_TX_R3p					AR4	No				
QR1		GXB_RX_R4n					AP1	No				
QR1		GXB_RX_R4p					AP2	No				
QR1		GXB_TX_R4n					AN3	No				
QR1		GXB_TX_R4p					AN4	No				
QR1		GXB_RX_R5n					AM1	No				
QR1		GXB_RX_R5p					AM2	No				
QR1		GXB_TX_R5n					AL3	No				
QR1		GXB_TX_R5p					AL4	No				
QR1		REFCLK_R2n,GXB_CMURX_R2n					AK1	No				
QR1		REFCLK_R2p,GXB_CMURX_R2p					AK2	No				
QR1		GXB_CMUTX_R2n					AJ3	No				
QR1		GXB_CMUTX_R2p					AJ4	No				
QR1		REFCLK_R3n,GXB_CMURX_R3n					AH1	No				
QR1		REFCLK_R3p,GXB_CMURX_R3p					AH2	No				
QR1		GXB_CMUTX_R3n					AG3	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
QR1		GXB_CMUTX_R3p					AG4	No				
QR1		GXB_RX_R6n					AF1	No				
QR1		GXB_RX_R6p					AF2	No				
QR1		GXB_TX_R6n					AE3	No				
QR1		GXB_TX_R6p					AE4	No				
QR1		GXB_RX_R7n					AD1	No				
QR1		GXB_RX_R7p					AD2	No				
QR1		GXB_TX_R7n					AC3	No				
QR1		GXB_TX_R7p					AC4	No				
QR2		GXB_RX_R8n					AB1	No				
QR2		GXB_RX_R8p					AB2	No				
QR2		GXB_TX_R8n					AA3	No				
QR2		GXB_TX_R8p					AA4	No				
QR2		GXB_RX_R9n					Y1	No				
QR2		GXB_RX_R9p					Y2	No				
QR2		GXB_TX_R9n					W3	No				
QR2		GXB_TX_R9p					W4	No				
QR2		REFCLK_R4n,GXB_CMURX_R4n					V1	No				
QR2		REFCLK_R4p,GXB_CMURX_R4p					V2	No				
QR2		GXB_CMUTX_R4n					U3	No				
QR2		GXB_CMUTX_R4p					U4	No				
QR2		REFCLK_R5n,GXB_CMURX_R5n					T1	No				
QR2		REFCLK_R5p,GXB_CMURX_R5p					T2	No				
QR2		GXB_CMUTX_R5n					R3	No				
QR2		GXB_CMUTX_R5p					R4	No				
QR2		GXB_RX_R10n					P1	No				
QR2		GXB_RX_R10p					P2	No				
QR2		GXB_TX_R10n					N3	No				
QR2		GXB_TX_R10p					N4	No				
QR2		GXB_RX_R11n					M1	No				
QR2		GXB_RX_R11p					M2	No				
QR2		GXB_TX_R11n					L3	No				
QR2		GXB_TX_R11p					L4	No				
QR3		GXB_RX_R12n					K1	No				
QR3		GXB_RX_R12p					K2	No				
QR3		GXB_TX_R12n					J3	No				
QR3		GXB_TX_R12p					J4	No				
QR3		GXB_RX_R13n					H1	No				
QR3		GXB_RX_R13p					H2	No				
QR3		GXB_TX_R13n					G3	No				
QR3		GXB_TX_R13p					G4	No				
QR3		REFCLK_R6n,GXB_CMURX_R6n					F1	No				
QR3		REFCLK_R6p,GXB_CMURX_R6p					F2	No				
QR3		GXB_CMUTX_R6n					E3	No				
QR3		GXB_CMUTX_R6p					E4	No				
QR3		REFCLK_R7n,GXB_CMURX_R7n					D1	No				
QR3		REFCLK_R7p,GXB_CMURX_R7p					D2	No				
QR3		GXB_CMUTX_R7n					A3	No				
QR3		GXB_CMUTX_R7p					B3	No				
QR3		GXB_RX_R14n					A5	No				
QR3		GXB_RX_R14p					B5	No				
QR3		GXB_TX_R14n					C6	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
QR3		GXB_TX_R14p					D6	No				
QR3		GXB_RX_R15n					A7	No				
QR3		GXB_RX_R15p					B7	No				
QR3		GXB_TX_R15n					C8	No				
QR3		GXB_TX_R15p					D8	No				
		GND					W37	No				
		GND					Y37	No				
		GND					AY10	No				
		GND					V8	No				
		GND					AB23	No				
		GND					BC12	No				
		GND					BC15	No				
		GND					BC18	No				
		GND					BC21	No				
		GND					BC24	No				
		GND					BC27	No				
		GND					BC30	No				
		GND					BC33	No				
		GND					AY12	No				
		GND					AY15	No				
		GND					AY18	No				
		GND					AY21	No				
		GND					AY24	No				
		GND					AY27	No				
		GND					AY30	No				
		GND					AY33	No				
		GND					AV9	No				
		GND					AV36	No				
		GND					AU7	No				
		GND					AU12	No				
		GND					AU15	No				
		GND					AU18	No				
		GND					AU21	No				
		GND					AU24	No				
		GND					AU30	No				
		GND					AU33	No				
		GND					AU38	No				
		GND					AT27	No				
		GND					AR9	No				
		GND					AR36	No				
		GND					AP7	No				
		GND					AP12	No				
		GND					AP15	No				
		GND					AP18	No				
		GND					AP21	No				
		GND					AP24	No				
		GND					AP27	No				
		GND					AP30	No				
		GND					AP33	No				
		GND					AP38	No				
		GND					AM9	No				
		GND					AM36	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					AL7	No				
		GND					AL12	No				
		GND					AL15	No				
		GND					AL18	No				
		GND					AL21	No				
		GND					AL24	No				
		GND					AL27	No				
		GND					AL30	No				
		GND					AL33	No				
		GND					AL38	No				
		GND					AJ15	No				
		GND					AH7	No				
		GND					AH13	No				
		GND					AH17	No				
		GND					AH19	No				
		GND					AH21	No				
		GND					AH23	No				
		GND					AH25	No				
		GND					AH27	No				
		GND					AH29	No				
		GND					AH32	No				
		GND					AH38	No				
		GND					AG16	No				
		GND					AG18	No				
		GND					AG20	No				
		GND					AG22	No				
		GND					AG24	No				
		GND					AG26	No				
		GND					AG28	No				
		GND					AF17	No				
		GND					AF19	No				
		GND					AF21	No				
		GND					AF23	No				
		GND					AF25	No				
		GND					AF27	No				
		GND					AF31	No				
		GND					AE7	No				
		GND					AE13	No				
		GND					AE15	No				
		GND					AE18	No				
		GND					AE20	No				
		GND					AE22	No				
		GND					AE24	No				
		GND					AE26	No				
		GND					AE28	No				
		GND					AE32	No				
		GND					AE38	No				
		GND					AD17	No				
		GND					AD19	No				
		GND					AD21	No				
		GND					AD23	No				
		GND					AD25	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					AD27	No				
		GND					AC18	No				
		GND					AC20	No				
		GND					AC24	No				
		GND					AC26	No				
		GND					AC28	No				
		GND					AC30	No				
		GND					AB7	No				
		GND					AB13	No				
		GND					AB15	No				
		GND					AB17	No				
		GND					AB19	No				
		GND					AB21	No				
		GND					AB25	No				
		GND					AB27	No				
		GND					AB32	No				
		GND					AB35	No				
		GND					AB38	No				
		GND					AA18	No				
		GND					AA20	No				
		GND					AA22	No				
		GND					AA24	No				
		GND					AA26	No				
		GND					AA28	No				
		GND					Y17	No				
		GND					Y19	No				
		GND					Y21	No				
		GND					Y23	No				
		GND					Y25	No				
		GND					Y27	No				
		GND					Y30	No				
		GND					W7	No				
		GND					W13	No				
		GND					W15	No				
		GND					W18	No				
		GND					W20	No				
		GND					W22	No				
		GND					W24	No				
		GND					W26	No				
		GND					W28	No				
		GND					W32	No				
		GND					W39	No				
		GND					V17	No				
		GND					V19	No				
		GND					V21	No				
		GND					V23	No				
		GND					V25	No				
		GND					V27	No				
		GND					V29	No				
		GND					U16	No				
		GND					U18	No				
		GND					U20	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					U22	No				
		GND					U24	No				
		GND					U26	No				
		GND					U28	No				
		GND					T7	No				
		GND					T13	No				
		GND					T29	No				
		GND					T32	No				
		GND					T38	No				
		GND					P12	No				
		GND					P15	No				
		GND					P18	No				
		GND					P21	No				
		GND					P24	No				
		GND					P27	No				
		GND					P30	No				
		GND					P33	No				
		GND					N7	No				
		GND					N9	No				
		GND					N36	No				
		GND					N38	No				
		GND					L12	No				
		GND					L15	No				
		GND					L18	No				
		GND					L21	No				
		GND					L24	No				
		GND					L27	No				
		GND					L30	No				
		GND					L33	No				
		GND					K7	No				
		GND					K9	No				
		GND					K36	No				
		GND					K38	No				
		GND					H12	No				
		GND					H15	No				
		GND					H18	No				
		GND					H21	No				
		GND					H24	No				
		GND					H27	No				
		GND					H30	No				
		GND					H33	No				
		GND					G7	No				
		GND					G9	No				
		GND					G36	No				
		GND					G38	No				
		GND					E12	No				
		GND					E15	No				
		GND					E18	No				
		GND					E21	No				
		GND					E24	No				
		GND					E27	No				
		GND					E30	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					E33	No				
		GND					B12	No				
		GND					B15	No				
		GND					B18	No				
		GND					B21	No				
		GND					B24	No				
		GND					B27	No				
		GND					B30	No				
		GND					B33	No				
		GND					A43	No				
		GND					BD36	No				
		GND					BD38	No				
		GND					BD40	No				
		GND					BD42	No				
		GND					BC36	No				
		GND					BC38	No				
		GND					BC40	No				
		GND					BC42	No				
		GND					BC43	No				
		GND					BB36	No				
		GND					BB37	No				
		GND					BB39	No				
		GND					BB41	No				
		GND					BB42	No				
		GND					BA37	No				
		GND					BA39	No				
		GND					BA41	No				
		GND					BA42	No				
		GND					BA43	No				
		GND					BA44	No				
		GND					AY41	No				
		GND					AY42	No				
		GND					AW43	No				
		GND					AW44	No				
		GND					AV41	No				
		GND					AV42	No				
		GND					AU43	No				
		GND					AU44	No				
		GND					AT41	No				
		GND					AT42	No				
		GND					AR43	No				
		GND					AR44	No				
		GND					AP41	No				
		GND					AP42	No				
		GND					AN43	No				
		GND					AN44	No				
		GND					AM41	No				
		GND					AM42	No				
		GND					AL43	No				
		GND					AL44	No				
		GND					AK41	No				
		GND					AK42	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					AJ35	No				
		GND					AJ43	No				
		GND					AJ44	No				
		GND					AH41	No				
		GND					AH42	No				
		GND					AG34	No				
		GND					AG36	No				
		GND					AG43	No				
		GND					AG44	No				
		GND					AF41	No				
		GND					AF42	No				
		GND					AE35	No				
		GND					AE43	No				
		GND					AE44	No				
		GND					AD41	No				
		GND					AD42	No				
		GND					AC34	No				
		GND					AC36	No				
		GND					AC43	No				
		GND					AC44	No				
		GND					AB41	No				
		GND					AB42	No				
		GND					AA35	No				
		GND					AA43	No				
		GND					AA44	No				
		GND					Y41	No				
		GND					Y42	No				
		GND					W34	No				
		GND					W36	No				
		GND					W43	No				
		GND					W44	No				
		GND					V41	No				
		GND					V42	No				
		GND					U35	No				
		GND					U43	No				
		GND					U44	No				
		GND					T41	No				
		GND					T42	No				
		GND					R34	No				
		GND					R36	No				
		GND					R43	No				
		GND					R44	No				
		GND					P41	No				
		GND					P42	No				
		GND					N43	No				
		GND					N44	No				
		GND					M41	No				
		GND					M42	No				
		GND					L43	No				
		GND					L44	No				
		GND					K41	No				
		GND					K42	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					J43	No				
		GND					J44	No				
		GND					H41	No				
		GND					H42	No				
		GND					G43	No				
		GND					G44	No				
		GND					F41	No				
		GND					F42	No				
		GND					E43	No				
		GND					E44	No				
		GND					D36	No				
		GND					D38	No				
		GND					D40	No				
		GND					D41	No				
		GND					D42	No				
		GND					C36	No				
		GND					C38	No				
		GND					C40	No				
		GND					C41	No				
		GND					C42	No				
		GND					C43	No				
		GND					C44	No				
		GND					B37	No				
		GND					B39	No				
		GND					B41	No				
		GND					B43	No				
		GND					A37	No				
		GND					A39	No				
		GND					A41	No				
		GND					BC44	No				
		GND					AA40	No				
		GND					AC40	No				
		GND					AG40	No				
		GND					AL40	No				
		GND					AN40	No				
		GND					AT40	No				
		GND					AU40	No				
		GND					AV40	No				
		GND					AA36	No				
		GND					AA37	No				
		GND					AB36	No				
		GND					AB37	No				
		GND					AC37	No				
		GND					AE36	No				
		GND					AE33	No				
		GND					AF37	No				
		GND					AF36	No				
		GND					AF35	No				
		GND					AF34	No				
		GND					AF33	No				
		GND					AG33	No				
		GND					AH37	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					AJ37	No				
		GND					AJ36	No				
		GND					AJ33	No				
		GND					AK36	No				
		GND					AK35	No				
		GND					AK34	No				
		GND					AK33	No				
		GND					W40	No				
		GND					AD40	No				
		GND					A8	No				
		GND					BD3	No				
		GND					BD5	No				
		GND					BD7	No				
		GND					BD9	No				
		GND					BC1	No				
		GND					BC2	No				
		GND					BC3	No				
		GND					BC5	No				
		GND					BC7	No				
		GND					BC9	No				
		GND					BB3	No				
		GND					BB4	No				
		GND					BB6	No				
		GND					BB8	No				
		GND					BB9	No				
		GND					BA1	No				
		GND					BA2	No				
		GND					BA3	No				
		GND					BA4	No				
		GND					BA6	No				
		GND					BA8	No				
		GND					AY3	No				
		GND					AY4	No				
		GND					AW1	No				
		GND					AW2	No				
		GND					AV3	No				
		GND					AV4	No				
		GND					AU1	No				
		GND					AU2	No				
		GND					AT3	No				
		GND					AT4	No				
		GND					AR1	No				
		GND					AR2	No				
		GND					AP3	No				
		GND					AP4	No				
		GND					AN1	No				
		GND					AN2	No				
		GND					AM3	No				
		GND					AM4	No				
		GND					AL1	No				
		GND					AL2	No				
		GND					AK3	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					AK4	No				
		GND					AJ1	No				
		GND					AJ2	No				
		GND					AJ10	No				
		GND					AH3	No				
		GND					AH4	No				
		GND					AG1	No				
		GND					AG2	No				
		GND					AG9	No				
		GND					AG11	No				
		GND					AF3	No				
		GND					AF4	No				
		GND					AE1	No				
		GND					AE2	No				
		GND					AE10	No				
		GND					AD3	No				
		GND					AD4	No				
		GND					AC1	No				
		GND					AC2	No				
		GND					AC9	No				
		GND					AC11	No				
		GND					AB3	No				
		GND					AB4	No				
		GND					AA1	No				
		GND					AA2	No				
		GND					AA10	No				
		GND					Y3	No				
		GND					Y4	No				
		GND					W1	No				
		GND					W2	No				
		GND					W9	No				
		GND					W11	No				
		GND					V3	No				
		GND					V4	No				
		GND					U1	No				
		GND					U2	No				
		GND					U10	No				
		GND					T3	No				
		GND					T4	No				
		GND					R1	No				
		GND					R2	No				
		GND					R9	No				
		GND					R11	No				
		GND					P3	No				
		GND					P4	No				
		GND					N1	No				
		GND					N2	No				
		GND					M3	No				
		GND					M4	No				
		GND					L1	No				
		GND					L2	No				
		GND					K3	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					K4	No				
		GND					J1	No				
		GND					J2	No				
		GND					H3	No				
		GND					H4	No				
		GND					G1	No				
		GND					G2	No				
		GND					F3	No				
		GND					F4	No				
		GND					E1	No				
		GND					E2	No				
		GND					D3	No				
		GND					D4	No				
		GND					D5	No				
		GND					D7	No				
		GND					D9	No				
		GND					C1	No				
		GND					C2	No				
		GND					C3	No				
		GND					C4	No				
		GND					C5	No				
		GND					C7	No				
		GND					C9	No				
		GND					B2	No				
		GND					B4	No				
		GND					B6	No				
		GND					B8	No				
		GND					A2	No				
		GND					A4	No				
		GND					A6	No				
		GND					E8	No				
		GND					E7	No				
		GND					K5	No				
		GND					AA5	No				
		GND					AC5	No				
		GND					AG5	No				
		GND					AL5	No				
		GND					AN5	No				
		GND					AT5	No				
		GND					AU5	No				
		GND					AV5	No				
		GND					AK12	No				
		GND					AK11	No				
		GND					AK10	No				
		GND					AK9	No				
		GND					AK8	No				
		GND					AJ12	No				
		GND					AJ9	No				
		GND					AJ8	No				
		GND					AH12	No				
		GND					AH8	No				
		GND					AG8	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		GND					AF12	No				
		GND					AF11	No				
		GND					AF10	No				
		GND					AF9	No				
		GND					AE9	No				
		GND					AE8	No				
		GND					AC8	No				
		GND					AB11	No				
		GND					AB10	No				
		GND					AB9	No				
		GND					AB8	No				
		GND					AA9	No				
		GND					AA8	No				
		GND					Y8	No				
		GND					U9	No				
		GND					W5	No				
		GND					AD5	No				
		VCC					AB22	No				
		VCC					AH18	No				
		VCC					AH28	No				
		VCC					AG17	No				
		VCC					AG21	No				
		VCC					AG23	No				
		VCC					AG25	No				
		VCC					AG27	No				
		VCC					AF18	No				
		VCC					AF20	No				
		VCC					AF22	No				
		VCC					AF24	No				
		VCC					AF28	No				
		VCC					AE17	No				
		VCC					AE21	No				
		VCC					AE23	No				
		VCC					AE25	No				
		VCC					AE27	No				
		VCC					AD18	No				
		VCC					AD20	No				
		VCC					AD22	No				
		VCC					AD24	No				
		VCC					AD28	No				
		VCC					AC17	No				
		VCC					AC21	No				
		VCC					AC23	No				
		VCC					AC25	No				
		VCC					AC27	No				
		VCC					AB18	No				
		VCC					AB20	No				
		VCC					AB24	No				
		VCC					AB28	No				
		VCC					AA17	No				
		VCC					AA21	No				
		VCC					AA23	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		VCC					AA25	No				
		VCC					AA27	No				
		VCC					Y18	No				
		VCC					Y20	No				
		VCC					Y22	No				
		VCC					Y24	No				
		VCC					Y28	No				
		VCC					W17	No				
		VCC					W21	No				
		VCC					W23	No				
		VCC					W25	No				
		VCC					W27	No				
		VCC					V16	No				
		VCC					V18	No				
		VCC					V20	No				
		VCC					V22	No				
		VCC					V24	No				
		VCC					V28	No				
		VCC					U17	No				
		VCC					U27	No				
		VCC					U29	No				
		VCC					T28	No				
		VCC					AJ23	No				
		VCC					AH20	No				
		VCC					AH22	No				
		VCC					AH24	No				
		VCC					AH26	No				
		VCC					AG19	No				
		VCC					AF26	No				
		VCC					AE19	No				
		VCC					AD26	No				
		VCC					AC19	No				
		VCC					AB26	No				
		VCC					AA19	No				
		VCC					Y26	No				
		VCC					W19	No				
		VCC					V26	No				
		VCC					U19	No				
		VCC					U21	No				
		VCC					U23	No				
		VCC					U25	No				
		VCC					T22	No				
		VCC					AH34	No				
		VCC					AJ34	No				
		VCC					AE34	No				
		VCC					Y34	No				
		VCC					U34	No				
		VCC					T34	No				
		VCC					AJ11	No				
		VCC					AH11	No				
		VCC					AE11	No				
		VCC					Y11	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		VCC					U11	No				
		VCC					T11	No				
		VCCPT					AC31	No				
		VCCPT					AC32	No				
		VCCPT					AT22	No				
		VCCPT					AC13	No				
		VCCPT					AC14	No				
		VCCPT					J23	No				
		DNU					AC22	No				
		VCCPGM					AM32	No				
		VCCPGM					AM13	No				
		TEMPDIODEn					G11	No				
		TEMPDIODEp					B9	No				
		VCC_CLKIN3C					AR24	No				
		VCC_CLKIN4C					AR21	No				
		VCC_CLKIN7C					K21	No				
		VCC_CLKIN8C					K24	No				
		VCCBAT					L13	No				
		VCCA_PLL_B1					AR23	No				
		VCCA_PLL_B2					AR22	No				
		VCCA_PLL_L1					M32	No				
		VCCA_PLL_L2					AA32	No				
		VCCA_PLL_L3					AD32	No				
		VCCA_PLL_L4					AP32	No				
		VCCA_PLL_R1					M13	No				
		VCCA_PLL_R2					AA13	No				
		VCCA_PLL_R3					AE12	No				
		VCCA_PLL_R4					AP13	No				
		VCCA_PLL_T1					K23	No				
		VCCA_PLL_T2					K22	No				
		VCCD_PLL_B1					AP23	No				
		VCCD_PLL_B2					AP22	No				
		VCCD_PLL_L1					N32	No				
		VCCD_PLL_L2					AB31	No				
		VCCD_PLL_L3					AD31	No				
		VCCD_PLL_L4					AN32	No				
		VCCD_PLL_R1					N13	No				
		VCCD_PLL_R2					AB14	No				
		VCCD_PLL_R3					AD13	No				
		VCCD_PLL_R4					AN13	No				
		VCCD_PLL_T1					L23	No				
		VCCD_PLL_T2					L22	No				
		VCCIO1A					U31	No				
		VCCIO1A					M34	No				
		VCCIO1A					L37	No				
		VCCIO1A					H35	No				
		VCCIO1A					H39	No				
		VCCIO1C					V33	No				
		VCCIO1C					V38	No				
		VCCIO1C					T37	No				
		VCCIO1C					N37	No				
		VCCIO2A					AV39	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		VCCIO2A					AT35	No				
		VCCIO2A					AR38	No				
		VCCIO2A					AN36	No				
		VCCIO2A					AM34	No				
		VCCIO2B					AL37	No				
		VCCIO2B					AH33	No				
		VCCIO2C					AJ38	No				
		VCCIO2C					AG37	No				
		VCCIO2C					AD37	No				
		VCCIO2C					AB34	No				
		VCCIO3A					BB34	No				
		VCCIO3A					AW32	No				
		VCCIO3A					AV30	No				
		VCCIO3A					AP29	No				
		VCCIO3A					AL31	No				
		VCCIO3B					BB29	No				
		VCCIO3B					BB27	No				
		VCCIO3B					AW27	No				
		VCCIO3B					AT28	No				
		VCCIO3B					AN27	No				
		VCCIO3C					BB24	No				
		VCCIO3C					AU25	No				
		VCCIO3C					AK25	No				
		VCCIO4A					AW13	No				
		VCCIO4A					BB11	No				
		VCCIO4A					AT15	No				
		VCCIO4A					AN16	No				
		VCCIO4A					AL16	No				
		VCCIO4B					BB16	No				
		VCCIO4B					BB19	No				
		VCCIO4B					AV17	No				
		VCCIO4B					AR18	No				
		VCCIO4B					AK19	No				
		VCCIO4C					AV21	No				
		VCCIO4C					BA21	No				
		VCCIO4C					AN21	No				
		VCCIO5A					AU6	No				
		VCCIO5A					AP8	No				
		VCCIO5A					AN10	No				
		VCCIO5A					AK13	No				
		VCCIO5A					AH15	No				
		VCCIO5B					AM8	No				
		VCCIO5B					AF14	No				
		VCCIO5C					AF8	No				
		VCCIO5C					AD8	No				
		VCCIO5C					AC7	No				
		VCCIO5C					Y7	No				
		VCCIO6A					T12	No				
		VCCIO6A					T14	No				
		VCCIO6A					N11	No				
		VCCIO6A					L8	No				
		VCCIO6A					J10	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		VCCIO6C					Y13	No				
		VCCIO6C					W8	No				
		VCCIO6C					T8	No				
		VCCIO6C					M7	No				
		VCCIO7A					C11	No				
		VCCIO7A					K14	No				
		VCCIO7A					G13	No				
		VCCIO7A					E10	No				
		VCCIO7A					D13	No				
		VCCIO7B					C16	No				
		VCCIO7B					M18	No				
		VCCIO7B					J17	No				
		VCCIO7B					G16	No				
		VCCIO7B					F18	No				
		VCCIO7C					C21	No				
		VCCIO7C					R20	No				
		VCCIO7C					G22	No				
		VCCIO8A					G32	No				
		VCCIO8A					M31	No				
		VCCIO8A					J31	No				
		VCCIO8A					D34	No				
		VCCIO8A					A33	No				
		VCCIO8B					G27	No				
		VCCIO8B					R26	No				
		VCCIO8B					K27	No				
		VCCIO8B					F30	No				
		VCCIO8B					C27	No				
		VCCIO8C					E23	No				
		VCCIO8C					M24	No				
		VCCIO8C					H25	No				
		VCCPD1A					W29	No				
		VCCPD1C					AA29	No				
		VCCPD2A					AG29	No				
		VCCPD2B					AE29	No				
		VCCPD2C					AC29	No				
		VCCPD3A					AJ29	No				
		VCCPD3B					AJ27	No				
		VCCPD3C					AJ25	No				
		VCCPD4A					AJ17	No				
		VCCPD4B					AJ19	No				
		VCCPD4C					AJ21	No				
		VCCPD5A					AH16	No				
		VCCPD5B					AF16	No				
		VCCPD5C					AD16	No				
		VCCPD6A					Y16	No				
		VCCPD6C					AB16	No				
		VCCPD7A					T16	No				
		VCCPD7B					T18	No				
		VCCPD7C					T20	No				
		VCCPD8A					R29	No				
		VCCPD8B					T26	No				
		VCCPD8C					T24	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				R32	No				
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				Y33	No				
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AG30	No				
2B	VREFB2BN0	VREFB2BN0	VREFB2BN0				AK37	No				
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				AE37	No				
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AP31	No				
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AP26	No				
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AN25	No				
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AP14	No				
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AR17	No				
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AN22	No				
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AM10	No				
5B	VREFB5BN0	VREFB5BN0	VREFB5BN0				AG12	No				
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AF7	No				
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				K10	No				
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				R7	No				
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				M15	No				
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				L19	No				
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				M20	No				
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				L31	No				
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				L28	No				
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				M23	No				
		NC					A35	No				
		NC					BA35	No				
		NC					AW11	No				
		NC					A10	No				
		NC					AW39	No				
		NC					AW40	No				
		NC					AW6	No				
		NC					AW5	No				
		NC					AJ26	No				
		NC					AJ28	No				
		NC					AF29	No				
		NC					AC16	No				
		NC					AB29	No				
		NC					AA16	No				
		NC					Y29	No				
		NC					W16	No				
		NC					E39	No				
		NC					E40	No				
		NC					E6	No				
		NC					E5	No				
		VCCAUX					K33	No				
		VCCAUX					AR33	No				
		VCCAUX					AR12	No				
		VCCAUX					K12	No				
		VCCA_L					AK40	No				
		VCCA_L					V40	No				
		VCCA_L					AJ40	No				
		VCCA_L					U40	No				
		VCCA_R					V5	No				
		VCCA_R					AK5	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		VCCA_R					U5	No				
		VCCA_R					AJ5	No				
		VCCH_GXBL0					AH36	No				
		VCCH_GXBL1					AD36	No				
		VCCH_GXBL2					Y36	No				
		VCCH_GXBL3					T36	No				
		VCCH_GXBR0					AH9	No				
		VCCH_GXBR1					AD9	No				
		VCCH_GXBR2					Y9	No				
		VCCH_GXBR3					T9	No				
		VCCL_GXBL0					AG35	No				
		VCCL_GXBL0					AH35	No				
		VCCL_GXBL1					AC35	No				
		VCCL_GXBL1					AD35	No				
		VCCL_GXBL2					W35	No				
		VCCL_GXBL2					Y35	No				
		VCCL_GXBL3					R35	No				
		VCCL_GXBL3					T35	No				
		VCCL_GXBR0					AG10	No				
		VCCL_GXBR0					AH10	No				
		VCCL_GXBR1					AC10	No				
		VCCL_GXBR1					AD10	No				
		VCCL_GXBR2					W10	No				
		VCCL_GXBR2					Y10	No				
		VCCL_GXBR3					R10	No				
		VCCL_GXBR3					T10	No				
		VCCR_L					T40	No				
		VCCR_L					AB40	No				
		VCCR_L					AH40	No				
		VCCR_L					AP40	No				
		VCCR_L					AR40	No				
		VCCR_R					T5	No				
		VCCR_R					AB5	No				
		VCCR_R					AH5	No				
		VCCR_R					AP5	No				
		VCCR_R					AR5	No				
		VCCT_L					P40	No				
		VCCT_L					Y40	No				
		VCCT_L					AF40	No				
		VCCT_L					AM40	No				
		VCCT_L					AE40	No				
		VCCT_R					P5	No				
		VCCT_R					Y5	No				
		VCCT_R					AF5	No				
		VCCT_R					AM5	No				
		VCCT_R					AE5	No				
		VCCHIP_L					AA34	No				
		VCCHIP_L					AB33	No				
		VCCHIP_L					AC33	No				
		VCCHIP_L					AD34	No				
		VCCHIP_L					AD33	No				
		VCCHIP_R					AA11	No				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1932	Dynamic OCT Support	DQS for X4 for F1932	DQS for X8/X9 for F1932	DQS for X16/ X18 for F1932	DQS for X32/ X36 for F1932
		VCCHIP_R					AB12	No				
		VCCHIP_R					AC12	No				
		VCCHIP_R					AD12	No				
		VCCHIP_R					AD11	No				
		RREF_L0					BD43	No				
		RREF_L1					B44	No				
		RREF_R0					BD2	No				
		RREF_R1					B1	No				

Notes:
(1) If the p pin or n pin is not available, the particular differential pair is not supported.
(2) Pins with * can be used as clock pins when the data rate for the transceiver blocks is below 6.5 Gbps.

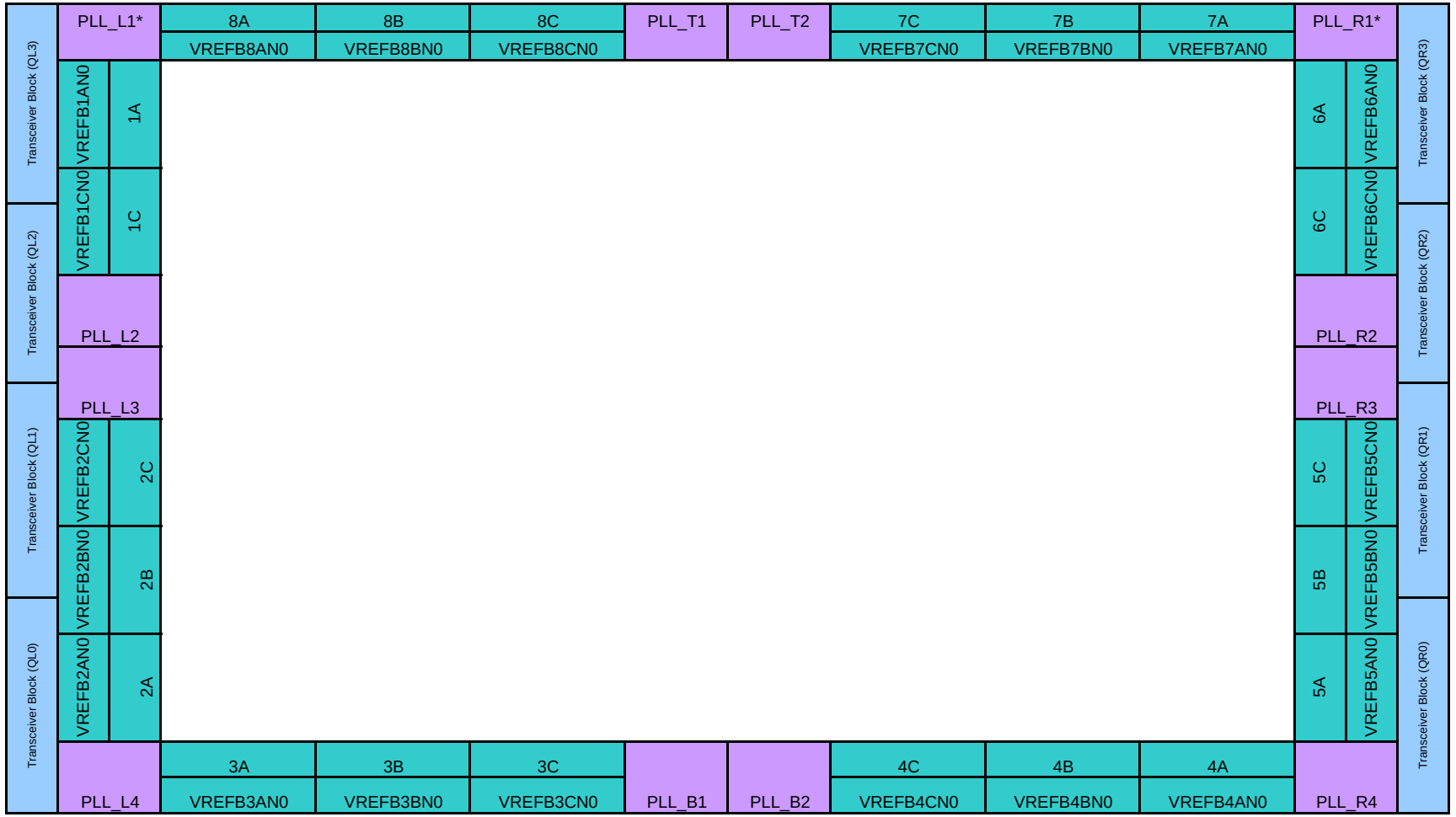
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[4:7,9, 11:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L4,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L4 and R4 respectively.
PLL_[L4,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L4 and R4 respectively.
PLL_[L1, L2, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[0:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
	Optional/Dual-Purpose Configuration Pins	
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn (Note 6)	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE (Note 6)	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0 (Note 6)	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[1:7] (Note 6)	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR (Note 6)	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[##][T,B], DQS[##][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B], DQSn[##][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B], DQ[##][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B], CQ[##][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[##][T,B], CQn[##][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, (Note 7) RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, (Note 7) RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
GND	Ground	Device ground pins.
VREF[1:8][A,C]N0, VREF[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
Transceiver (I/O Banks) Pins		
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers, specific to left (L) side and right (R) side.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p (Note 3)	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n (Note 3)	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p (Note 3)	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n (Note 3)	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p, GXB_CMURX_[L,R][0:7]p (Note 3 and 4)	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n, GXB_CMURX_[L,R][0:7]n (Note 3 and 4)	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p, (Note 4) GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

1. This pin definition is prepared based on the EP4S100G5.
2. Some of the pull-up /pull down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
   The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
   Refer to the Configuring Stratix IV GX Devices chapter in the Stratix IV GX Device Handbook for more information.
3. Transceiver signals GXB_RX[15..0] and GXB_TX[15..0] are device specific.
4. Dual purpose CMU Receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th channels.
5. Refer to pin connections guidelines and data sheet for the recommended operating voltage.
6. Although some configuration pins may indicate that they serve as dual purpose (I/O and configuration) pins, this functionality is device dependent.
   Refer to the pin list to determine if the regular I/O function is available for the specific dual-purpose configuration pin.
7. The regular I/O function is not available for some of these reference pins. The availability of the regular I/O function on these reference pins is device dependent.
   Refer to the pin list to determine if the regular I/O function is available for the specific reference pin.



Notes:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
2. PLLs with * do not have dedicated input pins.

Version Number	Date	Changes Made
1.0	9/18/2009	Initial release.
1.1	12/3/2009	- Added bank number for JTAG pins. - Added Note (6) and Note (7) in Pin Definitions. - Grouped nCSO, ASDO, and DCLK into dedicated configuration/JTAG pins in Pin Definitions.
1.2	10/10/2013	- Marked * to pin AY5, AY6, AY39, and AY40 in F1932 package. - Added note to F1932 package.
1.3	2/4/2015	Added the Dynamic OCT Support column in the Pin List.