Pin Information for the Stratix® IV GT EP4S100G2ES1 Device
Version 1.2
Notes (1), (2), (3)
WARNING: For ES1 silicon only

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
1A		TDI		TDI			J29	No			
1A		TMS		TMS			N27	No			
1A		TRST		TRST			A32	No			
1A		TCK		TCK			G30	No			
1A		TDO		TDO			F30	No			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	K29	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	L29	Yes			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C34	Yes			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D34	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J30	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	K30	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	C31	Yes	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D31	Yes	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	M28	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	N28	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	H32	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J32	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	B32	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	C32	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M31	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	N31	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	C33	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D33	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	M30	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	N30	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	G31	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	H31	Yes	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	M29	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	N29	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	E31	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F31	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	K31	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L31	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	E32	Yes	DQSn5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	F32	Yes	DQS5L	DQ3L/CQn3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	R28	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	T28	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	E34	Yes	DQSn6L	DQSn3L/DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	F34	Yes	DQS6L	DQS3L/CQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	R27	Yes	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	T27	Yes	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	J33	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	K32	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	F33	Yes	DQSn7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	G33	Yes	DQS7L		

Pin Information for the Stratix® IV GT EP4S100G2ES1 Device
Version 1.2
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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	P29	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	R29	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	H34	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	L32	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	M32	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	P32	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	P31	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	T30	Yes	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	N34	Yes	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	N33	Yes	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	M34	Yes	DQSn10L	DQ9L	DQSn8L/DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	M33	Yes	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	V28	Yes	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	W28	Yes	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	L34	Yes	DQS11L	DQS9L/CQ9L	DQ8L
1C	VREFB1CN0	IO		CLKUSR			R31	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R30	Yes	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	W30	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	W29	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA2			N35	Yes			
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	P34	Yes	DQS12L	DQ10L/CQn10L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	V27	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	W26	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA6			R35	Yes			
1C	VREFB1CN0	IO		DATA7			R34	Yes			
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	V30	Yes	DQ13L	DQ10L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	V29	Yes	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_OE			U35	Yes			
1C	VREFB1CN0	IO		DEV_CLRn			V34	Yes			
1C	VREFB1CN0	CLK1n	CLK1n				AA35	No			
1C	VREFB1CN0	CLK1p	CLK1p				AB34	No			
2C	VREFB2CN0	CLK3p	CLK3p				AC34	No			
2C	VREFB2CN0	CLK3n	CLK3n				AC35	No			
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AB30	Yes	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AB27	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AB28	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	AC28	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	AC29	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AK34	Yes	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	AL34	Yes	DQS16L	DQS18L/CQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AD28	Yes	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AD29	Yes	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29p	DIFFOUT_L57p	AH32	Yes	DQS17L	DQ18L/CQn18L	DQS19L/CQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29n	DIFFOUT_L57n	AH33	Yes	DQSn17L	DQ18L	DQSn19L/DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L29p	DIFFOUT_L58p	AE28	Yes	DQ17L	DQ18L	DQ19L

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
2C	VREFB2CN0	IO			DIFFIO_TX_L29n	DIFFOUT_L58n	AE29	Yes	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AN34	Yes	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	AD30	Yes	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AM34	Yes	DQS18L	DQS19L/CQ19L	DQ19L/CQn19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AF29	Yes	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AG30	Yes	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	AJ32	Yes	DQS19L	DQ19L/CQn19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32n	DIFFOUT_L63n	AK33	Yes	DQSn19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AE30	Yes	DQ19L	DQ19L	DQ19L
2A	VREFB2AN0	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AN32	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	AP33	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L33p	DIFFOUT_L66p	AC26	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L33n	DIFFOUT_L66n	AD26	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AN33	Yes	DQS20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34n	DIFFOUT_L67n	AP34	Yes	DQSn20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AD27	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AE27	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AT34	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AR34	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AJ31	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AH30	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AT33	Yes	DQS21L	DQS24L/CQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L36n	DIFFOUT_L71n	AU33	Yes	DQSn21L	DQSn24L/DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AK32	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36n	DIFFOUT_L72n	AL32	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AG29	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AH29	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AP32	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AR32	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AK31	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AL31	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	AN30	Yes	DQS23L	DQS25L/CQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	AP30	Yes	DQSn23L	DQSn25L/DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	AE26	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	AF26	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AM31	Yes	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AN31	Yes	DQSn24L	DQ25L	DQSn26L/DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AK30	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AL30	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AT31	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AU31	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AG28	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AH28	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AR31	Yes	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AT30	Yes	DQSn25L	DQSn26L/DQ26L	DQ26L

Pin Information for the Stratix® IV GT EP4S100G2ES1 Device
Version 1.2
Notes (1), (2), (3)
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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AG27	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	AH27	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AT32	Yes	DQS26L	DQ26L/CQn26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AU32	Yes	DQSn26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AL29	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AM29	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AU34	Yes			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AV34	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L44p	DIFFOUT_L88p	AJ29	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L44n	DIFFOUT_L88n	AK29	Yes			
		nCONFIG		nCONFIG			AW36	No			
		nSTATUS		nSTATUS			AW35	No			
		CONF_DONE		CONF_DONE			AV35	No			
		PORSEL					AP29	No			
		nCE		nCE			AN29	No			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AD25	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AE25	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AG25	Yes	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AF25	Yes	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AE24	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AK27	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AK26	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AJ26	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AH26	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AL27	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AK25	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AJ25	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AW34	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AW33	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AW32	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AV32	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AV31	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AW31	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AW30	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AV29	Yes	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AW28	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AW27	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AW29	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AV28	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AN27	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AP27	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AN26	Yes	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AM26	Yes	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AP26	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AL25	Yes	DQ5B	DQ3B	

Pin Information for the Stratix® IV GT EP4S100G2ES1 Device
Version 1.2
Notes (1), (2), (3)
WARNING: For ES1 silicon only

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AR28	Yes	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AP28	Yes	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AT29	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AU29	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AU28	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AT28	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AG24	Yes			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AH24	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AU27	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AT27	Yes			
3B	VREFB3BN0	IO				DIFFOUT_B21n	AM25	Yes	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B21p	AN25	Yes	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AP24	Yes	DQSn7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AN24	Yes	DQS7B	DQ7B/CQn7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B23n	AP25	Yes	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B23p	AR25	Yes	DQ7B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AU26	Yes	DQSn8B	DQSn7B/DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AT26	Yes	DQS8B	DQS7B/CQ7B	DQ7B/CQn7B
3B	VREFB3BN0	IO				DIFFOUT_B25n	AT25	Yes	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B25p	AU25	Yes	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AW26	Yes	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AV26	Yes	DQ8B	DQ7B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B27n	AH22	Yes	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B27p	AE23	Yes	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AG22	Yes	DQSn9B	DQ8B	DQSn7B/DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AF22	Yes	DQS9B	DQ8B/CQn8B	DQS7B/CQ7B
3B	VREFB3BN0	IO				DIFFOUT_B29n	AE22	Yes	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B29p	AF23	Yes	DQ9B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AL23	Yes	DQSn10B	DQSn8B/DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AK23	Yes	DQS10B	DQS8B/CQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AK24	Yes	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AJ22	Yes	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AJ23	Yes	DQ10B	DQ8B	DQ7B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AH23	Yes	DQ10B	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B33n	AN23	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B33p	AM23	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AN22	Yes	DQSn11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AM22	Yes	DQS11B	DQ11B/CQn11B	
3C	VREFB3CN0	IO				DIFFOUT_B35n	AL21	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B35p	AL22	Yes	DQ11B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AU24	Yes	DQSn12B	DQSn11B/DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AT24	Yes	DQS12B	DQS11B/CQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37n	AR23	Yes	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B37p	AP23	Yes	DQ12B	DQ11B	
3C	VREFB3CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AU23	Yes	DQ12B	DQ11B	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
3C	VREFB3CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AT23	Yes	DQ12B	DQ11B	
3C	VREFB3CN0	IO				DIFFOUT_B39n	AG20	Yes	DQ13B		
3C	VREFB3CN0	IO				DIFFOUT_B39p	AD21	Yes	DQ13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B40n	AF20	Yes	DQSn13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B40p	AE20	Yes	DQS13B		
3C	VREFB3CN0	IO				DIFFOUT_B41n	AE21	Yes	DQ13B		
3C	VREFB3CN0	IO				DIFFOUT_B41p	AG21	Yes	DQ13B		
3C	VREFB3CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B42n	AW25	Yes			
3C	VREFB3CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B42p	AV25	Yes			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B43n	AJ20	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B43p	AH20	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AW23	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AV23	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B45n	AP21	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B45p	AN21	No			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B23n	DIFFOUT_B46n	AU22	No			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B23p	DIFFOUT_B46p	AT22	No			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B47n	AW22	No			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B47p	AV22	No			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B24n	DIFFOUT_B48n	AT21	No			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B24p	DIFFOUT_B48p	AR22	No			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B25p	DIFFOUT_B49p	AW20	No			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B25n	DIFFOUT_B49n	AW21	No			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B50p	AV19	No			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B50n	AW19	No			
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B26p	DIFFOUT_B51p	AR20	No			
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B26n	DIFFOUT_B51n	AT20	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B52p	AN20	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B52n	AP20	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AU20	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AV20	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B54p	AH18	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B54n	AH19	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AT19	Yes			
4C	VREFB4CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AU19	Yes			
4C	VREFB4CN0	IO				DIFFOUT_B56p	AD19	Yes	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B56n	AG19	Yes	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AE19	Yes	DQS14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AF19	Yes	DQSn14B		
4C	VREFB4CN0	IO				DIFFOUT_B58p	AG18	Yes	DQ14B		
4C	VREFB4CN0	IO				DIFFOUT_B58n	AE18	Yes	DQ14B		
4C	VREFB4CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AT18	Yes	DQ15B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AU18	Yes	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60p	AT17	Yes	DQ15B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B60n	AW18	Yes	DQ15B	DQ16B	

Pin Information for the Stratix® IV GT EP4S100G2ES1 Device
Version 1.2
Notes (1), (2), (3)
WARNING: For ES1 silicon only

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
4C	VREFB4CN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AU17	Yes	DQS15B	DQS16B/CQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AV17	Yes	DQSn15B	DQSn16B/DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62p	AN19	Yes	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B62n	AM19	Yes	DQ16B	DQ16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32p	DIFFOUT_B63p	AN18	Yes	DQS16B	DQ16B/CQn16B	
4C	VREFB4CN0	IO			DIFFIO_RX_B32n	DIFFOUT_B63n	AP18	Yes	DQSn16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64p	AR19	Yes	DQ16B	DQ16B	
4C	VREFB4CN0	IO				DIFFOUT_B64n	AP19	Yes	DQ16B	DQ16B	
4B	VREFB4BN0	IO			DIFFIO_RX_B33p	DIFFOUT_B65p	AK17	Yes	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B33n	DIFFOUT_B65n	AL17	Yes	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B66p	AJ16	Yes	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B66n	AM17	Yes	DQ17B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B67p	AK16	Yes	DQS17B	DQS19B/CQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B67n	AL16	Yes	DQSn17B	DQSn19B/DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B68p	AH17	Yes	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B68n	AE17	Yes	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AF17	Yes	DQS18B	DQ19B/CQn19B	DQS20B/CQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AG17	Yes	DQSn18B	DQ19B	DQSn20B/DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B70p	AH16	Yes	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B70n	AG16	Yes	DQ18B	DQ19B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AP17	Yes	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AR17	Yes	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B72p	AN16	Yes	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B72n	AN17	Yes	DQ19B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AP16	Yes	DQS19B	DQS20B/CQ20B	DQ20B/CQn20B
4B	VREFB4BN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AR16	Yes	DQSn19B	DQSn20B/DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B74p	AW16	Yes	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B74n	AT16	Yes	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AU16	Yes	DQS20B	DQ20B/CQn20B	DQ20B
4B	VREFB4BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AV16	Yes	DQSn20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B76p	AU15	Yes	DQ20B	DQ20B	DQ20B
4B	VREFB4BN0	IO				DIFFOUT_B76n	AT15	Yes	DQ20B	DQ20B	DQ20B
4A	VREFB4AN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AN15	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AP15	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B78p	AE16	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B78n	AF16	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AV14	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AW14	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80p	AT14	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B80n	AU14	Yes	DQ21B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AV13	Yes	DQS21B	DQS24B/CQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AW13	Yes	DQSn21B	DQSn24B/DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82p	AW12	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B82n	AW11	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AU11	Yes	DQS22B	DQ24B/CQn24B	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AV11	Yes	DQSn22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84p	AT12	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO				DIFFOUT_B84n	AU12	Yes	DQ22B	DQ24B	
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AP14	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AR14	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86p	AP13	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B86n	AN14	Yes	DQ23B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AR13	Yes	DQS23B	DQS25B/CQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AT13	Yes	DQSn23B	DQSn25B/DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88p	AN13	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B88n	AL15	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AL13	Yes	DQS24B	DQ25B/CQn25B	DQS26B/CQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AM13	Yes	DQSn24B	DQ25B	DQSn26B/DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90p	AL14	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B90n	AM14	Yes	DQ24B	DQ25B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AJ13	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AK13	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92p	AH13	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B92n	AK14	Yes	DQ25B	DQ26B	DQ26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AH14	Yes	DQS25B	DQS26B/CQ26B	DQ26B/CQn26B
4A	VREFB4AN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AJ14	Yes	DQSn25B	DQSn26B/DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94p	AG14	Yes	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B94n	AG15	Yes	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B48p	DIFFOUT_B95p	AE14	Yes	DQS26B	DQ26B/CQn26B	DQ26B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B48n	DIFFOUT_B95n	AF14	Yes	DQSn26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96p	AD15	Yes	DQ26B	DQ26B	DQ26B
4A	VREFB4AN0	IO				DIFFOUT_B96n	AE15	Yes	DQ26B	DQ26B	DQ26B
		nIO_PULLUP		nIO_PULLUP			AM11	No			
		nCEO		nCEO			AT11	No			
		DCLK		DCLK			AR11	No			
		nCSO		nCSO			AP11	No			
		ASDO		ASDO			AN11	No			
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AM10	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AL10	Yes			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AW7	Yes			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AV7	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AP10	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AN10	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AW8	Yes	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AV8	Yes	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AJ11	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AH11	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AU10	Yes	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AT10	Yes	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AH12	Yes	DQ2R	DQ1R	DQ1R

Pin Information for the Stratix® IV GT EP4S100G2ES1 Device
Version 1.2
Notes (1), (2), (3)
WARNING: For ES1 silicon only

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AG12	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AW10	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AV10	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AG13	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AF13	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AU9	Yes	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AT9	Yes	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AP9	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AN9	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AU8	Yes	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AT8	Yes	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AP7	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AN7	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AR8	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AP8	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AL9	Yes	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AK9	Yes	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AU7	Yes	DQSn5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AT7	Yes	DQS5R	DQ3R/CQn3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AM8	Yes	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AL8	Yes	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AU6	Yes	DQSn6R	DQSn3R/DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AT6	Yes	DQS6R	DQS3R/CQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AJ10	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AH10	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AW4	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AV5	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AE12	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AE13	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AD12	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AD13	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AW5	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AW6	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AH8	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AH9	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AP6	Yes	DQS8R	DQ8R/CQn8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AK7	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AK8	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AM6	Yes	DQS9R	DQS8R/CQ8R	DQ8R/CQn8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15n	DIFFOUT_R29n	AE10	Yes	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	AE11	Yes	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AN6	Yes	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R31n	AF10	Yes	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	AF11	Yes	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AL6	Yes	DQS10R	DQ9R/CQn9R	DQS8R/CQ8R

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	AG10	Yes	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	AK6	Yes	DQS11R	DQS9R/CQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	AD10	Yes	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	AB10	Yes	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	AB11	Yes	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	AB12	Yes	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	AB13	Yes	DQ13R	DQ10R	
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	AC10	No			
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	AC11	No			
5C	VREFB5CN0	CLK8n	CLK8n				AC5	No			
5C	VREFB5CN0	CLK8p	CLK8p				AC6	No			
6C	VREFB6CN0	CLK10p	CLK10p				AB6	No			
6C	VREFB6CN0	CLK10n	CLK10n				AA5	No			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	W12	No			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	W11	No			
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	V12	Yes	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	V11	Yes	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	U10	Yes	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	V10	Yes	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	N9	Yes	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	P8	Yes	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	T10	Yes	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	R10	Yes	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	M6	Yes	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	N8	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	N7	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	M8	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	M7	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	K6	Yes	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	L8	Yes	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	L7	Yes	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	J6	Yes	DQS19R	DQ19R/CQn19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	K7	Yes	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	J7	Yes	DQ19R	DQ19R	DQ19R
6A	VREFB6AN0	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	G8	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R33n	DIFFOUT_R65n	F8	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	T13	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	T12	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	F7	Yes	DQS20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	E7	Yes	DQSn20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	H7	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	G7	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	R13	Yes	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	P13	Yes	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	G6	Yes	DQS21R	DQS24R/CQ24R	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	F6	Yes	DQSn21R	DQSn24R/DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	R12	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	R11	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	G9	Yes	DQS22R	DQ24R/CQn24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	F9	Yes	DQSn22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	N11	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	N10	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	F10	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	E10	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	M10	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	L10	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	D7	Yes	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	C7	Yes	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	K9	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	J9	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	D8	Yes	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	C8	Yes	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	K8	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J8	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	D9	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	C9	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	M11	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	L11	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	N12	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	M12	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D10	Yes	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	C10	Yes	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	K10	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	J10	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	D6	Yes			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	C6	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R44p	DIFFOUT_R88p	H10	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R44n	DIFFOUT_R88n	G10	Yes			
		MSEL2		MSEL2			A8	No			
		MSEL1		MSEL1			H11	No			
		MSEL0		MSEL0			J11	No			
7A	VREFB7AN0	IO				DIFFOUT_T1n	M13	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	N13	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	N14	Yes	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	P14	Yes	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	N15	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	R14	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	K13	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	L13	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	K12	Yes	DQ2T	DQ1T	DQ1T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
7A	VREFB7AN0	IO				DIFFOUT_T5p	M14	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	K14	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	L14	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	J13	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	J12	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	G13	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	H13	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	G14	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	H14	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	E13	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	F13	Yes	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	D13	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	F12	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	E14	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	F14	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	C11	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	A10	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	A11	Yes	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	B11	Yes	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	B10	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	D11	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	C14	Yes	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	D14	Yes	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	C13	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	C12	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A13	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B13	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	J15	Yes			
7A	VREFB7AN0	IO				DIFFOUT_T19p	K15	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	A14	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	B14	Yes			
7B	VREFB7BN0	IO				DIFFOUT_T21n	G15	Yes	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T21p	E16	Yes	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	F16	Yes	DQSn7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	G16	Yes	DQS7T	DQ7T/CQn7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T23n	G17	Yes	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T23p	F15	Yes	DQ7T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	C15	Yes	DQSn8T	DQSn7T/DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	D15	Yes	DQS8T	DQS7T/CQ7T	DQ7T/CQn7T
7B	VREFB7BN0	IO				DIFFOUT_T25n	A16	Yes	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T25p	D16	Yes	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	B16	Yes	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	C16	Yes	DQ8T	DQ7T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T27n	P16	Yes	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T27p	P17	Yes	DQ9T	DQ8T	DQ7T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	M16	Yes	DQSn9T	DQ8T	DQSn7T/DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	N16	Yes	DQS9T	DQ8T/CQn8T	DQS7T/CQ7T
7B	VREFB7BN0	IO				DIFFOUT_T29n	N17	Yes	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T29p	M17	Yes	DQ9T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	J16	Yes	DQSn10T	DQSn8T/DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	K16	Yes	DQS10T	DQS8T/CQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T31n	K17	Yes	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO				DIFFOUT_T31p	L16	Yes	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	H17	Yes	DQ10T	DQ8T	DQ7T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	J17	Yes	DQ10T	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T33n	C17	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T33p	F17	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	D17	Yes	DQSn11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	E17	Yes	DQS11T	DQ11T/CQn11T	
7C	VREFB7CN0	IO				DIFFOUT_T35n	C18	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T35p	D18	Yes	DQ11T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	F18	Yes	DQSn12T	DQSn11T/DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	G18	Yes	DQS12T	DQS11T/CQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37n	G20	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T37p	F20	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	F19	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	G19	Yes	DQ12T	DQ11T	
7C	VREFB7CN0	IO				DIFFOUT_T39n	R18	Yes	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T39p	J18	Yes	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	A17	Yes	DQSn13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	B17	Yes	DQS13T		
7C	VREFB7CN0	IO				DIFFOUT_T41n	H19	Yes	DQ13T		
7C	VREFB7CN0	IO				DIFFOUT_T41p	P18	Yes	DQ13T		
7C	VREFB7CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	A18	Yes			
7C	VREFB7CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	B19	Yes			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T43n	M19	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T43p	L19	No			
7C	VREFB7CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T44n	C19	No			
7C	VREFB7CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T44p	D19	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T45n	N19	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T45p	P19	No			
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T23n	DIFFOUT_T46n	C20	No			
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T23p	DIFFOUT_T46p	D20	No			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T47n	A19	No			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T47p	B20	No			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T24n	DIFFOUT_T48n	A20	No			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T24p	DIFFOUT_T48p	A21	No			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T25p	DIFFOUT_T49p	B22	No			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T25n	DIFFOUT_T49n	A22	No			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T50p	B23	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T50n	A23	No			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T26p	DIFFOUT_T51p	G21	No			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T26n	DIFFOUT_T51n	F21	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T52p	M20	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T52n	L20	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	D21	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	C22	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T54p	N20	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T54n	P20	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	A25	Yes			
8C	VREFB8CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	A24	Yes			
8C	VREFB8CN0	IO				DIFFOUT_T56p	M21	Yes	DQ14T		
8C	VREFB8CN0	IO				DIFFOUT_T56n	R20	Yes	DQ14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	D24	Yes	DQS14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	C24	Yes	DQSn14T		
8C	VREFB8CN0	IO				DIFFOUT_T58p	N21	Yes	DQ14T		
8C	VREFB8CN0	IO				DIFFOUT_T58n	M22	Yes	DQ14T		
8C	VREFB8CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	J22	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	H22	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60p	G22	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T60n	K22	Yes	DQ15T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	J23	Yes	DQS15T	DQS16T/CQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	H23	Yes	DQSn15T	DQSn16T/DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62p	E22	Yes	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T62n	D22	Yes	DQ16T	DQ16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32p	DIFFOUT_T63p	E23	Yes	DQS16T	DQ16T/CQn16T	
8C	VREFB8CN0	IO			DIFFIO_RX_T32n	DIFFOUT_T63n	D23	Yes	DQSn16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64p	G23	Yes	DQ16T	DQ16T	
8C	VREFB8CN0	IO				DIFFOUT_T64n	F23	Yes	DQ16T	DQ16T	
8B	VREFB8BN0	IO			DIFFIO_RX_T33p	DIFFOUT_T65p	K24	Yes	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T33n	DIFFOUT_T65n	J24	Yes	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T66p	M24	Yes	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T66n	J25	Yes	DQ17T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T34p	DIFFOUT_T67p	L23	Yes	DQS17T	DQS19T/CQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T34n	DIFFOUT_T67n	K23	Yes	DQSn17T	DQSn19T/DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T68p	N22	Yes	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T68n	M23	Yes	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	P23	Yes	DQS18T	DQ19T/CQn19T	DQS20T/CQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	N23	Yes	DQSn18T	DQ19T	DQSn20T/DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T70p	R22	Yes	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T70n	P22	Yes	DQ18T	DQ19T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	G24	Yes	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	F24	Yes	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T72p	G25	Yes	DQ19T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T72n	D25	Yes	DQ19T	DQ20T	DQ20T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
8B	VREFB8BN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	F25	Yes	DQS19T	DQS20T/CQ20T	DQ20T/CQn20T
8B	VREFB8BN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	E25	Yes	DQSn19T	DQSn20T/DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T74p	C25	Yes	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T74n	B25	Yes	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	C26	Yes	DQS20T	DQ20T/CQn20T	DQ20T
8B	VREFB8BN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	B26	Yes	DQSn20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T76p	A26	Yes	DQ20T	DQ20T	DQ20T
8B	VREFB8BN0	IO				DIFFOUT_T76n	D26	Yes	DQ20T	DQ20T	DQ20T
8A	VREFB8AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	G26	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	F26	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T78p	P24	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T78n	R24	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	A28	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	A27	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80p	C27	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T80n	D27	Yes	DQ21T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	C28	Yes	DQS21T	DQS24T/CQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	B28	Yes	DQSn21T	DQSn24T/DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82p	B31	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T82n	A31	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	B29	Yes	DQS22T	DQ24T/CQn24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	A29	Yes	DQSn22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84p	C29	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO				DIFFOUT_T84n	C30	Yes	DQ22T	DQ24T	
8A	VREFB8AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	F28	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	E28	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86p	D28	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T86n	F27	Yes	DQ23T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	E29	Yes	DQS23T	DQS25T/CQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	D29	Yes	DQSn23T	DQSn25T/DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88p	G27	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T88n	H26	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	H28	Yes	DQS24T	DQ25T/CQn25T	DQS26T/CQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	G28	Yes	DQSn24T	DQ25T	DQSn26T/DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90p	J26	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T90n	G29	Yes	DQ24T	DQ25T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	L26	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	K26	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92p	L25	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T92n	K28	Yes	DQ25T	DQ26T	DQ26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	K27	Yes	DQS25T	DQS26T/CQ26T	DQ26T/CQn26T
8A	VREFB8AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	J27	Yes	DQSn25T	DQSn26T/DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94p	M25	Yes	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T94n	N25	Yes	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T48p	DIFFOUT_T95p	P26	Yes	DQS26T	DQ26T/CQn26T	DQ26T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T48n	DIFFOUT_T95n	N26	Yes	DQSn26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96p	P25	Yes	DQ26T	DQ26T	DQ26T
8A	VREFB8AN0	IO				DIFFOUT_T96n	M27	Yes	DQ26T	DQ26T	DQ26T
QL2		GXB_TX_L11p					B36	No			
QL2		GXB_TX_L11n					B37	No			
QL2		GXB_RX_L11p					C38	No			
QL2		GXB_RX_L11n					C39	No			
QL2		GXB_TX_L10p					D36	No			
QL2		GXB_TX_L10n					D37	No			
QL2		GXB_RX_L10p					E38	No			
QL2		GXB_RX_L10n					E39	No			
QL2		GXB_CMUTX_L5p					F36	No			
QL2		GXB_CMUTX_L5n					F37	No			
QL2		REFCLK_L5p,GXB_CMURX_L5p					G38	No			
QL2		REFCLK_L5n,GXB_CMURX_L5n					G39	No			
QL2		GXB_CMUTX_L4p					H36	No			
QL2		GXB_CMUTX_L4n					H37	No			
QL2		REFCLK_L4p,GXB_CMURX_L4p					J38	No			
QL2		REFCLK_L4n,GXB_CMURX_L4n					J39	No			
QL2		GXB_TX_L9p					K36	No			
QL2		GXB_TX_L9n					K37	No			
QL2		GXB_RX_L9p					L38	No			
QL2		GXB_RX_L9n					L39	No			
QL2		GXB_TX_L8p					M36	No			
QL2		GXB_TX_L8n					M37	No			
QL2		GXB_RX_L8p					N38	No			
QL2		GXB_RX_L8n					N39	No			
QL1		GXB_TX_L7p					P36	No			
QL1		GXB_TX_L7n					P37	No			
QL1		GXB_RX_L7p					R38	No			
QL1		GXB_RX_L7n					R39	No			
QL1		GXB_TX_L6p					T36	No			
QL1		GXB_TX_L6n					T37	No			
QL1		GXB_RX_L6p					U38	No			
QL1		GXB_RX_L6n					U39	No			
QL1		GXB_CMUTX_L3p					V36	No			
QL1		GXB_CMUTX_L3n					V37	No			
QL1		REFCLK_L3p,GXB_CMURX_L3p					W38	No			
QL1		REFCLK_L3n,GXB_CMURX_L3n					W39	No			
QL1		GXB_CMUTX_L2p					Y36	No			
QL1		GXB_CMUTX_L2n					Y37	No			
QL1		REFCLK_L2p,GXB_CMURX_L2p					AA38	No			
QL1		REFCLK_L2n,GXB_CMURX_L2n					AA39	No			
QL1		GXB_TX_L5p					AB36	No			
QL1		GXB_TX_L5n					AB37	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
QL1		GXB_RX_L5p					AC38	No			
QL1		GXB_RX_L5n					AC39	No			
QL1		GXB_TX_L4p					AD36	No			
QL1		GXB_TX_L4n					AD37	No			
QL1		GXB_RX_L4p					AE38	No			
QL1		GXB_RX_L4n					AE39	No			
QL0		GXB_TX_L3p					AF36	No			
QL0		GXB_TX_L3n					AF37	No			
QL0		GXB_RX_L3p					AG38	No			
QL0		GXB_RX_L3n					AG39	No			
QL0		GXB_TX_L2p					AH36	No			
QL0		GXB_TX_L2n					AH37	No			
QL0		GXB_RX_L2p					AJ38	No			
QL0		GXB_RX_L2n					AJ39	No			
QL0		GXB_CMUTX_L1p					AK36	No			
QL0		GXB_CMUTX_L1n					AK37	No			
QL0		REFCLK_L1p,GXB_CMURX_L1p					AL38	No			
QL0		REFCLK_L1n,GXB_CMURX_L1n					AL39	No			
QL0		GXB_CMUTX_L0p					AM36	No			
QL0		GXB_CMUTX_L0n					AM37	No			
QL0		REFCLK_L0p,GXB_CMURX_L0p					AN38	No			
QL0		REFCLK_L0n,GXB_CMURX_L0n					AN39	No			
QL0		GXB_TX_L1p					AP36	No			
QL0		GXB_TX_L1n					AP37	No			
QL0		GXB_RX_L1p					AR38	No			
QL0		GXB_RX_L1n					AR39	No			
QL0		GXB_TX_L0p					AT36	No			
QL0		GXB_TX_L0n					AT37	No			
QL0		GXB_RX_L0p					AU38	No			
QL0		GXB_RX_L0n					AU39	No			
QR0		GXB_RX_R0n					AU1	No			
QR0		GXB_RX_R0p					AU2	No			
QR0		GXB_TX_R0n					AT3	No			
QR0		GXB_TX_R0p					AT4	No			
QR0		GXB_RX_R1n					AR1	No			
QR0		GXB_RX_R1p					AR2	No			
QR0		GXB_TX_R1n					AP3	No			
QR0		GXB_TX_R1p					AP4	No			
QR0		REFCLK_R0n,GXB_CMURX_R0n					AN1	No			
QR0		REFCLK_R0p,GXB_CMURX_R0p					AN2	No			
QR0		GXB_CMUTX_R0n					AM3	No			
QR0		GXB_CMUTX_R0p					AM4	No			
QR0		REFCLK_R1n,GXB_CMURX_R1n					AL1	No			
QR0		REFCLK_R1p,GXB_CMURX_R1p					AL2	No			
QR0		GXB_CMUTX_R1n					AK3	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
QR0		GXB_CMUTX_R1p					AK4	No			
QR0		GXB_RX_R2n					AJ1	No			
QR0		GXB_RX_R2p					AJ2	No			
QR0		GXB_TX_R2n					AH3	No			
QR0		GXB_TX_R2p					AH4	No			
QR0		GXB_RX_R3n					AG1	No			
QR0		GXB_RX_R3p					AG2	No			
QR0		GXB_TX_R3n					AF3	No			
QR0		GXB_TX_R3p					AF4	No			
QR1		GXB_RX_R4n					AE1	No			
QR1		GXB_RX_R4p					AE2	No			
QR1		GXB_TX_R4n					AD3	No			
QR1		GXB_TX_R4p					AD4	No			
QR1		GXB_RX_R5n					AC1	No			
QR1		GXB_RX_R5p					AC2	No			
QR1		GXB_TX_R5n					AB3	No			
QR1		GXB_TX_R5p					AB4	No			
QR1		REFCLK_R2n,GXB_CMURX_R2n					AA1	No			
QR1		REFCLK_R2p,GXB_CMURX_R2p					AA2	No			
QR1		GXB_CMUTX_R2n					Y3	No			
QR1		GXB_CMUTX_R2p					Y4	No			
QR1		REFCLK_R3n,GXB_CMURX_R3n					W1	No			
QR1		REFCLK_R3p,GXB_CMURX_R3p					W2	No			
QR1		GXB_CMUTX_R3n					V3	No			
QR1		GXB_CMUTX_R3p					V4	No			
QR1		GXB_RX_R6n					U1	No			
QR1		GXB_RX_R6p					U2	No			
QR1		GXB_TX_R6n					T3	No			
QR1		GXB_TX_R6p					T4	No			
QR1		GXB_RX_R7n					R1	No			
QR1		GXB_RX_R7p					R2	No			
QR1		GXB_TX_R7n					P3	No			
QR1		GXB_TX_R7p					P4	No			
QR2		GXB_RX_R8n					N1	No			
QR2		GXB_RX_R8p					N2	No			
QR2		GXB_TX_R8n					M3	No			
QR2		GXB_TX_R8p					M4	No			
QR2		GXB_RX_R9n					L1	No			
QR2		GXB_RX_R9p					L2	No			
QR2		GXB_TX_R9n					K3	No			
QR2		GXB_TX_R9p					K4	No			
QR2		REFCLK_R4n,GXB_CMURX_R4n					J1	No			
QR2		REFCLK_R4p,GXB_CMURX_R4p					J2	No			
QR2		GXB_CMUTX_R4n					H3	No			
QR2		GXB_CMUTX_R4p					H4	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
QR2		REFCLK_R5n,GXB_CMURX_R5n					G1	No			
QR2		REFCLK_R5p,GXB_CMURX_R5p					G2	No			
QR2		GXB_CMUTX_R5n					F3	No			
QR2		GXB_CMUTX_R5p					F4	No			
QR2		GXB_RX_R10n					E1	No			
QR2		GXB_RX_R10p					E2	No			
QR2		GXB_TX_R10n					D3	No			
QR2		GXB_TX_R10p					D4	No			
QR2		GXB_RX_R11n					C1	No			
QR2		GXB_RX_R11p					C2	No			
QR2		GXB_TX_R11n					B3	No			
QR2		GXB_TX_R11p					B4	No			
		GND					AL11	No			
		GND					Y21	No			
		GND					B27	No			
		GND					AV6	No			
		GND					AV9	No			
		GND					AV12	No			
		GND					AV15	No			
		GND					AV18	No			
		GND					AV21	No			
		GND					AV24	No			
		GND					AV27	No			
		GND					AV30	No			
		GND					AV33	No			
		GND					AR6	No			
		GND					AR9	No			
		GND					AR12	No			
		GND					AR15	No			
		GND					AR18	No			
		GND					AR21	No			
		GND					AR24	No			
		GND					AR27	No			
		GND					AR30	No			
		GND					AR33	No			
		GND					AM7	No			
		GND					AM9	No			
		GND					AM12	No			
		GND					AM15	No			
		GND					AM18	No			
		GND					AM21	No			
		GND					AM24	No			
		GND					AM27	No			
		GND					AM30	No			
		GND					AM33	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		GND					AJ7	No			
		GND					AJ9	No			
		GND					AJ12	No			
		GND					AJ15	No			
		GND					AJ18	No			
		GND					AJ21	No			
		GND					AJ24	No			
		GND					AJ27	No			
		GND					AJ30	No			
		GND					AJ33	No			
		GND					AF9	No			
		GND					AF12	No			
		GND					AF15	No			
		GND					AF18	No			
		GND					AF21	No			
		GND					AF24	No			
		GND					AF27	No			
		GND					AF30	No			
		GND					AD23	No			
		GND					AC7	No			
		GND					AC9	No			
		GND					AC12	No			
		GND					AC14	No			
		GND					AC16	No			
		GND					AC18	No			
		GND					AC20	No			
		GND					AC22	No			
		GND					AC24	No			
		GND					AC27	No			
		GND					AC30	No			
		GND					AC33	No			
		GND					AB15	No			
		GND					AB17	No			
		GND					AB19	No			
		GND					AB21	No			
		GND					AB23	No			
		GND					AB25	No			
		GND					AA14	No			
		GND					AA16	No			
		GND					AA18	No			
		GND					AA22	No			
		GND					AA24	No			
		GND					Y12	No			
		GND					Y15	No			
		GND					Y17	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		GND					Y19	No			
		GND					Y23	No			
		GND					Y25	No			
		GND					Y27	No			
		GND					Y30	No			
		GND					W10	No			
		GND					W14	No			
		GND					W16	No			
		GND					W18	No			
		GND					W20	No			
		GND					W22	No			
		GND					W24	No			
		GND					V15	No			
		GND					V17	No			
		GND					V19	No			
		GND					V21	No			
		GND					V23	No			
		GND					V25	No			
		GND					U9	No			
		GND					U12	No			
		GND					U14	No			
		GND					U16	No			
		GND					U18	No			
		GND					U20	No			
		GND					U22	No			
		GND					U24	No			
		GND					U26	No			
		GND					U28	No			
		GND					U30	No			
		GND					T15	No			
		GND					T17	No			
		GND					T19	No			
		GND					T21	No			
		GND					T23	No			
		GND					T25	No			
		GND					P7	No			
		GND					P9	No			
		GND					P12	No			
		GND					P15	No			
		GND					P21	No			
		GND					P27	No			
		GND					P30	No			
		GND					P33	No			
		GND					N18	No			
		GND					N24	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		GND					L6	No			
		GND					L9	No			
		GND					L12	No			
		GND					L15	No			
		GND					L18	No			
		GND					L21	No			
		GND					L24	No			
		GND					L27	No			
		GND					L30	No			
		GND					L33	No			
		GND					H6	No			
		GND					H9	No			
		GND					H12	No			
		GND					H15	No			
		GND					H18	No			
		GND					H21	No			
		GND					H24	No			
		GND					H27	No			
		GND					H30	No			
		GND					H33	No			
		GND					E6	No			
		GND					E9	No			
		GND					E12	No			
		GND					E15	No			
		GND					E18	No			
		GND					E21	No			
		GND					E24	No			
		GND					E27	No			
		GND					E30	No			
		GND					E33	No			
		GND					B9	No			
		GND					B12	No			
		GND					B15	No			
		GND					B18	No			
		GND					B21	No			
		GND					B24	No			
		GND					B30	No			
		GND					A38	No			
		GND					A37	No			
		GND					A36	No			
		GND					A35	No			
		GND					A33	No			
		GND					B39	No			
		GND					B38	No			
		GND					B35	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		GND					B34	No			
		GND					B33	No			
		GND					C37	No			
		GND					C36	No			
		GND					D39	No			
		GND					D38	No			
		GND					E37	No			
		GND					E36	No			
		GND					F39	No			
		GND					T34	No			
		GND					AW37	No			
		GND					AV37	No			
		GND					AV38	No			
		GND					AV39	No			
		GND					AU36	No			
		GND					AU37	No			
		GND					AT38	No			
		GND					AT39	No			
		GND					AR36	No			
		GND					AR37	No			
		GND					AP38	No			
		GND					AP39	No			
		GND					AN36	No			
		GND					AN37	No			
		GND					AM38	No			
		GND					AM39	No			
		GND					AL36	No			
		GND					AL37	No			
		GND					AK38	No			
		GND					AK39	No			
		GND					AJ36	No			
		GND					AJ37	No			
		GND					AH38	No			
		GND					AH39	No			
		GND					AG36	No			
		GND					AG37	No			
		GND					AF33	No			
		GND					AF38	No			
		GND					AF39	No			
		GND					AE36	No			
		GND					AE37	No			
		GND					AD32	No			
		GND					AD34	No			
		GND					AD38	No			
		GND					AD39	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		GND					AC36	No			
		GND					AC37	No			
		GND					AB33	No			
		GND					AB38	No			
		GND					AB39	No			
		GND					AA36	No			
		GND					AA37	No			
		GND					Y32	No			
		GND					Y34	No			
		GND					Y38	No			
		GND					Y39	No			
		GND					W36	No			
		GND					W37	No			
		GND					V33	No			
		GND					V38	No			
		GND					V39	No			
		GND					U36	No			
		GND					U37	No			
		GND					T32	No			
		GND					T38	No			
		GND					T39	No			
		GND					R36	No			
		GND					R37	No			
		GND					P38	No			
		GND					P39	No			
		GND					N36	No			
		GND					N37	No			
		GND					M38	No			
		GND					M39	No			
		GND					L36	No			
		GND					L37	No			
		GND					K38	No			
		GND					K39	No			
		GND					J36	No			
		GND					J37	No			
		GND					H38	No			
		GND					H39	No			
		GND					G36	No			
		GND					G37	No			
		GND					F38	No			
		GND					A7	No			
		GND					A5	No			
		GND					A4	No			
		GND					A3	No			
		GND					A2	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		GND					B7	No			
		GND					B6	No			
		GND					B5	No			
		GND					B2	No			
		GND					B1	No			
		GND					C4	No			
		GND					C3	No			
		GND					D2	No			
		GND					D1	No			
		GND					E4	No			
		GND					E3	No			
		GND					F2	No			
		GND					T8	No			
		GND					AW3	No			
		GND					AV1	No			
		GND					AV2	No			
		GND					AV3	No			
		GND					AU3	No			
		GND					AU4	No			
		GND					AT1	No			
		GND					AT2	No			
		GND					AR3	No			
		GND					AR4	No			
		GND					AP1	No			
		GND					AP2	No			
		GND					AN3	No			
		GND					AN4	No			
		GND					AM1	No			
		GND					AM2	No			
		GND					AL3	No			
		GND					AL4	No			
		GND					AK1	No			
		GND					AK2	No			
		GND					AJ3	No			
		GND					AJ4	No			
		GND					AH1	No			
		GND					AH2	No			
		GND					AG3	No			
		GND					AG4	No			
		GND					AF1	No			
		GND					AF2	No			
		GND					AF7	No			
		GND					AE3	No			
		GND					AE4	No			
		GND					AD1	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		GND					AD2	No			
		GND					AD6	No			
		GND					AD8	No			
		GND					AC3	No			
		GND					AC4	No			
		GND					AB1	No			
		GND					AB2	No			
		GND					AB7	No			
		GND					AA3	No			
		GND					AA4	No			
		GND					Y1	No			
		GND					Y2	No			
		GND					Y6	No			
		GND					Y8	No			
		GND					W3	No			
		GND					W4	No			
		GND					V1	No			
		GND					V2	No			
		GND					V7	No			
		GND					U3	No			
		GND					U4	No			
		GND					T1	No			
		GND					T2	No			
		GND					T6	No			
		GND					R3	No			
		GND					R4	No			
		GND					P1	No			
		GND					P2	No			
		GND					N3	No			
		GND					N4	No			
		GND					M1	No			
		GND					M2	No			
		GND					L3	No			
		GND					L4	No			
		GND					K1	No			
		GND					K2	No			
		GND					J3	No			
		GND					J4	No			
		GND					H1	No			
		GND					H2	No			
		GND					G3	No			
		GND					G4	No			
		GND					F1	No			
		VCC					Y20	No			
		VCC					AC15	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		VCC					AC17	No			
		VCC					AC19	No			
		VCC					AC21	No			
		VCC					AC23	No			
		VCC					AC25	No			
		VCC					AB14	No			
		VCC					AB16	No			
		VCC					AB18	No			
		VCC					AB20	No			
		VCC					AB22	No			
		VCC					AB24	No			
		VCC					AA15	No			
		VCC					AA17	No			
		VCC					AA19	No			
		VCC					AA21	No			
		VCC					AA23	No			
		VCC					AA25	No			
		VCC					Y14	No			
		VCC					Y16	No			
		VCC					Y18	No			
		VCC					Y22	No			
		VCC					Y24	No			
		VCC					W15	No			
		VCC					W17	No			
		VCC					W19	No			
		VCC					W21	No			
		VCC					W23	No			
		VCC					W25	No			
		VCC					V14	No			
		VCC					V16	No			
		VCC					V18	No			
		VCC					V20	No			
		VCC					V22	No			
		VCC					V24	No			
		VCC					V26	No			
		VCC					U15	No			
		VCC					U17	No			
		VCC					U19	No			
		VCC					U21	No			
		VCC					U23	No			
		VCC					U25	No			
		VCC					T14	No			
		VCC					T16	No			
		VCC					T18	No			
		VCC					T20	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		VCC					T22	No			
		VCC					T24	No			
		VCC					T26	No			
		VCC					AE32	No			
		VCC					AF32	No			
		VCC					AB32	No			
		VCC					AA32	No			
		VCC					V32	No			
		VCC					U32	No			
		VCC					AF8	No			
		VCC					AE8	No			
		VCC					AB8	No			
		VCC					AA8	No			
		VCC					V8	No			
		VCC					U8	No			
		VCCPT					AA27	No			
		VCCPT					AA26	No			
		VCCPT					AM20	No			
		VCCPT					AA12	No			
		VCCPT					Y13	No			
		VCCPT					H20	No			
		DNU					AA20	No			
		VCCPGM					AK28	No			
		VCCPGM					AK12	No			
		TEMPDIODEn					E11	No			
		TEMPDIODEp					A9	No			
		VCC_CLKIN3C					AK21	No			
		VCC_CLKIN4C					AK18	No			
		VCC_CLKIN7C					K18	No			
		VCC_CLKIN8C					K21	No			
		VCCBAT					K11	No			
		VCCA_PLL_B1					AL20	No			
		VCCA_PLL_B2					AL19	No			
		VCCA_PLL_L2					Y29	No			
		VCCA_PLL_L3					AA29	No			
		VCCA_PLL_R2					Y10	No			
		VCCA_PLL_R3					AA10	No			
		VCCA_PLL_T1					J20	No			
		VCCA_PLL_T2					J19	No			
		VCCD_PLL_B1					AK20	No			
		VCCD_PLL_B2					AK19	No			
		VCCD_PLL_L2					Y28	No			
		VCCD_PLL_L3					AA28	No			
		VCCD_PLL_R2					Y11	No			
		VCCD_PLL_R3					AA11	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		VCCD_PLL_T1					K20	No			
		VCCD_PLL_T2					K19	No			
		VCCIO1A					E35	No			
		VCCIO1A					J31	No			
		VCCIO1A					G32	No			
		VCCIO1A					G34	No			
		VCCIO1A					D32	No			
		VCCIO1C					K33	No			
		VCCIO1C					AA30	No			
		VCCIO1C					T29	No			
		VCCIO1C					N32	No			
		VCCIO2A					AJ28	No			
		VCCIO2A					AT35	No			
		VCCIO2A					AP31	No			
		VCCIO2A					AM32	No			
		VCCIO2A					AG26	No			
		VCCIO2C					AF31	No			
		VCCIO2C					AL33	No			
		VCCIO2C					AH31	No			
		VCCIO2C					AG33	No			
		VCCIO3A					AH25	No			
		VCCIO3A					AU30	No			
		VCCIO3A					AR29	No			
		VCCIO3A					AL26	No			
		VCCIO3B					AG23	No			
		VCCIO3B					AR26	No			
		VCCIO3C					AH21	No			
		VCCIO3C					AW24	No			
		VCCIO3C					AK22	No			
		VCCIO4A					AH15	No			
		VCCIO4A					AU13	No			
		VCCIO4A					AP12	No			
		VCCIO4A					AK15	No			
		VCCIO4B					AJ17	No			
		VCCIO4B					AW15	No			
		VCCIO4C					AJ19	No			
		VCCIO4C					AW17	No			
		VCCIO4C					AU21	No			
		VCCIO5A					AK10	No			
		VCCIO5A					AW9	No			
		VCCIO5A					AR7	No			
		VCCIO5A					AR10	No			
		VCCIO5A					AN8	No			
		VCCIO5C					AE9	No			
		VCCIO5C					AL7	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		VCCIO5C					AJ8	No			
		VCCIO5C					AH7	No			
		VCCIO6A					B8	No			
		VCCIO6A					M9	No			
		VCCIO6A					H8	No			
		VCCIO6A					E5	No			
		VCCIO6A					E8	No			
		VCCIO6C					H5	No			
		VCCIO6C					V13	No			
		VCCIO6C					T11	No			
		VCCIO6C					P10	No			
		VCCIO7A					A12	No			
		VCCIO7A					M15	No			
		VCCIO7A					J14	No			
		VCCIO7A					D12	No			
		VCCIO7B					A15	No			
		VCCIO7B					L17	No			
		VCCIO7C					C21	No			
		VCCIO7C					M18	No			
		VCCIO7C					E19	No			
		VCCIO8A					A30	No			
		VCCIO8A					M26	No			
		VCCIO8A					J28	No			
		VCCIO8A					D30	No			
		VCCIO8B					E26	No			
		VCCIO8B					K25	No			
		VCCIO8C					C23	No			
		VCCIO8C					L22	No			
		VCCIO8C					F22	No			
		VCCPD1A					U27	No			
		VCCPD1C					W27	No			
		VCCPD2A					AB26	No			
		VCCPD2C					Y26	No			
		VCCPD3A					AD24	No			
		VCCPD3B					AD22	No			
		VCCPD3C					AD20	No			
		VCCPD4A					AD14	No			
		VCCPD4B					AD16	No			
		VCCPD4C					AD18	No			
		VCCPD5A					AC13	No			
		VCCPD5C					AA13	No			
		VCCPD6A					U13	No			
		VCCPD6C					W13	No			
		VCCPD7A					R15	No			
		VCCPD7B					R17	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		VCCPD7C					R19	No			
		VCCPD8A					R25	No			
		VCCPD8B					R23	No			
		VCCPD8C					R21	No			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				P28	No			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				U29	No			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AF28	No			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				AB29	No			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AN28	No			
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AL24	No			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AP22	No			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AN12	No			
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AM16	No			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AL18	No			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AG11	No			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AD11	No			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				P11	No			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				U11	No			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G12	No			
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H16	No			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				E20	No			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				F29	No			
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				H25	No			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				J21	No			
		NC					L28	No			
		NC					AM28	No			
		NC					AK11	No			
		NC					F11	No			
		NC					AV36	No			
		NC					AU35	No			
		NC					AU5	No			
		NC					AV4	No			
		NC					AD17	No			
		NC					R16	No			
		NC					R26	No			
		NC					J34	No			
		NC					K34	No			
		NC					AJ34	No			
		NC					AH34	No			
		NC					AJ6	No			
		NC					AH6	No			
		NC					P6	No			
		NC					N6	No			
		NC					C35	No			
		NC					D35	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		NC					F35	No			
		NC					G35	No			
		NC					H35	No			
		NC					J35	No			
		NC					K35	No			
		NC					T31	No			
		NC					R33	No			
		NC					R32	No			
		NC					L35	No			
		NC					V31	No			
		NC					U31	No			
		NC					W33	No			
		NC					W32	No			
		NC					W35	No			
		NC					W34	No			
		NC					AF34	No			
		NC					AE35	No			
		NC					AG34	No			
		NC					AG35	No			
		NC					AC31	No			
		NC					AC32	No			
		NC					AB31	No			
		NC					AJ35	No			
		NC					AH35	No			
		NC					AK35	No			
		NC					AG31	No			
		NC					AG32	No			
		NC					AL35	No			
		NC					AN35	No			
		NC					AD31	No			
		NC					AM35	No			
		NC					AE31	No			
		NC					AP35	No			
		NC					AR35	No			
		NC					AT5	No			
		NC					AR5	No			
		NC					AP5	No			
		NC					AM5	No			
		NC					AN5	No			
		NC					AL5	No			
		NC					AG9	No			
		NC					AK5	No			
		NC					AD9	No			
		NC					AJ5	No			
		NC					AG7	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		NC					AG8	No			
		NC					AC8	No			
		NC					AB9	No			
		NC					AH5	No			
		NC					AG5	No			
		NC					AG6	No			
		NC					AE5	No			
		NC					AF6	No			
		NC					W6	No			
		NC					W5	No			
		NC					W8	No			
		NC					W7	No			
		NC					V6	No			
		NC					U5	No			
		NC					T9	No			
		NC					R6	No			
		NC					R5	No			
		NC					V9	No			
		NC					R7	No			
		NC					N5	No			
		NC					L5	No			
		NC					R9	No			
		NC					R8	No			
		NC					K5	No			
		NC					J5	No			
		NC					G5	No			
		NC					F5	No			
		NC					D5	No			
		NC					C5	No			
		VCCAUX					H29	No			
		VCCAUX					AL28	No			
		VCCAUX					AL12	No			
		VCCAUX					G11	No			
		VCCA_L					AF35	No			
		VCCA_L					M35	No			
		VCCA_R					AF5	No			
		VCCA_R					M5	No			
		VCCH_GXBL0					AE34	No			
		VCCH_GXBL1					AA34	No			
		VCCH_GXBL2					U34	No			
		VCCH_GXBR0					AE6	No			
		VCCH_GXBR1					AA6	No			
		VCCH_GXBR2					U6	No			
		VCCL_GXBL0					AE33	No			
		VCCL_GXBL0					AD33	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		VCCL_GXBL1					Y33	No			
		VCCL_GXBL1					AA33	No			
		VCCL_GXBL2					T33	No			
		VCCL_GXBL2					U33	No			
		VCCL_GXBR0					AD7	No			
		VCCL_GXBR0					AE7	No			
		VCCL_GXBR1					AA7	No			
		VCCL_GXBR1					Y7	No			
		VCCL_GXBR2					U7	No			
		VCCL_GXBR2					T7	No			
		VCCR_L					Y35	No			
		VCCR_L					AD35	No			
		VCCR_L					T35	No			
		VCCR_R					Y5	No			
		VCCR_R					AD5	No			
		VCCR_R					T5	No			
		VCCT_L					V35	No			
		VCCT_L					AB35	No			
		VCCT_L					P35	No			
		VCCT_R					V5	No			
		VCCT_R					AB5	No			
		VCCT_R					P5	No			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	Dynamic OCT Support	DQS for X4 for F1517	DQS for X8/X9 for F1517	DQS for X16/ X18 for F1517
		VCCHIP_L					Y31	No			
		VCCHIP_L					AA31	No			
		VCCHIP_L					W31	No			
		VCCHIP_R					Y9	No			
		VCCHIP_R					AA9	No			
		VCCHIP_R					W9	No			
		RREF_L0					AW38	No			
		RREF_L1					A34	No			
		RREF_R0					AW2	No			
		RREF_R1					A6	No			

Notes:
(1) Pins with this symbol (*) can be used as clock pins when the transceiver blocks operate below 6.5Gbps speed.
(2) Pins with this symbol (**) can only be used in configuration mode. These pins can not be used as user I/O pins after configuration.
(3) Pins with this symbol (***) can only be used as single-ended I/O.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Clock and PLL Pins
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[4:7,9, 11:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L4,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L4 and R4 respectively.
PLL_[L4,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L4 and R4 respectively.
PLL_[L1, L2, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[0:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Optional/Dual-Purpose Configuration Pins		
nCSO	I/O, Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	I/O, Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

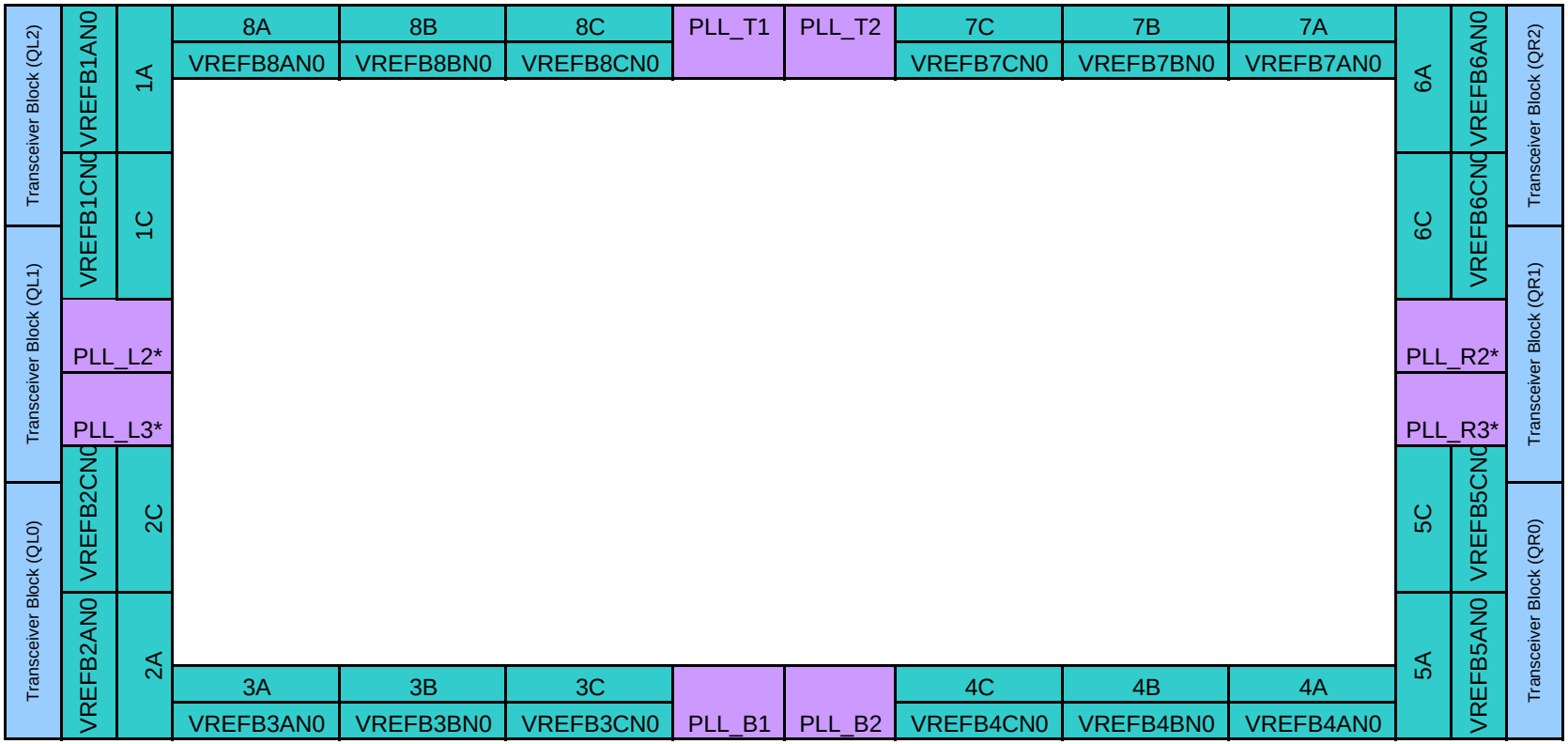
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[##][T,B], DQS[##][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B], DQSn[##][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B], DQ[##][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B], CQ[##][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[##][T,B], CQn[##][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), 3.0V PCI/PCI-X and LVTTL 3.3V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[1:8][A,C]N0, VREF[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
		Transceiver (I/O Banks) Pins
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers, specific to left (L) side and right (R) side.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p (Note 3)	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n (Note 3)	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p (Note 3)	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n (Note 3)	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
REFCLK_[L,R][0:7]p, GXB_CMURX_[L,R][0:7]p (Note 3 and 4)	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n, GXB_CMURX_[L,R][0:7]n (Note 3 and 4)	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p, (Note 4) GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

1. This pin definition is prepared based on the EP4S100G5.
2. Some of the pull-up /pull down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
Refer to the Configuring Stratix IV GX Devices chapter in the Stratix IV GX Device Handbook for more information.
3. Transceiver signals GXB_RX[15..0] and GXB_TX[15..0] are device specific.
4. Dual purpose CMU Receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th channels.
5. Refer to pin connections guidelines and data sheet for the recommended operating voltage.



Notes:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
2. PLL blocks with * only have clock pins enabled for use when the transceiver blocks operate below 6.5Gbps data rate.

Version Number	Date	Changes Made
1.0	1/23/2009	Initial release.
1.1	4/17/2009	Update device name(ES1).
1.2	2/4/2015	Added the Dynamic OCT Support column in the Pin List.