Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
		VCCD_PLL7					H25					
		VCCA_PLL7					H26					
		GNDA_PLL7					F26					
		GNDA_PLL7					G26					
B2	VREFB2N0	FPLL7CLKp	INPUT				D30					
B2	VREFB2N0	FPLL7CLKn	INPUT				D29					
B2	VREFB2N0	IO	DIFFIO_TX41p				K25					
B2	VREFB2N0	IO	DIFFIO_TX41n				K24					
B2	VREFB2N0	IO	DIFFIO_RX40p				D32					
B2	VREFB2N0	IO	DIFFIO_RX40n				D31					
B2	VREFB2N0	IO	DIFFIO_TX40p				H28					
B2	VREFB2N0	IO	DIFFIO_TX40n				H27					
B2	VREFB2N0	IO	DIFFIO_RX39p				E30					
B2	VREFB2N0	IO	DIFFIO_RX39n				E29					
B2	VREFB2N0	IO	DIFFIO_TX39p				J27					
B2	VREFB2N0	IO	DIFFIO_TX39n				J26					
B2	VREFB2N0	VREFB2N0	VREFB2N0		D20	D23	F28					
B2	VREFB2N0	IO	DIFFIO_RX38p				F30					
B2	VREFB2N0	IO	DIFFIO_RX38n				F29					
B2	VREFB2N0	IO	DIFFIO_TX38p				L24					
B2	VREFB2N0	IO	DIFFIO_TX38n				L23					
B2	VREFB2N0	IO	DIFFIO_RX37p				G30					
B2	VREFB2N0	IO	DIFFIO_RX37n				G29					
B2	VREFB2N0	IO	DIFFIO_TX37p				K27					
B2	VREFB2N0	IO	DIFFIO_TX37n				K26					
B2	VREFB2N0	IO	DIFFIO_RX36p			C26	H30					
B2	VREFB2N0	IO	DIFFIO_RX36n			C25	H29					
B2	VREFB2N0	IO	DIFFIO_TX36p			H20	M23					
B2	VREFB2N0	IO	DIFFIO_TX36n			H19	M22					
B2	VREFB2N0	IO	DIFFIO_RX35p			D25	E32					
B2	VREFB2N0	IO	DIFFIO_RX35n			D24	E31					
B2	VREFB2N0	IO	DIFFIO_TX35p			G21	L26					
B2	VREFB2N0	IO	DIFFIO_TX35n			G20	L25					
B2	VREFB2N1	IO	DIFFIO_RX34p			E24	F32					
B2	VREFB2N1	IO	DIFFIO_RX34n			E23	F31					
B2	VREFB2N1	IO	DIFFIO_TX34p			F22	M25					
B2	VREFB2N1	IO	DIFFIO_TX34n			F21	M24					
B2	VREFB2N1	IO	DIFFIO_RX33p			E26	G32					
B2	VREFB2N1	IO	DIFFIO_RX33n			E25	G31					
B2	VREFB2N1	IO	DIFFIO_TX33p			H22	N23					
B2	VREFB2N1	IO	DIFFIO_TX33n			H21	N22					
B2	VREFB2N1	IO	DIFFIO_RX32p			F24	H32					
B2	VREFB2N1	IO	DIFFIO_RX32n			F23	H31					
B2	VREFB2N1	IO	DIFFIO_TX32p			J22	M27					
B2	VREFB2N1	IO	DIFFIO_TX32n			J21	M26					
B2	VREFB2N1	VREFB2N1	VREFB2N1		F18	G22	J28					
B2	VREFB2N1	IO	DIFFIO_RX31p			F26	J32					
B2	VREFB2N1	IO	DIFFIO_RX31n			F25	J31					
B2	VREFB2N1	IO	DIFFIO_TX31p			J20	N25					
B2	VREFB2N1	IO	DIFFIO_TX31n			J19	N24					
B2	VREFB2N1	IO	DIFFIO_RX30p		C22	G24	K30					
B2	VREFB2N1	IO	DIFFIO_RX30n		C21	G23	K29					
B2	VREFB2N1	IO	DIFFIO_TX30p		E20	K22	N27					
B2	VREFB2N1	IO	DIFFIO_TX30n		E19	K21	N26					
B2	VREFB2N1	IO	DIFFIO_RX29p		D22	H24	K32					
B2	VREFB2N1	IO	DIFFIO_RX29n		D21	H23	K31					
B2	VREFB2N1	IO	DIFFIO_TX29p		F20	K20	P29					
B2	VREFB2N1	IO	DIFFIO_TX29n		F19	K19	P28					
B2	VREFB2N1	IO	DIFFIO_RX28p		E22	J24	L30					
B2	VREFB2N1	IO	DIFFIO_RX28n		E21	J23	L29					
B2	VREFB2N1	IO	DIFFIO_TX28p		G20	L23	P27					
B2	VREFB2N1	IO	DIFFIO_TX28n		G19	L22	P26					
B2	VREFB2N2	IO	DIFFIO_RX27p		F22	K24	N29					
B2	VREFB2N2	IO	DIFFIO_RX27n		F21	K23	N28					
B2	VREFB2N2	IO	DIFFIO_TX27p		G18	L21	P25					
B2	VREFB2N2	IO	DIFFIO_TX27n		G17	L20	P24					
B2	VREFB2N2	IO	DIFFIO_RX26p		H20	G26	M30					
B2	VREFB2N2	IO	DIFFIO_RX26n		H19	G25	M29					
B2	VREFB2N2	IO	DIFFIO_TX26p		H18	L19	R27					
B2	VREFB2N2	IO	DIFFIO_TX26n		H17	L18	R26					
B2	VREFB2N2	IO	DIFFIO_RX25p		G22	H26	L32					
B2	VREFB2N2	IO	DIFFIO_RX25n		G21	H25	L31					
B2	VREFB2N2	IO	DIFFIO_TX25p		J17	M24	R23					
B2	VREFB2N2	IO	DIFFIO_TX25n		J16	M23	R22					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B2	VREFB2N2	IO	DIFFIO_RX24p		H22	J26	N31					
B2	VREFB2N2	IO	DIFFIO_RX24n		H21	J25	N30					
B2	VREFB2N2	IO	DIFFIO_TX24p		J19	M22	R25					
B2	VREFB2N2	IO	DIFFIO_TX24n		J18	M21	R24					
B2	VREFB2N2	VREFB2N2	VREFB2N2		L19	N23	P30					
B2	VREFB2N2	IO	DIFFIO_RX23p		J21	L25	M32					
B2	VREFB2N2	IO	DIFFIO_RX23n		J20	L24	M31					
B2	VREFB2N2	IO	DIFFIO_TX23p		K18	N22	R29					
B2	VREFB2N2	IO	DIFFIO_TX23n		K17	N21	R28					
B2	VREFB2N2	IO	DIFFIO_RX22p		K20	K26	P32					
B2	VREFB2N2	IO	DIFFIO_RX22n		K19	K25	P31					
B2	VREFB2N2	IO	DIFFIO_TX22p		K16	N20	T28					
B2	VREFB2N2	IO	DIFFIO_TX22n		K15	N19	T27					
B2	VREFB2N2	IO	DIFFIO_RX21p		K22	M26	R31					
B2	VREFB2N2	IO	DIFFIO_RX21n		K21	M25	R30					
B2	VREFB2N2	IO	DIFFIO_TX21p		L16	M20	T23					
B2	VREFB2N2	IO	DIFFIO_TX21n		L15	M19	T22					
B2	VREFB2N2	IO	CLK0n/DIFFIO_RX_C0n		L20	P24	T31					
B2	VREFB2N2	IO	CLK0p/DIFFIO_RX_C0p		L21	P25	T32					
B2	VREFB2N2	CLK1n	INPUT		M20	N24	T29					
B2	VREFB2N2	CLK1p	INPUT		M21	N25	T30					
		VCCD_PLL1			M16	P19	U24					
		VCCA_PLL1			M17	P21	T24					
		GNDA_PLL1			L17	N18	T25					
		GNDA_PLL1			L18	P18	T26					
		GNDA_PLL2			N17	R19	U25					
		GNDA_PLL2			N18	R20	U26					
		VCCA_PLL2			M19	R21	V26					
		VCCD_PLL2			M18	P20	V25					
B1	VREFB1N0	IO	CLK2p/DIFFIO_RX_C1p		N22	R26	U32					
B1	VREFB1N0	IO	CLK2n/DIFFIO_RX_C1n		N21	R25	U31					
B1	VREFB1N0	CLK3p	INPUT		N20	P23	U30					
B1	VREFB1N0	CLK3n	INPUT		N19	P22	U29					
B1	VREFB1N0	IO	DIFFIO_RX20p		P21	T25	V31					
B1	VREFB1N0	IO	DIFFIO_RX20n		P20	T24	V30					
B1	VREFB1N0	IO	DIFFIO_TX20p		N16	R24	U23					
B1	VREFB1N0	IO	DIFFIO_TX20n		N15	R23	U22					
B1	VREFB1N0	IO	DIFFIO_RX19p		R22	U26	W32					
B1	VREFB1N0	IO	DIFFIO_RX19n		R21	U25	W31					
B1	VREFB1N0	IO	DIFFIO_TX19p		P17	U24	U28					
B1	VREFB1N0	IO	DIFFIO_TX19n		P16	U23	U27					
B1	VREFB1N0	VREFB1N0	VREFB1N0		R20	T23	W30					
B1	VREFB1N0	IO	DIFFIO_RX18p		T22	V26	AA32					
B1	VREFB1N0	IO	DIFFIO_RX18n		T21	V25	AA31					
B1	VREFB1N0	IO	DIFFIO_TX18p		P19	V24	V29					
B1	VREFB1N0	IO	DIFFIO_TX18n		P18	V23	V28					
B1	VREFB1N0	IO	DIFFIO_RX17p		U22	W26	Y31					
B1	VREFB1N0	IO	DIFFIO_RX17n		U21	W25	Y30					
B1	VREFB1N0	IO	DIFFIO_TX17p		R19	W22	V24					
B1	VREFB1N0	IO	DIFFIO_TX17n		R18	W21	V23					
B1	VREFB1N0	IO	DIFFIO_RX16p		T20	Y26	AB32					
B1	VREFB1N0	IO	DIFFIO_RX16n		T19	Y25	AB31					
B1	VREFB1N0	IO	DIFFIO_TX16p		R17	V22	W29					
B1	VREFB1N0	IO	DIFFIO_TX16n		R16	V21	W28					
B1	VREFB1N0	IO	DIFFIO_RX15p		U20	AA26	AA30					
B1	VREFB1N0	IO	DIFFIO_RX15n		U19	AA25	AA29					
B1	VREFB1N0	IO	DIFFIO_TX15p		T18	U22	W27					
B1	VREFB1N0	IO	DIFFIO_TX15n		T17	U21	W26					
B1	VREFB1N1	IO	DIFFIO_RX14p		V22	AA24	Y29					
B1	VREFB1N1	IO	DIFFIO_RX14n		V21	AA23	Y28					
B1	VREFB1N1	IO	DIFFIO_TX14p		U18	T20	W25					
B1	VREFB1N1	IO	DIFFIO_TX14n		U17	T19	W24					
B1	VREFB1N1	IO	DIFFIO_RX13p		Y22	Y24	AB30					
B1	VREFB1N1	IO	DIFFIO_RX13n		Y21	Y23	AB29					
B1	VREFB1N1	IO	DIFFIO_TX13p		V19	T22	Y27					
B1	VREFB1N1	IO	DIFFIO_TX13n		V18	T21	Y26					
B1	VREFB1N1	IO	DIFFIO_RX12p		W22	W24	AC32					
B1	VREFB1N1	IO	DIFFIO_RX12n		W21	W23	AC31					
B1	VREFB1N1	IO	DIFFIO_TX12p		W20	U20	AA27					
B1	VREFB1N1	IO	DIFFIO_TX12n		W19	U19	AA26					
B1	VREFB1N1	VREFB1N1	VREFB1N1		V20	Y22	AD28					
B1	VREFB1N1	IO	DIFFIO_RX11p			AB26	AB28					
B1	VREFB1N1	IO	DIFFIO_RX11n			AB25	AB27					
B1	VREFB1N1	IO	DIFFIO_TX11p			V20	Y25					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B1	VREFB1N1	IO	DIFFIO_TX11n			V19	Y24					
B1	VREFB1N1	IO	DIFFIO_RX10p			AB24	AD32					
B1	VREFB1N1	IO	DIFFIO_RX10n			AB23	AD31					
B1	VREFB1N1	IO	DIFFIO_TX10p			AA22	Y23					
B1	VREFB1N1	IO	DIFFIO_TX10n			AA21	Y22					
B1	VREFB1N1	IO	DIFFIO_RX9p			AC25	AE32					
B1	VREFB1N1	IO	DIFFIO_RX9n			AC24	AE31					
B1	VREFB1N1	IO	DIFFIO_TX9p			Y21	AD27					
B1	VREFB1N1	IO	DIFFIO_TX9n			Y20	AD26					
B1	VREFB1N1	IO	DIFFIO_RX8p			AD26	AF32					
B1	VREFB1N1	IO	DIFFIO_RX8n			AD25	AF31					
B1	VREFB1N1	IO	DIFFIO_TX8p			W20	AC27					
B1	VREFB1N1	IO	DIFFIO_TX8n			W19	AC26					
B1	VREFB1N2	IO	DIFFIO_RX7p				AG32					
B1	VREFB1N2	IO	DIFFIO_RX7n				AG31					
B1	VREFB1N2	IO	DIFFIO_TX7p				AA23					
B1	VREFB1N2	IO	DIFFIO_TX7n				AA22					
B1	VREFB1N2	IO	DIFFIO_RX6p				AE30					
B1	VREFB1N2	IO	DIFFIO_RX6n				AE29					
B1	VREFB1N2	IO	DIFFIO_TX6p				AA25					
B1	VREFB1N2	IO	DIFFIO_TX6n				AA24					
B1	VREFB1N2	IO	DIFFIO_RX5p				AF30					
B1	VREFB1N2	IO	DIFFIO_RX5n				AF29					
B1	VREFB1N2	IO	DIFFIO_TX5p				AB26					
B1	VREFB1N2	IO	DIFFIO_TX5n				AB25					
B1	VREFB1N2	IO	DIFFIO_RX4p				AH32					
B1	VREFB1N2	IO	DIFFIO_RX4n				AH31					
B1	VREFB1N2	IO	DIFFIO_TX4p				AC25					
B1	VREFB1N2	IO	DIFFIO_TX4n				AC24					
B1	VREFB1N2	VREFB1N2	VREFB1N2		Y20	AC23	AG28					
B1	VREFB1N2	IO	DIFFIO_RX3p				AG30					
B1	VREFB1N2	IO	DIFFIO_RX3n				AG29					
B1	VREFB1N2	IO	DIFFIO_TX3p				AB24					
B1	VREFB1N2	IO	DIFFIO_TX3n				AB23					
B1	VREFB1N2	IO	DIFFIO_RX2p				AJ32					
B1	VREFB1N2	IO	DIFFIO_RX2n				AJ31					
B1	VREFB1N2	IO	DIFFIO_TX2p				AD25					
B1	VREFB1N2	IO	DIFFIO_TX2n				AD24					
B1	VREFB1N2	IO	DIFFIO_RX1p				AH30					
B1	VREFB1N2	IO	DIFFIO_RX1n				AH29					
B1	VREFB1N2	IO	DIFFIO_TX1p				AE26					
B1	VREFB1N2	IO	DIFFIO_TX1n				AE25					
B1	VREFB1N2	FPLL8CLKn	INPUT				AJ29					
B1	VREFB1N2	FPLL8CLKp	INPUT				AJ30					
B1	VREFB1N2	IO	DIFFIO_TX0p				AE28					
B1	VREFB1N2	IO	DIFFIO_TX0n				AE27					
		GNDA_PLL8					AG26					
		GNDA_PLL8					AG27					
		VCCA_PLL8					AF26					
		VCCD_PLL8					AF25					
B8	VREFB8N0	TDI		TDI	AB21	AE25	AL31					
B8	VREFB8N0	TMS		TMS	AA20	AD24	AE24					
B8	VREFB8N0	TCK		TCK	AA19	AB22	AF24					
B8	VREFB8N0	TRST		TRST	AB19	AB21	AK30					
B8	VREFB8N0	nCONFIG		nCONFIG	W18	AA20	AL30					
B8	VREFB8N0	VCCSEL		VCCSEL	V17	Y19	AC23					
B8	VREFB8N0	IO				AC19	AE22					
B8	VREFB8N0	IO					AF22					
B8	VREFB8N0	IO		CS	T16	AC21	AC22					
B8	VREFB8N0	IO		CLKUSR	U16	AA19	AD23					
B8	VREFB8N0	IO		nWS	V16	AB20	AE23					
B8	VREFB8N0	IO		nRS	W17	AC20	AF23					
B8	VREFB8N0	IO					AD22					
B8	VREFB8N0	IO					AF21					
B8	VREFB8N0	IO	DQ17B		R15	AE24	AH28	DQ3B	DQ8B			
B8	VREFB8N0	IO	DQSn17B			AD23	AK29	DQ3B	DQ8B	DQ1B	DQ3B	DQ1B
B8	VREFB8N0	VREFB8N0	VREFB8N0		Y19	AC22	AK31					
B8	VREFB8N0	IO	DQ17B		T15	AF24	AJ28	DQ3B	DQ8B	DQ1B	DQ3B	
B8	VREFB8N0	IO	DQ17B			AE22	AM29	DQ3B	DQ8B	DQ1B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQ17B		Y14	AD22	AL29	DQ3B	DQ8B	DQ1B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQS17B			AE23	AK28	DQVLD3B	DQVLD8B			
B8	VREFB8N0	IO			R14	V18	AG20					
B8	VREFB8N0	IO					AE21					
B8	VREFB8N0	IO	DQ16B			AB19	AK27		DQ8B		DQ3B	DQ1B

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B8	VREFB8N0	IO	DQSn16B				AL28		DQSn8B		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ16B		T14	W18	AJ27		DQ8B		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ16B				AM28		DQ8B		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ16B			AC18	AM27		DQ8B		DQ3B	DQ1B
B8	VREFB8N0	IO	DQS16B				AL27		DQS8B		DQVLD3B	
B8	VREFB8N0	IO					AB21					
B8	VREFB8N0	IO			U15	Y18	AD21					
B8	VREFB8N0	IO	DQ15B			AF22	AK26	DQ3B	DQ7B	DQ1B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQSn15B		W14	AE21	AL26	DQSn3B	DQ7B	DQ1B	DQSn3B	DQ1B
B8	VREFB8N1	IO	DQ15B			AD21	AJ26	DQ3B	DQ7B	DQ1B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ15B		U14	AD20	AM25	DQ3B	DQ7B	DQ1B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ15B			AF21	AM26	DQ3B	DQ7B	DQ1B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQS15B		W15	AE20	AL25	DQS3B	DQVLD7B	DQVLD1B	DQS3B	
B8	VREFB8N1	IO					AC21					
B8	VREFB8N1	IO					AF20					
B8	VREFB8N1	IO	DQ14B			AB18	AG24		DQ7B		DQ3B	DQ1B
B8	VREFB8N1	IO	DQSn14B				AH25		DQSn7B		DQ3B	DQ1B
B8	VREFB8N1	IO	DQ14B		T13	V17	AH26		DQ7B		DQ3B	DQ1B
B8	VREFB8N1	IO	DQ14B				AH24		DQ7B		DQ3B	DQ1B
B8	VREFB8N1	IO	DQ14B			AC17	AK25		DQ7B		DQ3B	DQ1B
B8	VREFB8N1	IO	DQS14B				AJ25		DQS7B			
B8	VREFB8N1	IO			U13	W17	AB20					
B8	VREFB8N1	IO					AE20					
B8	VREFB8N1	IO	DQ13B		Y18	AF20	AM24	DQ2B	DQ6B	DQ1B		
B8	VREFB8N1	IO	DQSn13B		AA18	AE19	AL24	DQ2B	DQ6B	DQSn1B	DQ2B	DQSn1B
B8	VREFB8N1	VREFB8N1	VREFB8N1		W16	AA18	AJ24					
B8	VREFB8N1	IO	DQ13B		Y17	AD19	AK24	DQ2B	DQ6B	DQ1B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ13B		AB18	AD18	AK23	DQ2B	DQ6B	DQ1B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ13B		AB17	AF19	AM23	DQ2B	DQ6B	DQ1B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQS13B		AA17	AE18	AL23	DQVLD2B	DQVLD6B	DQS1B		DQS1B
B8	VREFB8N1	IO					AD20					
B8	VREFB8N1	IO				Y17	AC20					
B8	VREFB8N1	IO	DQ12B		V15	AB17	AG23		DQ6B		DQ2B	DQ1B
B8	VREFB8N1	IO	DQSn12B				AH22		DQSn6B		DQ2B	DQ1B
B8	VREFB8N1	IO	DQ12B			V16	AG22		DQ6B		DQ2B	DQ1B
B8	VREFB8N1	IO	DQ12B				AK22		DQ6B		DQ2B	DQ1B
B8	VREFB8N1	IO	DQ12B		U12	AA17	AJ23		DQ6B		DQ2B	DQ1B
B8	VREFB8N1	IO	DQS12B				AJ22		DQS6B		DQVLD2B	DQVLD1B
B8	VREFB8N1	IO					AB19					
B8	VREFB8N1	IO				W16	AF19					
B8	VREFB8N1	IO	DQ11B		AB16	AF18	AM22	DQ2B	DQ5B	DQ1B	DQ2B	DQ1B
B8	VREFB8N1	IO	DQSn11B		AA16	AE17	AL22	DQSn2B	DQ5B	DQ1B	DQSn2B	DQ1B
B8	VREFB8N2	IO	DQ11B		Y16	AD17	AJ21	DQ2B	DQ5B	DQ1B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ11B		Y15	AF17	AK21	DQ2B	DQ5B	DQ1B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ11B		AB15	AD16	AM21	DQ2B	DQ5B	DQ1B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQS11B		AA15	AE16	AL21	DQS2B	DQVLD5B		DQS2B	
B8	VREFB8N2	IO					AB18					
B8	VREFB8N2	IO					AC19					
B8	VREFB8N2	IO	DQ10B		V13	AA16	AH20		DQ5B		DQ2B	DQ1B
B8	VREFB8N2	IO	DQSn10B				AJ20		DQSn5B		DQ2B	DQ1B
B8	VREFB8N2	IO	DQ10B			V14	AJ19		DQ5B		DQ2B	DQ1B
B8	VREFB8N2	IO	DQ10B				AH19		DQ5B		DQ2B	DQ1B
B8	VREFB8N2	IO	DQ10B		V14	W15	AL20		DQ5B		DQ2B	DQ1B
B8	VREFB8N2	IO	DQS10B				AK20		DQS5B			
B8	VREFB8N2	VREFB8N2	VREFB8N2		AA14	AC16	AK19					
B8	VREFB8N2	IO					AB17					
B8	VREFB8N2	IO				Y16	AC18					
B8	VREFB8N2	IO					AD19					
B8	VREFB8N2	IO					AE19					
B8	VREFB8N2	IO		RUnLU	V11	Y15	AG17					
B8	VREFB8N2	IO		DEV_OE	V12	AA14	AH17					
B8	VREFB8N2	IO		DEV_CLRn	W11	AA15	AG19					
B8	VREFB8N2	IO		nCS	W12	AB15	AG18					
B12	VREFB8N2	IO	PLL12_FBn/OUT2n		W13	AC15	AL19					
B12	VREFB8N2	IO	PLL12_FBp/OUT2p				AM19					
B8	VREFB8N2	IO					AC17					
B8	VREFB8N2	IO				AB16	AD18					
B12	VREFB8N2	IO	PLL12_OUT1n				AH18					
B12	VREFB8N2	IO	PLL12_OUT1p				AJ18					
B12	VREFB8N2	IO	PLL12_OUT0n				AK18					
B12	VREFB8N2	IO	PLL12_OUT0p		Y13	AD15	AL18					
B8	VREFB8N2	IO	CLK5n		Y12	AB14	AJ17					
B8	VREFB8N2	IO	CLK5p		AA12	AC14	AK17					
B8	VREFB8N2	IO	CLK4n		AA13	AE15	AL17					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B8	VREFB8N2	IO	CLK4p		AB13	AF15	AM17					
B12		VCC_PLL12_OUT					AF16					
		VCCD_PLL12					AE18					
		VCCA_PLL12					AF18					
		GNDA_PLL12					AD17					
		GNDA_PLL12					AE17					
		GNDA_PLL6			T11	W13	AD16					
		GNDA_PLL6			T12	W14	AE16					
		VCCA_PLL6			R12	Y13	AE15					
		VCCD_PLL6			U11	Y14	AD15					
B10		VCC_PLL6_OUT			R11	V13	AF15					
B7	VREFB7N0	IO	CLK7p		Y10	AC13	AH16					
B7	VREFB7N0	IO	CLK7n		W10	AB13	AG16					
B7	VREFB7N0	IO	CLK6p		AA11	AE14	AM16					
B7	VREFB7N0	IO	CLK6n		Y11	AD14	AL16					
B10	VREFB7N0	IO	PLL6_OUT1p		AA9	AE13	AJ15					
B10	VREFB7N0	IO	PLL6_OUT1n		Y9	AD13	AH15					
B10	VREFB7N0	IO	PLL6_OUT0p		AB10	AF12	AK16					
B10	VREFB7N0	IO	PLL6_OUT0n		AA10	AE12	AJ16					
B10	VREFB7N0	IO	PLL6_FBp/OUT2p		W9	AD12	AL15					
B10	VREFB7N0	IO	PLL6_FBn/OUT2n		V9	AC12	AK15					
B7	VREFB7N0	IO					AB16					
B7	VREFB7N0	IO					AC16					
B7	VREFB7N0	IO					AB15					
B7	VREFB7N0	IO					AC15					
B7	VREFB7N0	IO	DQ9B		AB8	AE11	AM14	DQ1B	DQ4B			
B7	VREFB7N0	IO	DQSn9B		AA8	AE10	AL13	DQ1B	DQ4B	DQ0B	DQ1B	DQ0B
B7	VREFB7N0	VREFB7N0	VREFB7N0		W8	AC11	AK14					
B7	VREFB7N0	IO	DQ9B		Y7	AC10	AJ13	DQ1B	DQ4B	DQ0B	DQ1B	
B7	VREFB7N0	IO	DQ9B		Y8	AF10	AJ14	DQ1B	DQ4B	DQ0B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQ9B		AB7	AD11	AL14	DQ1B	DQ4B	DQ0B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQS9B		AA7	AD10	AK13	DQVLD1B	DQVLD4B			
B7	VREFB7N0	IO					AD14					
B7	VREFB7N0	IO					AC14					
B7	VREFB7N0	IO	DQ8B			Y12	AG15		DQ4B		DQ1B	DQ0B
B7	VREFB7N0	IO	DQSn8B				AH14		DQSn4B		DQ1B	DQ0B
B7	VREFB7N0	IO	DQ8B		U10	W12	AF13		DQ4B		DQ1B	DQ0B
B7	VREFB7N0	IO	DQ8B			Y11	AG13		DQ4B		DQ1B	DQ0B
B7	VREFB7N0	IO	DQ8B				AH13		DQ4B		DQ1B	DQ0B
B7	VREFB7N0	IO	DQS8B		V10	AA12	AG14		DQS4B		DQVLD1B	
B7	VREFB7N0	IO					AB14					
B7	VREFB7N0	IO					AE14					
B7	VREFB7N0	IO	DQ7B		AB6	AF9	AM12	DQ1B	DQ3B	DQ0B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQSn7B		AA6	AE9	AL12	DQSn1B	DQ3B	DQ0B	DQSn1B	DQ0B
B7	VREFB7N1	IO	DQ7B		Y6	AD8	AM11	DQ1B	DQ3B	DQ0B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ7B		Y5	AC8	AJ12	DQ1B	DQ3B	DQ0B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ7B		AB5	AC9	AK12	DQ1B	DQ3B	DQ0B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQS7B		AA5	AD9	AL11	DQS1B	DQVLD3B	DQVLD0B	DQS1B	
B7	VREFB7N1	IO					AB13					
B7	VREFB7N1	IO					AD13					
B7	VREFB7N1	IO	DQ6B			V12	AM10		DQ3B		DQ1B	DQ0B
B7	VREFB7N1	IO	DQSn6B			AA11	AK11		DQSn3B		DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B				AL10		DQ3B		DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B		T10	W11	AH11		DQ3B		DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B				AJ11		DQ3B		DQ1B	DQ0B
B7	VREFB7N1	IO	DQS6B			AB12	AK10		DQS3B			
B7	VREFB7N1	IO					AC13					
B7	VREFB7N1	IO					AE13					
B7	VREFB7N1	IO	DQ5B		U9	AF8	AG12	DQ0B	DQ2B	DQ0B		
B7	VREFB7N1	IO	DQSn5B			AE8	AG11	DQ0B	DQ2B	DQSn0B	DQ0B	DQSn0B
B7	VREFB7N1	VREFB7N1	VREFB7N1		W6	AA9	AJ9					
B7	VREFB7N1	IO	DQ5B		T9	AC7	AF10	DQ0B	DQ2B	DQ0B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ5B			AD7	AG10	DQ0B	DQ2B	DQ0B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ5B			AF7	AF12	DQ0B	DQ2B	DQ0B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQS5B		V8	AE7	AF11	DQVLD0B	DQVLD2B	DQS0B		DQS0B
B7	VREFB7N1	IO					AB12					
B7	VREFB7N1	IO				Y10	AE12					
B7	VREFB7N1	IO	DQ4B				AM9		DQ2B		DQ0B	DQ0B
B7	VREFB7N1	IO	DQSn4B		W7	AB11	AL9		DQSn2B		DQ0B	DQ0B
B7	VREFB7N1	IO	DQ4B				AJ8		DQ2B		DQ0B	DQ0B
B7	VREFB7N1	IO	DQ4B			Y9	AK8		DQ2B		DQ0B	DQ0B
B7	VREFB7N1	IO	DQ4B			AA10	AJ10		DQ2B		DQ0B	DQ0B
B7	VREFB7N1	IO	DQS4B				AK9		DQS2B		DQVLD0B	DQVLD0B
B7	VREFB7N1	IO					AC12					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B7	VREFB7N1	IO					AD12					
B7	VREFB7N1	IO	DQ3B		U8	AF6	AM8	DQ0B	DQ1B	DQ0B	DQ0B	DQ0B
B7	VREFB7N1	IO	DQSn3B			AE6	AL8	DQSn0B	DQ1B	DQ0B	DQSn0B	DQ0B
B7	VREFB7N2	IO	DQ3B		T8	AC6	AJ7	DQ0B	DQ1B	DQ0B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ3B			AE5	AK7	DQ0B	DQ1B	DQ0B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ3B		V7	AF5	AM7	DQ0B	DQ1B	DQ0B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQS3B			AD6	AL7	DQS0B	DQVLD1B		DQS0B	
B7	VREFB7N2	IO					AD11					
B7	VREFB7N2	IO					AE11					
B7	VREFB7N2	IO	DQ2B			AB10	AM6		DQ1B		DQ0B	DQ0B
B7	VREFB7N2	IO	DQSn2B				AL6		DQSn1B		DQ0B	DQ0B
B7	VREFB7N2	IO	DQ2B		U7	W10	AJ6		DQ1B		DQ0B	DQ0B
B7	VREFB7N2	IO	DQ2B			W9	AK6		DQ1B		DQ0B	DQ0B
B7	VREFB7N2	IO	DQ2B				AM5		DQ1B		DQ0B	DQ0B
B7	VREFB7N2	IO	DQS2B		R9	AB9	AL5		DQS1B			
B7	VREFB7N2	IO					AB11					
B7	VREFB7N2	IO					AC11					
B7	VREFB7N2	IO	DQ1B			AD5	AH9		DQ0B			
B7	VREFB7N2	IO	DQSn1B		V6	AE4	AH8		DQ0B			
B7	VREFB7N2	VREFB7N2	VREFB7N2		AA4	AC5	AK2					
B7	VREFB7N2	IO	DQ1B			AD3	AH7		DQ0B			
B7	VREFB7N2	IO	DQ1B			AD4	AH6		DQ0B			
B7	VREFB7N2	IO	DQ1B		T7	AF3	AG9		DQ0B			
B7	VREFB7N2	IO	DQS1B			AE3	AG8		DQVLD0B			
B7	VREFB7N2	IO					AD10					
B7	VREFB7N2	IO					AE10					
B7	VREFB7N2	IO	DQ0B		U6	AA8	AM4		DQ0B			
B7	VREFB7N2	IO	DQSn0B			AB8	AK5		DQSn0B			
B7	VREFB7N2	IO	DQ0B				AH5		DQ0B			
B7	VREFB7N2	IO	DQ0B			V10	AJ5		DQ0B			
B7	VREFB7N2	IO	DQ0B		W5	AB7	AL4		DQ0B			
B7	VREFB7N2	IO	DQS0B				AK4		DQS0B			
B7	VREFB7N2	PORSEL		PORSEL	V5	Y8	AL2					
B7	VREFB7N2	nIO_PULLUP		nIO_PULLUP	AB2	AE2	AK3					
B7	VREFB7N2	PLL_ENA		PLL_ENA	Y4	AB6	AF8					
		GND			AB4	AA7	AF9					
B7	VREFB7N2	nCEO		nCEO	AA3	AB5	AL3					
		VCCD_PLL9					AE8					
		VCCA_PLL9					AE7					
		GNDA_PLL9					AF7					
		GNDA_PLL9					AG7					
B6	VREFB6N0	IO	DIFFIO_TX83n				AD9					
B6	VREFB6N0	IO	DIFFIO_TX83p				AD8					
B6	VREFB6N0	FPLL9CLKp	INPUT				AJ3					
B6	VREFB6N0	FPLL9CLKn	INPUT				AJ4					
B6	VREFB6N0	IO	DIFFIO_TX82n				AC9					
B6	VREFB6N0	IO	DIFFIO_TX82p				AC8					
B6	VREFB6N0	IO	DIFFIO_RX82n				AJ2					
B6	VREFB6N0	IO	DIFFIO_RX82p				AJ1					
B6	VREFB6N0	IO	DIFFIO_TX81n				AB10					
B6	VREFB6N0	IO	DIFFIO_TX81p				AB9					
B6	VREFB6N0	IO	DIFFIO_RX81n				AH4					
B6	VREFB6N0	IO	DIFFIO_RX81p				AH3					
B6	VREFB6N0	IO	DIFFIO_TX80n				AB8					
B6	VREFB6N0	IO	DIFFIO_TX80p				AB7					
B6	VREFB6N0	IO	DIFFIO_RX80n				AH2					
B6	VREFB6N0	IO	DIFFIO_RX80p				AH1					
B6	VREFB6N0	VREFB6N0	VREFB6N0		Y3	AC4	AG5					
B6	VREFB6N0	IO	DIFFIO_TX79n				AC7					
B6	VREFB6N0	IO	DIFFIO_TX79p				AC6					
B6	VREFB6N0	IO	DIFFIO_RX79n				AG4					
B6	VREFB6N0	IO	DIFFIO_RX79p				AG3					
B6	VREFB6N0	IO	DIFFIO_TX78n				AA9					
B6	VREFB6N0	IO	DIFFIO_TX78p				AA8					
B6	VREFB6N0	IO	DIFFIO_RX78n				AG2					
B6	VREFB6N0	IO	DIFFIO_RX78p				AG1					
B6	VREFB6N0	IO	DIFFIO_TX77n				AD7					
B6	VREFB6N0	IO	DIFFIO_TX77p				AD6					
B6	VREFB6N0	IO	DIFFIO_RX77n				AF4					
B6	VREFB6N0	IO	DIFFIO_RX77p				AF3					
B6	VREFB6N0	IO	DIFFIO_TX76n				AA7					
B6	VREFB6N0	IO	DIFFIO_TX76p				AA6					
B6	VREFB6N0	IO	DIFFIO_RX76n				AF2					
B6	VREFB6N0	IO	DIFFIO_RX76p				AF1					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B6	VREFB6N1	IO	DIFFIO_TX75n			Y7	AA11					
B6	VREFB6N1	IO	DIFFIO_TX75p			Y6	AA10					
B6	VREFB6N1	IO	DIFFIO_RX75n			AD2	AE4					
B6	VREFB6N1	IO	DIFFIO_RX75p			AD1	AE3					
B6	VREFB6N1	IO	DIFFIO_TX74n			AA6	AB6					
B6	VREFB6N1	IO	DIFFIO_TX74p			AA5	AB5					
B6	VREFB6N1	IO	DIFFIO_RX74n			AC3	AE2					
B6	VREFB6N1	IO	DIFFIO_RX74p			AC2	AE1					
B6	VREFB6N1	IO	DIFFIO_TX73n			W8	Y11					
B6	VREFB6N1	IO	DIFFIO_TX73p			W7	Y10					
B6	VREFB6N1	IO	DIFFIO_RX73n			AB4	AD2					
B6	VREFB6N1	IO	DIFFIO_RX73p			AB3	AD1					
B6	VREFB6N1	IO	DIFFIO_TX72n			W6	Y9					
B6	VREFB6N1	IO	DIFFIO_TX72p			W5	Y8					
B6	VREFB6N1	IO	DIFFIO_RX72n			AA4	AC4					
B6	VREFB6N1	IO	DIFFIO_RX72p			AA3	AC3					
B6	VREFB6N1	VREFB6N1	VREFB6N1		U3	Y5	AD5					
B6	VREFB6N1	IO	DIFFIO_TX71n		W4	V8	Y7					
B6	VREFB6N1	IO	DIFFIO_TX71p		W3	V7	Y6					
B6	VREFB6N1	IO	DIFFIO_RX71n		W2	Y4	AC2					
B6	VREFB6N1	IO	DIFFIO_RX71p		W1	Y3	AC1					
B6	VREFB6N1	IO	DIFFIO_TX70n		V4	V6	W5					
B6	VREFB6N1	IO	DIFFIO_TX70p		V3	V5	W4					
B6	VREFB6N1	IO	DIFFIO_RX70n		Y2	W4	AB4					
B6	VREFB6N1	IO	DIFFIO_RX70p		Y1	W3	AB3					
B6	VREFB6N1	IO	DIFFIO_TX69n		U5	U8	W7					
B6	VREFB6N1	IO	DIFFIO_TX69p		U4	U7	W6					
B6	VREFB6N1	IO	DIFFIO_RX69n		V2	AB2	AB2					
B6	VREFB6N1	IO	DIFFIO_RX69p		V1	AB1	AB1					
B6	VREFB6N2	IO	DIFFIO_TX68n		T6	T7	W9					
B6	VREFB6N2	IO	DIFFIO_TX68p		T5	T6	W8					
B6	VREFB6N2	IO	DIFFIO_RX68n		T4	AA2	Y5					
B6	VREFB6N2	IO	DIFFIO_RX68p		T3	AA1	Y4					
B6	VREFB6N2	IO	DIFFIO_TX67n		R8	U6	V5					
B6	VREFB6N2	IO	DIFFIO_TX67p		R7	U5	V4					
B6	VREFB6N2	IO	DIFFIO_RX67n		U2	Y2	AA4					
B6	VREFB6N2	IO	DIFFIO_RX67p		U1	Y1	AA3					
B6	VREFB6N2	IO	DIFFIO_TX66n		R6	V4	V7					
B6	VREFB6N2	IO	DIFFIO_TX66p		R5	V3	V6					
B6	VREFB6N2	IO	DIFFIO_RX66n		R4	W2	AA2					
B6	VREFB6N2	IO	DIFFIO_RX66p		R3	W1	AA1					
B6	VREFB6N2	IO	DIFFIO_TX65n		P6	T9	V10					
B6	VREFB6N2	IO	DIFFIO_TX65p		P5	T8	V9					
B6	VREFB6N2	IO	DIFFIO_RX65n		T2	V2	Y3					
B6	VREFB6N2	IO	DIFFIO_RX65p		T1	V1	Y2					
B6	VREFB6N2	VREFB6N2	VREFB6N2		P4	R5	W3					
B6	VREFB6N2	IO	DIFFIO_TX64n		P8	U4	U11					
B6	VREFB6N2	IO	DIFFIO_TX64p		P7	U3	U10					
B6	VREFB6N2	IO	DIFFIO_RX64n		R2	U2	W2					
B6	VREFB6N2	IO	DIFFIO_RX64p		R1	U1	W1					
B6	VREFB6N2	IO	DIFFIO_TX63n		N8	T5	U6					
B6	VREFB6N2	IO	DIFFIO_TX63p		N7	T4	U5					
B6	VREFB6N2	IO	DIFFIO_RX63n		P3	T3	V3					
B6	VREFB6N2	IO	DIFFIO_RX63p		P2	T2	V2					
B6	VREFB6N2	CLK9n	INPUT		N4	R4	U4					
B6	VREFB6N2	CLK9p	INPUT		N3	R3	U3					
B6	VREFB6N2	IO	CLK8n/DIFFIO_RX_C2n		N2	R2	U2					
B6	VREFB6N2	IO	CLK8p/DIFFIO_RX_C2p		N1	R1	U1					
		VCCD_PLL3			M5	P7	U7					
		VCCA_PLL3			M4	R6	U9					
		GNDA_PLL3			N5	R7	U8					
		GNDA_PLL3			N6	R8	V8					
		GNDA_PLL4			L4	N8	R8					
		GNDA_PLL4			L5	N9	T8					
		VCCA_PLL4			M6	P8	R9					
		VCCD_PLL4			L6	P9	T9					
B5	VREFB5N0	CLK11p	INPUT		M2	N2	T3					
B5	VREFB5N0	CLK11n	INPUT		M3	N3	T4					
B5	VREFB5N0	IO	CLK10p/DIFFIO_RX_C3p		L2	P2	T1					
B5	VREFB5N0	IO	CLK10n/DIFFIO_RX_C3n		L3	P3	T2					
B5	VREFB5N0	IO	DIFFIO_TX62n		L8	N7	T11					
B5	VREFB5N0	IO	DIFFIO_TX62p		L7	N6	T10					
B5	VREFB5N0	IO	DIFFIO_RX62n		K2	M2	P2					
B5	VREFB5N0	IO	DIFFIO_RX62p		K1	M1	P1					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B5	VREFB5N0	IO	DIFFIO_TX61n		K8	P5	T6					
B5	VREFB5N0	IO	DIFFIO_TX61p		K7	P4	T5					
B5	VREFB5N0	IO	DIFFIO_RX61n		K4	L3	R3					
B5	VREFB5N0	IO	DIFFIO_RX61p		K3	L2	R2					
B5	VREFB5N0	IO	DIFFIO_TX60n		K6	N5	R11					
B5	VREFB5N0	IO	DIFFIO_TX60p		K5	N4	R10					
B5	VREFB5N0	IO	DIFFIO_RX60n		J3	K2	M2					
B5	VREFB5N0	IO	DIFFIO_RX60p		J2	K1	M1					
B5	VREFB5N0	VREFB5N0	VREFB5N0		J4	K5	P3					
B5	VREFB5N0	IO	DIFFIO_TX59n		J6	M6	R5					
B5	VREFB5N0	IO	DIFFIO_TX59p		J5	M5	R4					
B5	VREFB5N0	IO	DIFFIO_RX59n		H2	J2	N3					
B5	VREFB5N0	IO	DIFFIO_RX59p		H1	J1	N2					
B5	VREFB5N0	IO	DIFFIO_TX58n		J8	M8	R7					
B5	VREFB5N0	IO	DIFFIO_TX58p		J7	M7	R6					
B5	VREFB5N0	IO	DIFFIO_RX58n		G2	K4	L2					
B5	VREFB5N0	IO	DIFFIO_RX58p		G1	K3	L1					
B5	VREFB5N0	IO	DIFFIO_TX57n		H6	L9	P11					
B5	VREFB5N0	IO	DIFFIO_TX57p		H5	L8	P10					
B5	VREFB5N0	IO	DIFFIO_RX57n		H4	H2	M4					
B5	VREFB5N0	IO	DIFFIO_RX57p		H3	H1	M3					
B5	VREFB5N0	IO	DIFFIO_TX56n		G6	L7	P5					
B5	VREFB5N0	IO	DIFFIO_TX56p		G5	L6	P4					
B5	VREFB5N0	IO	DIFFIO_RX56n		F2	G2	N5					
B5	VREFB5N0	IO	DIFFIO_RX56p		F1	G1	N4					
B5	VREFB5N1	IO	DIFFIO_TX55n		G4	M4	P7					
B5	VREFB5N1	IO	DIFFIO_TX55p		G3	M3	P6					
B5	VREFB5N1	IO	DIFFIO_RX55n		E2	J4	L4					
B5	VREFB5N1	IO	DIFFIO_RX55p		E1	J3	L3					
B5	VREFB5N1	IO	DIFFIO_TX54n		F5	L5	P9					
B5	VREFB5N1	IO	DIFFIO_TX54p		F4	L4	P8					
B5	VREFB5N1	IO	DIFFIO_RX54n		D2	H4	K2					
B5	VREFB5N1	IO	DIFFIO_RX54p		D1	H3	K1					
B5	VREFB5N1	IO	DIFFIO_TX53n		E4	K9	N9					
B5	VREFB5N1	IO	DIFFIO_TX53p		E3	K8	N8					
B5	VREFB5N1	IO	DIFFIO_RX53n		C2	G4	K4					
B5	VREFB5N1	IO	DIFFIO_RX53p		C1	G3	K3					
B5	VREFB5N1	IO	DIFFIO_TX52n			K7	N7					
B5	VREFB5N1	IO	DIFFIO_TX52p			K6	N6					
B5	VREFB5N1	IO	DIFFIO_RX52n			F4	J2					
B5	VREFB5N1	IO	DIFFIO_RX52p			F3	J1					
B5	VREFB5N1	VREFB5N1	VREFB5N1		F3	G5	J5					
B5	VREFB5N1	IO	DIFFIO_TX51n			J8	M7					
B5	VREFB5N1	IO	DIFFIO_TX51p			J7	M6					
B5	VREFB5N1	IO	DIFFIO_RX51n			F2	H2					
B5	VREFB5N1	IO	DIFFIO_RX51p			F1	H1					
B5	VREFB5N1	IO	DIFFIO_TX50n			H8	M9					
B5	VREFB5N1	IO	DIFFIO_TX50p			H7	M8					
B5	VREFB5N1	IO	DIFFIO_RX50n			E4	J4					
B5	VREFB5N1	IO	DIFFIO_RX50p			E3	J3					
B5	VREFB5N1	IO	DIFFIO_TX49n			J6	M11					
B5	VREFB5N1	IO	DIFFIO_TX49p			J5	M10					
B5	VREFB5N1	IO	DIFFIO_RX49n			E2	G2					
B5	VREFB5N1	IO	DIFFIO_RX49p			E1	G1					
B5	VREFB5N2	IO	DIFFIO_TX48n			H6	L6					
B5	VREFB5N2	IO	DIFFIO_TX48p			H5	L5					
B5	VREFB5N2	IO	DIFFIO_RX48n			D3	G4					
B5	VREFB5N2	IO	DIFFIO_RX48p			D2	G3					
B5	VREFB5N2	IO	DIFFIO_TX47n			G7	K7					
B5	VREFB5N2	IO	DIFFIO_TX47p			G6	K6					
B5	VREFB5N2	IO	DIFFIO_RX47n			C2	F2					
B5	VREFB5N2	IO	DIFFIO_RX47p			C1	F1					
B5	VREFB5N2	IO	DIFFIO_TX46n				L8					
B5	VREFB5N2	IO	DIFFIO_TX46p				L7					
B5	VREFB5N2	IO	DIFFIO_RX46n				F4					
B5	VREFB5N2	IO	DIFFIO_RX46p				F3					
B5	VREFB5N2	IO	DIFFIO_TX45n				L10					
B5	VREFB5N2	IO	DIFFIO_TX45p				L9					
B5	VREFB5N2	IO	DIFFIO_RX45n				E2					
B5	VREFB5N2	IO	DIFFIO_RX45p				E1					
B5	VREFB5N2	VREFB5N2	VREFB5N2		D3	D4	F5					
B5	VREFB5N2	IO	DIFFIO_TX44n				K9					
B5	VREFB5N2	IO	DIFFIO_TX44p				K8					
B5	VREFB5N2	IO	DIFFIO_RX44n				E4					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B5	VREFB5N2	IO	DIFFIO_RX44p				E3					
B5	VREFB5N2	IO	DIFFIO_TX43n				J9					
B5	VREFB5N2	IO	DIFFIO_TX43p				J8					
B5	VREFB5N2	IO	DIFFIO_RX43n				D2					
B5	VREFB5N2	IO	DIFFIO_RX43p				D1					
B5	VREFB5N2	IO	DIFFIO_TX42n				J7					
B5	VREFB5N2	IO	DIFFIO_TX42p				J6					
B5	VREFB5N2	FPLL10CLKn	INPUT				D4					
B5	VREFB5N2	FPLL10CLKp	INPUT				D3					
		GNDA_PLL10					G7					
		GNDA_PLL10					G8					
		VCCA_PLL10					H8					
		VCCD_PLL10					H7					
		TEMPDIODEp			A2	E5	G9					
		TEMPDIODEn			C3	F5	B3					
B4	VREFB4N0	TDO		TDO	B3	F6	C3					
B4	VREFB4N0	MSEL3		MSEL3	A4	F7	H10					
B4	VREFB4N0	MSEL2		MSEL2	B4	E6	J10					
B4	VREFB4N0	MSEL1		MSEL1	D4	B2	F6					
B4	VREFB4N0	MSEL0		MSEL0	E5	G8	B2					
B4	VREFB4N0	IO	DQS0T			E7	C4		DQS0T			
B4	VREFB4N0	IO	DQ0T				B4		DQ0T			
B4	VREFB4N0	IO	DQ0T		H7	E8	D5		DQ0T			
B4	VREFB4N0	IO	DQ0T			J9	E5		DQ0T			
B4	VREFB4N0	IO	DQSn0T				C5		DQSn0T			
B4	VREFB4N0	IO	DQ0T		G7	F8	A4		DQ0T			
B4	VREFB4N0	IO					H11					
B4	VREFB4N0	IO					J11					
B4	VREFB4N0	IO	DQS1T			B3	B5		DQVLD0T			
B4	VREFB4N0	IO	DQ1T			A3	A5		DQ0T			
B4	VREFB4N0	IO	DQ1T		F6	C4	D6		DQ0T			
B4	VREFB4N0	IO	DQ1T			C3	C6		DQ0T			
B4	VREFB4N0	VREFB4N0	VREFB4N0		C4	D5	C2					
B4	VREFB4N0	IO	DQSn1T		D5	B4	B6		DQ0T			
B4	VREFB4N0	IO	DQ1T			C5	A6		DQ0T			
B4	VREFB4N0	IO					K11					
B4	VREFB4N0	IO					H12					
B4	VREFB4N0	IO	DQS2T		D6	E9	D7		DQS1T			
B4	VREFB4N0	IO	DQ2T				B7		DQ1T		DQ0T	DQ0T
B4	VREFB4N0	IO	DQ2T			K10	E7		DQ1T		DQ0T	DQ0T
B4	VREFB4N0	IO	DQ2T			H9	E6		DQ1T		DQ0T	DQ0T
B4	VREFB4N0	IO	DQSn2T				C7		DQSn1T		DQ0T	DQ0T
B4	VREFB4N0	IO	DQ2T		E6	G9	A7		DQ1T		DQ0T	DQ0T
B4	VREFB4N0	IO					J12					
B4	VREFB4N0	IO					L12					
B4	VREFB4N0	IO	DQS3T			C6	B8	DQS0T	DQVLD1T		DQS0T	
B4	VREFB4N0	IO	DQ3T		E7	A5	C9	DQ0T	DQ1T	DQ0T	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ3T			B5	A8	DQ0T	DQ1T	DQ0T	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ3T		F7	D6	C8	DQ0T	DQ1T	DQ0T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQSn3T			B6	B9	DQSn0T	DQ1T	DQ0T	DQSn0T	DQ0T
B4	VREFB4N1	IO	DQ3T			A6	A9	DQ0T	DQ1T	DQ0T	DQ0T	DQ0T
B4	VREFB4N1	IO			G8	J10	H13					
B4	VREFB4N1	IO					K12					
B4	VREFB4N1	IO	DQS4T				F9		DQS2T		DQVLD0T	DQVLD0T
B4	VREFB4N1	IO	DQ4T			H10	D8		DQ2T		DQ0T	DQ0T
B4	VREFB4N1	IO	DQ4T		H9	K11	E8		DQ2T		DQ0T	DQ0T
B4	VREFB4N1	IO	DQ4T				F8		DQ2T		DQ0T	DQ0T
B4	VREFB4N1	IO	DQSn4T			E10	E9		DQSn2T		DQ0T	DQ0T
B4	VREFB4N1	IO	DQ4T		G9	F10	F10		DQ2T		DQ0T	DQ0T
B4	VREFB4N1	IO					J13					
B4	VREFB4N1	IO					L13					
B4	VREFB4N1	IO	DQS5T			B7	C10	DQVLD0T	DQVLD2T	DQS0T		DQS0T
B4	VREFB4N1	IO	DQ5T			A7	A10	DQ0T	DQ2T	DQ0T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T		F8	C7	B10	DQ0T	DQ2T	DQ0T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T			D7	D10	DQ0T	DQ2T	DQ0T	DQ0T	DQ0T
B4	VREFB4N1	VREFB4N1	VREFB4N1		D7	F9	D9					
B4	VREFB4N1	IO	DQSn5T		D8	B8	C11	DQ0T	DQ2T	DQSn0T	DQ0T	DQSn0T
B4	VREFB4N1	IO	DQ5T			A8	D11	DQ0T	DQ2T	DQ0T		
B4	VREFB4N1	IO					H14					
B4	VREFB4N1	IO					K13					
B4	VREFB4N1	IO	DQS6T				F11		DQS3T			
B4	VREFB4N1	IO	DQ6T		E8	G10	E11		DQ3T		DQ1T	DQ0T
B4	VREFB4N1	IO	DQ6T			J11	G10		DQ3T		DQ1T	DQ0T
B4	VREFB4N1	IO	DQ6T				G11		DQ3T		DQ1T	DQ0T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B4	VREFB4N1	IO	DQSn6T			E11	F12		DQSn3T		DQ1T	DQ0T
B4	VREFB4N1	IO	DQ6T		F9	F11	G12		DQ3T		DQ1T	DQ0T
B4	VREFB4N1	IO					J14					
B4	VREFB4N1	IO					L14					
B4	VREFB4N1	IO	DQS7T		B5	C9	C12	DQS1T	DQVLD3T	DQVLD0T	DQS1T	
B4	VREFB4N1	IO	DQ7T		A5	D9	D12	DQ1T	DQ3T	DQ0T	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		C5	D8	A11	DQ1T	DQ3T	DQ0T	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		C6	C8	B11	DQ1T	DQ3T	DQ0T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQSn7T		B6	B9	B12	DQSn1T	DQ3T	DQ0T	DQSn1T	DQ0T
B4	VREFB4N2	IO	DQ7T		A6	A9	A12	DQ1T	DQ3T	DQ0T	DQ1T	DQ0T
B4	VREFB4N2	IO					K14					
B4	VREFB4N2	IO					L15					
B4	VREFB4N2	IO	DQS8T			E12	F14		DQS4T		DQVLD1T	
B4	VREFB4N2	IO	DQ8T		E9	G11	E13		DQ4T		DQ1T	DQ0T
B4	VREFB4N2	IO	DQ8T				F13		DQ4T		DQ1T	DQ0T
B4	VREFB4N2	IO	DQ8T			H11	G13		DQ4T		DQ1T	DQ0T
B4	VREFB4N2	IO	DQSn8T		E10	F12	E14		DQSn4T		DQ1T	DQ0T
B4	VREFB4N2	IO	DQ8T				F15		DQ4T		DQ1T	DQ0T
B4	VREFB4N2	IO					J15					
B4	VREFB4N2	IO					L16					
B4	VREFB4N2	IO	DQS9T		B7	C10	C13	DQVLD1T	DQVLD4T			
B4	VREFB4N2	IO	DQ9T		A7	C11	B14	DQ1T	DQ4T	DQ0T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		C8	A10	D14	DQ1T	DQ4T	DQ0T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		C7	D10	D13	DQ1T	DQ4T	DQ0T	DQ1T	
B4	VREFB4N2	VREFB4N2	VREFB4N2		D9	D11	C14					
B4	VREFB4N2	IO	DQSn9T		B8	B10	B13	DQ1T	DQ4T	DQ0T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		A8	B11	A14	DQ1T	DQ4T			
B4	VREFB4N2	IO					K15					
B4	VREFB4N2	IO					L17					
B4	VREFB4N2	IO					K17					
B4	VREFB4N2	IO				F13	K16					
B9	VREFB4N2	IO	PLL5_FBn/OUT2n		C9	D12	E15					
B9	VREFB4N2	IO	PLL5_FBp/OUT2p		B9	C12	D15					
B9	VREFB4N2	IO	PLL5_OUT0n		B10	B12	C15					
B9	VREFB4N2	IO	PLL5_OUT0p		A10	A12	B15					
B9	VREFB4N2	IO	PLL5_OUT1n		D10	E13	D16					
B9	VREFB4N2	IO	PLL5_OUT1p		C10	D13	C16					
B4	VREFB4N2	IO	CLK12n		C11	C13	B16					
B4	VREFB4N2	IO	CLK12p		B11	B13	A16					
B4	VREFB4N2	IO	CLK13n		C12	C14	F16					
B4	VREFB4N2	IO	CLK13p		B12	B14	E16					
B9		VCC_PLL5_OUT			G10	H12	J16					
		VCCD_PLL5			G11	H14	H15					
		VCCA_PLL5			F12	G12	G15					
		GNDA_PLL5			F10	H13	G16					
		GNDA_PLL5			F11	J13	H16					
		GNDA_PLL11					G18					
		GNDA_PLL11					H18					
		VCCA_PLL11					H17					
		VCCD_PLL11					J18					
B11		VCC_PLL11_OUT					J17					
B3	VREFB3N0	IO	CLK14p		A13	A15	A17					
B3	VREFB3N0	IO	CLK14n		B13	B15	B17					
B3	VREFB3N0	IO	CLK15p		C13	C15	C17					
B3	VREFB3N0	IO	CLK15n		D13	D15	D17					
B11	VREFB3N0	IO	PLL11_OUT0p				B18					
B11	VREFB3N0	IO	PLL11_OUT0n			D14	C18					
B11	VREFB3N0	IO	PLL11_OUT1p				D18					
B11	VREFB3N0	IO	PLL11_OUT1n				E18					
B3	VREFB3N0	IO					K18					
B3	VREFB3N0	IO			F13	J14	L18					
B11	VREFB3N0	IO	PLL11_FBp/OUT2p				A19					
B11	VREFB3N0	IO	PLL11_FBn/OUT2n				B19					
B3	VREFB3N0	IO		PGM2	D12	E15	F18					
B3	VREFB3N0	IO		PGM1	E11	F15	F19					
B3	VREFB3N0	IO		PGM0	H11	F14	E17					
B3	VREFB3N0	IO		ASDO	G12	G14	F17					
B3	VREFB3N0	IO		nCSO	D11	E14	G19					
B3	VREFB3N0	IO		CRC_ERROR	E12	F16	G20					
B3	VREFB3N0	IO		DATA0	E13	E16	H19					
B3	VREFB3N0	IO		DATA1	H12	G15	F20					
B3	VREFB3N0	VREFB3N0	VREFB3N0		B14	D16	C19					
B3	VREFB3N0	IO	DQS10T			D17	D19		DQS5T			
B3	VREFB3N0	IO	DQ10T				B20		DQ5T		DQ2T	DQ1T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B3	VREFB3N0	IO	DQ10T		G13	H15	E19		DQ5T		DQ2T	DQ1T
B3	VREFB3N0	IO	DQ10T				C20		DQ5T		DQ2T	DQ1T
B3	VREFB3N0	IO	DQSn10T			G16	D20		DQSn5T		DQ2T	DQ1T
B3	VREFB3N0	IO	DQ10T		E14	J15	E20		DQ5T		DQ2T	DQ1T
B3	VREFB3N0	IO					K19					
B3	VREFB3N0	IO					L19					
B3	VREFB3N0	IO	DQS11T		B15	B16	B21	DQS2T	DQVLD5T		DQS2T	
B3	VREFB3N0	IO	DQ11T		A15	C16	A21	DQ2T	DQ5T	DQ1T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		C15	A17	C21	DQ2T	DQ5T	DQ1T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		C16	C17	A22	DQ2T	DQ5T	DQ1T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQSn11T		B16	B17	B22	DQSn2T	DQ5T	DQ1T	DQSn2T	DQ1T
B3	VREFB3N1	IO	DQ11T		A16	A18	C22	DQ2T	DQ5T	DQ1T	DQ2T	DQ1T
B3	VREFB3N1	IO					H20					
B3	VREFB3N1	IO				H16	J19					
B3	VREFB3N1	IO	DQS12T				D22		DQS6T		DQVLD2T	DQVLD1T
B3	VREFB3N1	IO	DQ12T		F14	F17	D23		DQ6T		DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T				D21		DQ6T		DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T			K16	F22		DQ6T		DQ2T	DQ1T
B3	VREFB3N1	IO	DQSn12T				E22		DQSn6T		DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T		E15	G17	F23		DQ6T		DQ2T	DQ1T
B3	VREFB3N1	IO					K20					
B3	VREFB3N1	IO				H17	J20					
B3	VREFB3N1	IO	DQS13T		B17	B18	B23	DQVLD2T	DQVLD6T	DQS1T		DQS1T
B3	VREFB3N1	IO	DQ13T		A17	A19	A23	DQ2T	DQ6T	DQ1T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		A18	C18	C23	DQ2T	DQ6T	DQ1T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		C17	C19	C24	DQ2T	DQ6T	DQ1T	DQ2T	DQ1T
B3	VREFB3N1	VREFB3N1	VREFB3N1		D16	F18	D24					
B3	VREFB3N1	IO	DQSn13T		B18	B19	B24	DQ2T	DQ6T	DQSn1T	DQ2T	DQSn1T
B3	VREFB3N1	IO	DQ13T		C18	A20	A24	DQ2T	DQ6T	DQ1T		
B3	VREFB3N1	IO					H21					
B3	VREFB3N1	IO					L20					
B3	VREFB3N1	IO	DQS14T		D15	E17	B25		DQS7T			
B3	VREFB3N1	IO	DQ14T				A25		DQ7T		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ14T			J17	A26		DQ7T		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ14T				D26		DQ7T		DQ3T	DQ1T
B3	VREFB3N1	IO	DQSn14T		D14	G18	B26		DQSn7T		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ14T				C26		DQ7T		DQ3T	DQ1T
B3	VREFB3N1	IO					J21					
B3	VREFB3N1	IO				K17	K21					
B3	VREFB3N1	IO	DQS15T		C14	B20	D25	DQS3T	DQVLD7T	DQVLD1T	DQS3T	
B3	VREFB3N1	IO	DQ15T			A21	E24	DQ3T	DQ7T	DQ1T	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		G14	C20	C25	DQ3T	DQ7T	DQ1T	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T			C21	E27	DQ3T	DQ7T	DQ1T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQSn15T		F15	B21	E25	DQSn3T	DQ7T	DQ1T	DQSn3T	DQ1T
B3	VREFB3N2	IO	DQ15T			A22	E26	DQ3T	DQ7T	DQ1T	DQ3T	DQ1T
B3	VREFB3N2	IO					G21					
B3	VREFB3N2	IO			G15	H18	L21					
B3	VREFB3N2	IO	DQS16T				B27		DQS8T		DQVLD3T	
B3	VREFB3N2	IO	DQ16T			E18	A27		DQ8T		DQ3T	DQ1T
B3	VREFB3N2	IO	DQ16T				A28		DQ8T		DQ3T	DQ1T
B3	VREFB3N2	IO	DQ16T		F16	J18	D27		DQ8T		DQ3T	DQ1T
B3	VREFB3N2	IO	DQSn16T				B28		DQSn8T		DQ3T	DQ1T
B3	VREFB3N2	IO	DQ16T			D18	C27		DQ8T		DQ3T	DQ1T
B3	VREFB3N2	IO					J22					
B3	VREFB3N2	IO					K22					
B3	VREFB3N2	IO	DQS17T		H14	B23	C28	DQVLD3T	DQVLD8T			
B3	VREFB3N2	IO	DQ17T			C22	B29	DQ3T	DQ8T	DQ1T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		J15	B22	A29	DQ3T	DQ8T	DQ1T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T			A24	D28	DQ3T	DQ8T	DQ1T	DQ3T	
B3	VREFB3N2	VREFB3N2	VREFB3N2		C19	D22	C31					
B3	VREFB3N2	IO	DQSn17T		G16	C23	C29	DQ3T	DQ8T	DQ1T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T			B24	E28	DQ3T	DQ8T			
B3	VREFB3N2	IO					H22					
B3	VREFB3N2	IO			H16	K18	G22					
B3	VREFB3N2	IO		DATA2	D17	E19	G23					
B3	VREFB3N2	IO		DATA3	A19	D20	H23					
B3	VREFB3N2	IO		DATA4	E16	G19	J23					
B3	VREFB3N2	IO		DATA5	E17	D19	L22					
B3	VREFB3N2	IO		DATA6	B19	E20	F24					
B3	VREFB3N2	IO		DATA7	D18	F20	G24					
B3	VREFB3N2	IO		RDYnBSY	F17	F19	H24					
B3	VREFB3N2	IO		INIT_DONE	E18	D21	G25					
B3	VREFB3N2	nSTATUS		nSTATUS	B20	E21	B30					
B3	VREFB3N2	nCE		nCE	A21	E22	C30					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
B3	VREFB3N2	DCLK		DCLK	D19	C24	B31					
B3	VREFB3N2	CONF_DONE		CONF_DONE	C20	B25	J25					
		VCCIO2			B22	D26	C32					
		VCCIO2			L22	L26	M28					
		VCCIO2				M17	R32					
		VCCIO2					T21					
		VCCIO1			AA22	AC26	AA28					
		VCCIO1			M22	P17	AK32					
		VCCIO1				T26	U21					
		VCCIO1					V32					
		VCCIO8			AB12	AF16	AA17					
		VCCIO8			AB20	AF23	AH21					
		VCCIO8				U14	AM18					
		VCCIO8					AM30					
		VCCIO7			AB3	AF4	AA16					
		VCCIO7			AB11	AF11	AH12					
		VCCIO7				U12	AM3					
		VCCIO7					AM15					
		VCCIO6			AA1	AC1	AA5					
		VCCIO6			M1	R10	AK1					
		VCCIO6				T1	U12					
		VCCIO6					V1					
		VCCIO5			B1	D1	C1					
		VCCIO5			L1	L1	M5					
		VCCIO5				N10	R1					
		VCCIO5					T12					
		VCCIO4			A3	A4	A3					
		VCCIO4			A11	A11	A15					
		VCCIO4				K13	E12					
		VCCIO4					M16					
		VCCIO3			A12	A16	A18					
		VCCIO3			A20	A23	A30					
		VCCIO3				K15	E21					
		VCCIO3					M17					
		VCCINT			H8	L10	AA12					
		VCCINT			J9	L12	AC10					
		VCCINT			J11	L14	K10					
		VCCINT			J13	L16	K23					
		VCCINT			K10	M11	M21					
		VCCINT			K12	M13	N13					
		VCCINT			L11	M15	N15					
		VCCINT			L13	N12	N17					
		VCCINT			M8	N14	N19					
		VCCINT			M10	N16	P14					
		VCCINT			M12	P11	P16					
		VCCINT			M14	P13	P18					
		VCCINT			N11	P15	P20					
		VCCINT			N13	R12	R13					
		VCCINT			P9	R14	R15					
		VCCINT			P12	R16	R17					
		VCCINT			P14	T11	R19					
		VCCINT				T13	T14					
		VCCINT				T15	T16					
		VCCINT				T17	T18					
		VCCINT				U10	T20					
		VCCINT				U16	U13					
		VCCINT				U18	U15					
		VCCINT				V9	U17					
		VCCINT					U19					
		VCCINT					V14					
		VCCINT					V16					
		VCCINT					V18					
		VCCINT					V20					
		VCCINT					W13					
		VCCINT					W15					
		VCCINT					W17					
		VCCINT					W19					
		VCCINT					W21					
		VCCINT					Y14					
		VCCINT					Y16					
		VCCINT					Y18					
		VCCINT					Y20					
		GND			A1	A2	A2					
		GND			A9	A13	A13					

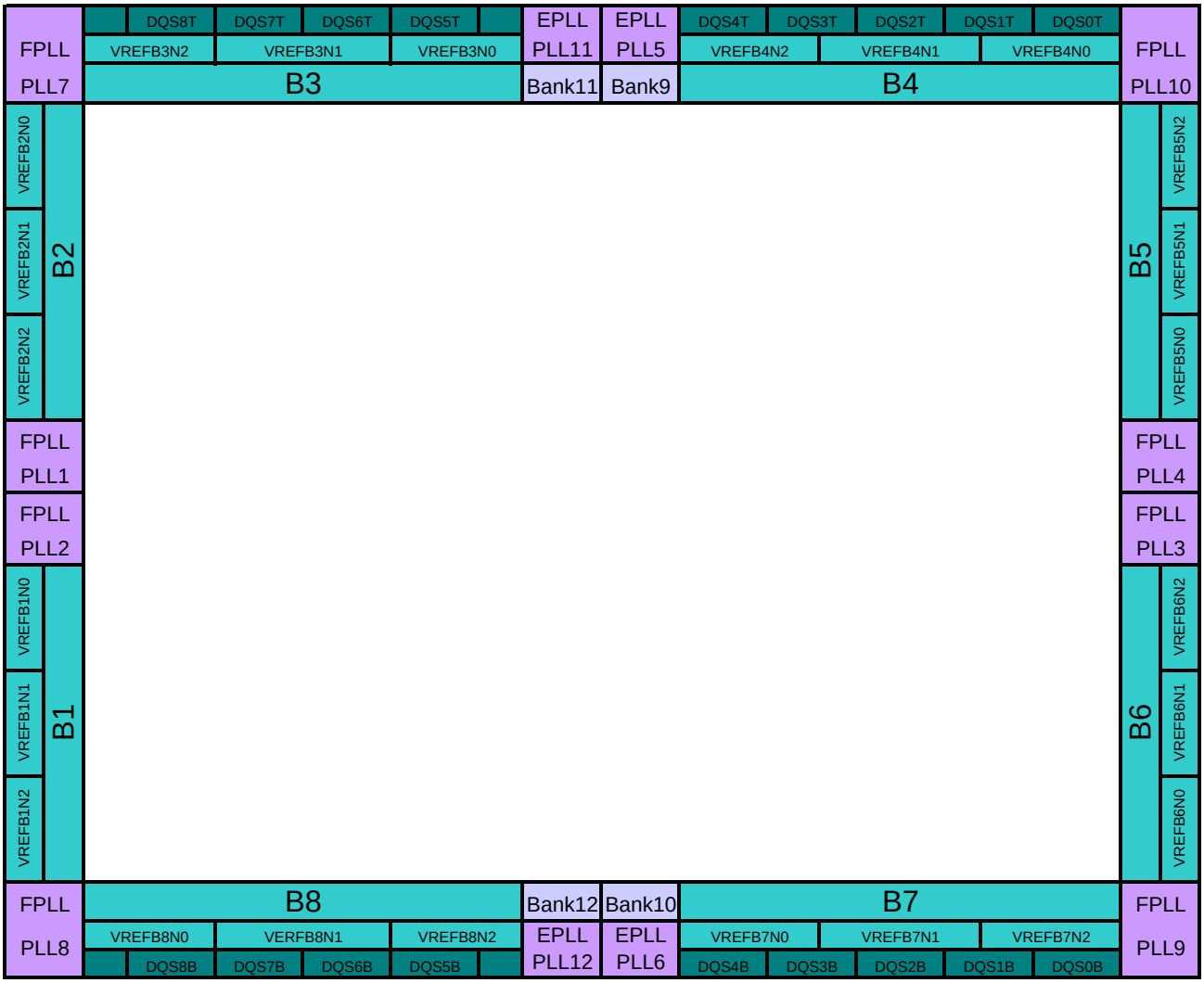
Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
		GND				A14	A20					
		GND					A31					
		GND			A14	A25	AA14					
		GND			A22	AA13	AA19					
		GND				AE1	AA21					
		GND					AB22					
		GND			AA2	AE26	AC5					
		GND			AA21	AF2	AC28					
		GND				AF13	AF17					
		GND					AG6					
		GND			AB1	AF14	AH10					
		GND			AB9	AF25	AH23					
		GND				B1	AH27					
		GND					AL1					
		GND			AB14	B26	AL32					
		GND			AB22	G13	AM2					
		GND				K12	AM13					
		GND					AM20					
		GND			B2	K14	AM31					
		GND			B21	L11	B1					
		GND				L13	B32					
		GND					E10					
		GND			H15	L15	E23					
		GND			J1	L17	F7					
		GND				M10	F27					
		GND					G17					
		GND			J10	M12	J24					
		GND			J12	M14	K5					
		GND				M16	K28					
		GND					L11					
		GND			J14	N1	M12					
		GND			J22	N11	M14					
		GND			K9	N13	M19					
		GND			K11	N15	N1					
		GND			K13	N17	N14					
		GND			L10	N26	N16					
		GND			L12	P1	N18					
		GND			L14	P6	N20					
		GND			M7	P10	N32					
		GND			M9	P12	P12					
		GND			M11	P14	P13					
		GND			M13	P16	P15					
		GND			M15	P26	P17					
		GND			N10	R11	P19					
		GND			N12	R13	P21					
		GND			N14	R15	R14					
		GND			P1	R17	R16					
		GND			P11	R22	R18					
		GND			P13	T10	R20					
		GND			P22	T12	T7					
		GND			R10	T14	T13					
		GND				T16	T15					
		GND				T18	T17					
		GND				U9	T19					
		GND				U11	U14					
		GND				U13	U16					
		GND				U15	U18					
		GND				U17	U20					
		GND					V11					
		GND					V13					
		GND					V15					
		GND					V17					
		GND					V19					
		GND					V22					
		GND					V27					
		GND					W12					
		GND					W14					
		GND					W16					
		GND					W18					
		GND					W20					
		GND					Y1					
		GND					Y13					
		GND					Y15					
		GND					Y17					

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/ DQS for x4	Configuration Function	F484	F672	F1020	DQS for x8/x9 in F484/F672	DQS for x8/x9 in F1020	DQS for x16/x18 in F672	DQS for x16/x18 in F1020	DQS for x32/x36 in F1020
		GND					Y19					
		GND					Y32					
		VCCPD2			K14	M18	N21					
		VCCPD2					R21					
		VCCPD1			P15	R18	V21					
		VCCPD1					Y21					
		VCCPD8			R13	V15	AA18					
		VCCPD8					AA20					
		VCCPD7			P10	V11	AA13					
		VCCPD7					AA15					
		VCCPD6			N9	R9	V12					
		VCCPD6					Y12					
		VCCPD5			L9	M9	N12					
		VCCPD5					R12					
		VCCPD4			H10	J12	M13					
		VCCPD4					M15					
		VCCPD3			H13	J16	M18					
		VCCPD3					M20					
		NC					AC29					
		NC					AC30					
		NC					AD3					
		NC					AD4					
		NC					AD29					
		NC					AD30					
		NC					AE5					
		NC					AE6					
		NC					AE9					
		NC					AF5					
		NC					AF6					
		NC					AF14					
		NC					AF27					
		NC					AF28					
		NC					AG21					
		NC					AG25					
		NC					F21					
		NC					F25					
		NC					G5					
		NC					G6					
		NC					G14					
		NC					G27					
		NC					G28					
		NC					H3					
		NC					H4					
		NC					H5					
		NC					H6					
		NC					H9					
		NC					J29					
		NC					J30					
		NC					L27					
		NC					L28					
		NC					N10					
		NC					N11					
		NC					P22					
		NC					P23					
		NC					W10					
		NC					W11					
		NC					W22					
		NC					W23					

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HyperTransport™ technology, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCPD[1..8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The VCCPD pins must be connected to 3.3 V and must ramp-up from 0 V to 3.3 V within 100 ms to ensure successful configuration. If you use the AES key programming feature of the device, VCCPD8 powers the circuitry enabling the key to be programmed in non-volatile memory. During key programming, apply 3.7 V to VCCPD8. Refer to AN341-Using the Design Security Feature in Stratix II and Stratix II GX Devices for more information.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[1..8]N[0..2]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All the VREF pins within a bank are shorted together. If VREF pins are not used, designers should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p & PLL5_FBn/OUT2n. This pin is the VCCIO pin for bank 9.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p & PLL6_FBn/OUT2n. This pin is the VCCIO pin for bank 10.
VCC_PLL11_OUT	Power	External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p & PLL11_FBn/OUT2n. This pin is the VCCIO pin for bank 11. The 484 pin and 672 pin packages do not support VCC_PLL11_OUT because they do not have EPLL11. For those packages, the bank 11 I/O pins are powered by VCCIO for bank 3.
VCC_PLL12_OUT	Power	External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p & PLL12_FBn/OUT2n. This pin is the VCCIO pin for bank 12. The 484 pin and 672 pin packages do not support VCC_PLL12_OUT because they do not have EPLL12. For those packages, the bank 12 I/O pins are powered by VCCIO for bank 8.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
VCCD_PLL[1..12]	Power	Digital power for PLLs[1..12]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12].
NC	No Connect	Do not drive signals into these pins.
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD or ground. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix II device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix II device. If the temperature sensing diode is not used then connect this pin to GND.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Stratix II device. In AS mode, DCLK is an output from the Stratix II device that provides timing for the configuration interface. In PPA mode, DCLK should be tied to VCC to prevent this pin from floating.
MSEL[0..3]	Input	Configuration input pins that set the Stratix II device configuration scheme. These pins must be hard-wired to VCCPD or GND.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to VCC or to the configuration device's nINIT_CONF pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. The JTAG circuitry can be disabled by connecting TRST to GND.
		Clock and PLL Pins
CLK[1,3,9,11]p	Clock, Input	Dedicated clock input pins 1, 3, 9, & 11 that can also be used for data inputs.
CLK[1,3,9,11]n	Clock, Input	Dedicated negative terminal clock input pins for differential clock input that can also be used for data inputs.
CLK[0,2,8,10]p/DIFFIO_RX_C[0..3]p	I/O, Clock, RX channel	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[0,2,8,10]n/DIFFIO_RX_C[0..3]n	I/O, Clock, RX channel	These pins can be used as I/O pins, the negative terminal clock input pins for differential clock input, or the negative terminal data pins of differential receiver channels.
CLK[4-7,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-7,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative terminal clock input pins for differential clock input.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FPLL[7..10]CLKp	Clock, Input	Dedicated clock inputs for fast PLLs (PLLs 7 through 10) that can also be used for data inputs.
FPLL[7..10]CLKn	Clock, Input	Dedicated negative terminal associated with FPLL[7..10]CLKp pins that can also be used for data inputs.
PLL5_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5). When not used as PLL output, these pins can be used as I/O with single ended inputs only. They cannot be used as differential input.
PLL5_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL6_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6). When not used as PLL output, these pins can be used as I/O with single ended inputs only. They cannot be used as differential input.
PLL6_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[5..6]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[5..6].
PLL[5..6]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[5..6]_FBp or negative terminal clock output pins for differential clock output.
PLL11_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 11. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL11). When not used as PLL output, these pins can be used as I/O with single ended inputs only. They cannot be used as differential input.
PLL11_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL11. If the clock outputs are single ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL12_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 12. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL12). When not used as PLL output, these pins can be used as I/O with single ended inputs only. They cannot be used as differential input.
PLL12_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL12. If the clock outputs are single ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[11..12]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[11..12].
PLL[11..12]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[11..12]_FBp or negative terminal clock output pins for differential clock output.
		Optional/Dual-Purpose Configuration Pins
nCSO	I/O (non-AS mode), Output	Output control signal from the Stratix II FPGA to the serial configuration device in AS mode that enables the configuration device.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
ASDO	I/O (non-AS mode), Output	Control signal from the Stratix II FPGA to the serial configuration device in AS mode used to read out configuration data.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete.
DATA[1..7]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
DATA7	I/O, Bidirectional	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal has been strobed low.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
nCS, CS	I/O, Input	These are chip-select inputs that enable the Stratix II device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. If the nRS pin is not used in PPA mode, it should be tied high. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
PGM[0..2]	I/O, Output	These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUnLU	I/O, Input	Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration modes, this pin is available as general-purpose user I/O pin.
Dual-Purpose Differential & External Memory Interface Pins		
DIFFIO_RX[1..40, 43..82]p/n	I/O, RX channel	Dual-purpose differential receiver channels 1 to 40 and channels 43 to 82. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[0..83]p/n	I/O, TX channel	Dual-purpose differential transmitter channels 0 to 83. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[0..17][T,B]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[0..17][T,B]	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.
DQ[0..17][T,B]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DQVLD[0..8][T,B]	I/O, DQVLD	Optional data valid signal for use in external memory interfacing.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
3. The DQ/DQS groups depicted above are in x8/x9 mode. DQ/DQS support differs across the package offerings.

Version Number	Date	Changes Made
1.0	1/21/2004	Initial revision
1.1	2/25/2004	Changed pin names PLL[5, 6,11,12]_FBp/OUT2n to PLL[5,6,11,12]_FBn/OUT2n
		Added the F484 and F672 packages
1.2	3/18/2004	Added "DQS for x32/x36" column to Pin List
		Added "DQS for x8/x9 in F484/F672" & "DQS for x16/x18 in F672" columns, & changed column name from "DQS for x8/x9" to "DQS for x8/x9 in F1020" & from "DQS for x16/x18" to "DQS for x6/x8 in F1020" in Pin List
1.3	3/31/2004	Changed pin names from CLK[10,8,2,0]p to CLK[10,8,2,0]p/DIFFIO_RX_C[3..0]p & CLK[10,8,2,0]n to CLK[10,8,2,0]n/DIFFIO_RX_C[3..0]n in Pin List
		File status changed to Final
1.4	7/23/2004	Added CRC_ERROR in pin list and pin definitions
1.5	9/10/2004	Removed DQ bit indices
		Updated DQ and NC definitions
1.6	11/26/2004	Removed bank and VREF assignment from GND pins in pin list
1.7	6/27/2005	Updated Pin List to include DQS for x4
		Updated Pin Description for VCCPD
		Updated Pin Description for VCC_PLL11/12_OUT
1.8	6/16/2006	Changed VCC_PLLx_out definitions from "This pin should be connected to the VCCIO level of bank x" to "This pin is the VCCIO pin for bank x".
		Added input usage informations for PLLx_OUT[0..1]p
1.9	2/5/2007	Corrected numbering of DIFFIO_RX in pin description.
2.0	2/13/2007	Removed redundant rows and updated the description for VCCPD8 during key programming.