Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L5		GXB_TX_L32n					E35				
GXB_L5		GXB_TX_L32p					E34				
GXB_L5		GXB_RX_L32n,GXB_REFCLK_L32n					C39				
GXB_L5		GXB_RX_L32p,GXB_REFCLK_L32p					C38				
GXB_L5		GXB_TX_L31n					F33				
GXB_L5		GXB_TX_L31p					F32				
GXB_L5		GXB_RX_L31n,GXB_REFCLK_L31n					D37				
GXB_L5		GXB_RX_L31p,GXB_REFCLK_L31p					D36				
GXB_L5		GXB_TX_L30n					G35				
GXB_L5		GXB_TX_L30p					G34				
GXB_L5		GXB_RX_L30n,GXB_REFCLK_L30n					E39				
GXB_L5		GXB_RX_L30p,GXB_REFCLK_L30p					E38				
GXB_L5		REFCLK10Lp					L29				
GXB_L5		REFCLK10Ln					L30				
GXB_L4		REFCLK9Lp					N29				
GXB_L4		REFCLK9Ln					N30				
GXB_L4		GXB_TX_L29n					H33				
GXB_L4		GXB_TX_L29p					H32				
GXB_L4		GXB_RX_L29n,GXB_REFCLK_L29n					F37				
GXB_L4		GXB_RX_L29p,GXB_REFCLK_L29p					F36				
GXB_L4		GXB_TX_L28n					J35				
GXB_L4		GXB_TX_L28p					J34				
GXB_L4		GXB_RX_L28n,GXB_REFCLK_L28n					G39				
GXB_L4		GXB_RX_L28p,GXB_REFCLK_L28p					G38				
GXB_L4		GXB_TX_L27n					K33				
GXB_L4		GXB_TX_L27p					K32				
GXB_L4		GXB_RX_L27n,GXB_REFCLK_L27n					H37				
GXB_L4		GXB_RX_L27p,GXB_REFCLK_L27p					H36				
GXB_L4		GXB_TX_L26n					L35				
GXB_L4		GXB_TX_L26p					L34				
GXB_L4		GXB_RX_L26n,GXB_REFCLK_L26n					J39				
GXB_L4		GXB_RX_L26p,GXB_REFCLK_L26p					J38				
GXB_L4		GXB_TX_L25n					M33				
GXB_L4		GXB_TX_L25p					M32				
GXB_L4		GXB_RX_L25n,GXB_REFCLK_L25n					K37				
GXB_L4		GXB_RX_L25p,GXB_REFCLK_L25p					K36				
GXB_L4		GXB_TX_L24n					N35				
GXB_L4		GXB_TX_L24p					N34				
GXB_L4		GXB_RX_L24n,GXB_REFCLK_L24n					L39				
GXB_L4		GXB_RX_L24p,GXB_REFCLK_L24p					L38				
GXB_L4		REFCLK8Lp					R30				
GXB_L4		REFCLK8Ln					R31				
GXB_L3		REFCLK7Lp					U29				
GXB_L3		REFCLK7Ln					U30				
GXB_L3		GXB_TX_L23n					P33				
GXB_L3		GXB_TX_L23p					P32				
GXB_L3		GXB_RX_L23n,GXB_REFCLK_L23n					M37				
GXB_L3		GXB_RX_L23p,GXB_REFCLK_L23p					M36				
GXB_L3		GXB_TX_L22n					P37				
GXB_L3		GXB_TX_L22p					P36				
GXB_L3		GXB_RX_L22n,GXB_REFCLK_L22n					N39				
GXB_L3		GXB_RX_L22p,GXB_REFCLK_L22p					N38				
GXB_L3		GXB_TX_L21n					R35				
GXB_L3		GXB_TX_L21p					R34				
GXB_L3		GXB_RX_L21n,GXB_REFCLK_L21n					R39				
GXB_L3		GXB_RX_L21p,GXB_REFCLK_L21p					R38				
GXB_L3		GXB_TX_L20n					T33				
GXB_L3		GXB_TX_L20p					T32				
GXB_L3		GXB_RX_L20n,GXB_REFCLK_L20n					T37				
GXB_L3		GXB_RX_L20p,GXB_REFCLK_L20p					T36				
GXB_L3		GXB_TX_L19n					U35				
GXB_L3		GXB_TX_L19p					U34				
GXB_L3		GXB_RX_L19n,GXB_REFCLK_L19n					U39				
GXB_L3		GXB_RX_L19p,GXB_REFCLK_L19p					U38				
GXB_L3		GXB_TX_L18n					V33				
GXB_L3		GXB_TX_L18p					V32				
GXB_L3		GXB_RX_L18n,GXB_REFCLK_L18n					V37				
GXB_L3		GXB_RX_L18p,GXB_REFCLK_L18p					V36				
GXB_L3		REFCLK6Lp					W30				
GXB_L3		REFCLK6Ln					W31				
GXB_L2		REFCLK5Lp					AA29				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L2		REFCLK5Ln					AA30				
GXB_L2		GXB_TX_L17n					W35				
GXB_L2		GXB_TX_L17p					W34				
GXB_L2		GXB_RX_L17n,GXB_REFCLK_L17n					W39				
GXB_L2		GXB_RX_L17p,GXB_REFCLK_L17p					W38				
GXB_L2		GXB_TX_L16n					Y33				
GXB_L2		GXB_TX_L16p					Y32				
GXB_L2		GXB_RX_L16n,GXB_REFCLK_L16n					AA39				
GXB_L2		GXB_RX_L16p,GXB_REFCLK_L16p					AA38				
GXB_L2		GXB_TX_L15n					Y37				
GXB_L2		GXB_TX_L15p					Y36				
GXB_L2		GXB_RX_L15n,GXB_REFCLK_L15n					AB37				
GXB_L2		GXB_RX_L15p,GXB_REFCLK_L15p					AB36				
GXB_L2		GXB_TX_L14n					AA35				
GXB_L2		GXB_TX_L14p					AA34				
GXB_L2		GXB_RX_L14n,GXB_REFCLK_L14n					AC39				
GXB_L2		GXB_RX_L14p,GXB_REFCLK_L14p					AC38				
GXB_L2		GXB_TX_L13n					AB33				
GXB_L2		GXB_TX_L13p					AB32				
GXB_L2		GXB_RX_L13n,GXB_REFCLK_L13n					AD37				
GXB_L2		GXB_RX_L13p,GXB_REFCLK_L13p					AD36				
GXB_L2		GXB_TX_L12n					AC35				
GXB_L2		GXB_TX_L12p					AC34				
GXB_L2		GXB_RX_L12n,GXB_REFCLK_L12n					AE39				
GXB_L2		GXB_RX_L12p,GXB_REFCLK_L12p					AE38				
GXB_L2		REFCLK4Lp					AC30				
GXB_L2		REFCLK4Ln					AC31				
GXB_L1		REFCLK3Lp					AE29				
GXB_L1		REFCLK3Ln					AE30				
GXB_L1		GXB_TX_L11n					AD33				
GXB_L1		GXB_TX_L11p					AD32				
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					AF37				
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					AF36				
GXB_L1		GXB_TX_L10n					AE35				
GXB_L1		GXB_TX_L10p					AE34				
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					AG39				
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					AG38				
GXB_L1		GXB_TX_L9n					AF33				
GXB_L1		GXB_TX_L9p					AF32				
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					AH37				
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					AH36				
GXB_L1		GXB_TX_L8n					AG35				
GXB_L1		GXB_TX_L8p					AG34				
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					AJ39				
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					AJ38				
GXB_L1		GXB_TX_L7n					AH33				
GXB_L1		GXB_TX_L7p					AH32				
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					AK37				
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					AK36				
GXB_L1		GXB_TX_L6n					AJ35				
GXB_L1		GXB_TX_L6p					AJ34				
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					AL39				
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					AL38				
GXB_L1		REFCLK2Lp					AG30				
GXB_L1		REFCLK2Ln					AG31				
GXB_L0		REFCLK1Lp					AJ29				
GXB_L0		REFCLK1Ln					AJ30				
GXB_L0		GXB_TX_L5n					AK33				
GXB_L0		GXB_TX_L5p					AK32				
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					AM37				
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					AM36				
GXB_L0		GXB_TX_L4n					AL35				
GXB_L0		GXB_TX_L4p					AL34				
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AN39				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AN38				
GXB_L0		GXB_TX_L3n					AM33				
GXB_L0		GXB_TX_L3p					AM32				
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AP37				
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AP36				
GXB_L0		GXB_TX_L2n					AN35				
GXB_L0		GXB_TX_L2p					AN34				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AR39				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AR38				
GXB_L0		GXB_TX_L1n					AP33				
GXB_L0		GXB_TX_L1p					AP32				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AT37				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AT36				
GXB_L0		GXB_TX_L0n					AR35				
GXB_L0		GXB_TX_L0p					AR34				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AU39				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AU38				
GXB_L0		REFCLK0Lp					AL30				
GXB_L0		REFCLK0Ln					AL31				
3A		nCONFIG		nCONFIG			AW35				
3A		TRST		TRST			AV35				
3A		TMS		TMS			AV33				
3A		TCK		TCK			AW33				
3A		TDI		TDI			AR31				
3A		TDO		TDO			AM28				
3A		nCSO		nCSO			AU34				
3A		AS_DATA3		AS_DATA3			AU33				
3A		AS_DATA2		AS_DATA2			AV34				
3A		AS_DATA1		AS_DATA1			AW34				
3A		AS_DATA0,ASDO		AS_DATA0,ASDO			AT33				
3A		DCLK		DCLK			AN28				
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_TX_B1n	DIFFOUT_B1n	AT32	DQ1B	DQ1B		
3A	VREFB3AN0	IO		CRC_ERROR	DIFFIO_TX_B1p	DIFFOUT_B1p	AU32	DQ1B	DQ1B		
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_RX_B2n	DIFFOUT_B2n	AP30	DQSn1B	DQ1B		
3A	VREFB3AN0	IO		DEV_OE	DIFFIO_RX_B2p	DIFFOUT_B2p	AR30	DQS1B	DQ1B/CQn1B		
3A	VREFB3AN0	IO		DEV_CLRn	DIFFIO_TX_B3n	DIFFOUT_B3n	AU31	DQ1B	DQ1B		
3A	VREFB3AN0	IO		INIT_DONE	DIFFIO_TX_B3p	DIFFOUT_B3p	AT31	DQ1B	DQ1B		
3A	VREFB3AN0	IO		nCEO	DIFFIO_RX_B4n	DIFFOUT_B4n	AV30	DQSn2B	DQSn1B/DQ1B		
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B4p	DIFFOUT_B4p	AV31	DQS2B	DQS1B/CQ1B		
3A	VREFB3AN0	IO		PR_REQUEST	DIFFIO_TX_B5n	DIFFOUT_B5n	AW30	DQ2B	DQ1B		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B5p	DIFFOUT_B5p	AW31	DQ2B	DQ1B		
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B6n	DIFFOUT_B6n	AU29	DQ2B	DQ1B		
3A	VREFB3AN0	IO		CvP_CONFDONE	DIFFIO_RX_B6p	DIFFOUT_B6p	AT29	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B7n	DIFFOUT_B7n	AT28	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B7p	DIFFOUT_B7p	AR29	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA0	DIFFIO_RX_B8n	DIFFOUT_B8n	AR28	DQSn3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA1	DIFFIO_RX_B8p	DIFFOUT_B8p	AR27	DQS3B	DQ2B/CQn2B	DQ1B	
3A	VREFB3AN0	IO		DATA2	DIFFIO_TX_B9n	DIFFOUT_B9n	AN27	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA3	DIFFIO_TX_B9p	DIFFOUT_B9p	AP27	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA4	DIFFIO_RX_B10n	DIFFOUT_B10n	AL26	DQSn4B	DQSn2B/DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_RX_B10p	DIFFOUT_B10p	AM27	DQS4B	DQS2B/CQ2B	DQ1B/CQn1B	
3A	VREFB3AN0	IO		DATA6	DIFFIO_TX_B11n	DIFFOUT_B11n	AK25	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B11p	DIFFOUT_B11p	AL25	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B12n	DIFFOUT_B12n	AJ26	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_RX_B12p	DIFFOUT_B12p	AK26	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_TX_B13n	DIFFOUT_B13n	AE25	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B13p	DIFFOUT_B13p	AE26	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B14n	DIFFOUT_B14n	AC25	DQSn5B	DQ3B	DQSn1B/DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_RX_B14p	DIFFOUT_B14p	AD25	DQS5B	DQ3B/CQn3B	DQS1B/CQ1B	
3A	VREFB3AN0	IO		DATA14	DIFFIO_TX_B15n	DIFFOUT_B15n	AC27	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B15p	DIFFOUT_B15p	AD27	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B16n	AH26	DQSn6B	DQSn3B/DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B16p	AH27	DQS6B	DQS3B/CQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AG27	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AF27	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK5n		DIFFIO_RX_B18n	DIFFOUT_B18n	AG25	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK5p		DIFFIO_RX_B18p	DIFFOUT_B18p	AF25	DQ6B	DQ3B	DQ1B	
3B	VREFB3BN0	IO		DATA16	DIFFIO_TX_B19n	DIFFOUT_B19n	AV28	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA17	DIFFIO_TX_B19p	DIFFOUT_B19p	AU28	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA18	DIFFIO_RX_B20n	DIFFOUT_B20n	AW28	DQSn7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA19	DIFFIO_RX_B20p	DIFFOUT_B20p	AW27	DQS7B	DQ4B/CQn4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA20	DIFFIO_TX_B21n	DIFFOUT_B21n	AV27	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA21	DIFFIO_TX_B21p	DIFFOUT_B21p	AU26	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK0n		DIFFIO_RX_B22n	DIFFOUT_B22n	AW25	DQSn8B	DQSn4B/DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK0p		DIFFIO_RX_B22p	DIFFOUT_B22p	AW24	DQS8B	DQS4B/CQ4B	DQ2B/CQn2B	DQ1B
3B	VREFB3BN0	IO		DATA22	DIFFIO_TX_B23n	DIFFOUT_B23n	AU23	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA23	DIFFIO_TX_B23p	DIFFOUT_B23p	AV24	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B24n	DIFFOUT_B24n	AV25	DQ8B	DQ4B	DQ2B	DQ1B

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B24p	DIFFOUT_B24p	AU25	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B25n	DIFFOUT_B25n	AF24	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B25p	DIFFOUT_B25p	AE24	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B26n	DIFFOUT_B26n	AD23	DQSn9B	DQ5B	DQSn2B/DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B26p	DIFFOUT_B26p	AE23	DQS9B	DQ5B/CQn5B	DQS2B/CQ2B	DQ1B
3B	VREFB3BN0	IO		DATA24	DIFFIO_TX_B27n	DIFFOUT_B27n	AG24	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA25	DIFFIO_TX_B27p	DIFFOUT_B27p	AH24	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK2n		DIFFIO_RX_B28n	DIFFOUT_B28n	AF22	DQSn10B	DQSn5B/DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK2p		DIFFIO_RX_B28p	DIFFOUT_B28p	AG22	DQS10B	DQS5B/CQ5B	DQ2B	DQ1B/CQn1B
3B	VREFB3BN0	IO		DATA26	DIFFIO_TX_B29n	DIFFOUT_B29n	AD22	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA27	DIFFIO_TX_B29p	DIFFOUT_B29p	AE22	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK3n		DIFFIO_RX_B30n	DIFFOUT_B30n	AG23	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK3p		DIFFIO_RX_B30p	DIFFOUT_B30p	AH23	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA28	DIFFIO_TX_B31n	DIFFOUT_B31n	AP26	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO		DATA29	DIFFIO_TX_B31p	DIFFOUT_B31p	AN26	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO		DATA30	DIFFIO_RX_B32n	DIFFOUT_B32n	AR25	DQSn11B	DQ6B	DQ3B	DQSn1B/DQ1B
3B	VREFB3BN0	IO		DATA31	DIFFIO_RX_B32p	DIFFOUT_B32p	AT25	DQS11B	DQ6B/CQn6B	DQ3B	DQS1B/CQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AT26	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AR26	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AR24	DQSn12B	DQSn6B/DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AP24	DQS12B	DQS6B/CQ6B	DQ3B/CQn3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AT23	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AR23	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AP23	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AN23	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AJ22	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AK22	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AJ23	DQSn13B	DQ7B	DQSn3B/DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AJ24	DQS13B	DQ7B/CQn7B	DQS3B/CQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AK23	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AL22	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AN25	DQSn14B	DQSn7B/DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AM25	DQS14B	DQS7B/CQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AL24	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AL23	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AM24	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AN24	DQ14B	DQ7B	DQ3B	DQ1B
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B85n	DIFFOUT_B85n	AL19	DQ29B	DQ8B		
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B85p	DIFFOUT_B85p	AL20	DQ29B	DQ8B		
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B86n	DIFFOUT_B86n	AN21	DQSn29B	DQ8B		
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B86p	DIFFOUT_B86p	AM21	DQS29B	DQ8B/CQn8B		
4C	VREFB4CN0	IO			DIFFIO_TX_B87n	DIFFOUT_B87n	AK19	DQ29B	DQ8B		
4C	VREFB4CN0	IO			DIFFIO_TX_B87p	DIFFOUT_B87p	AJ19	DQ29B	DQ8B		
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B88n	DIFFOUT_B88n	AP21	DQSn30B	DQSn8B/DQ8B		
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B88p	DIFFOUT_B88p	AR21	DQS30B	DQS8B/CQ8B		
4C	VREFB4CN0	IO			DIFFIO_TX_B89n	DIFFOUT_B89n	AN22	DQ30B	DQ8B		
4C	VREFB4CN0	IO			DIFFIO_TX_B89p	DIFFOUT_B89p	AM22	DQ30B	DQ8B		
4C	VREFB4CN0	IO	CLK7n		DIFFIO_RX_B90n	DIFFOUT_B90n	AN20	DQ30B	DQ8B		
4C	VREFB4CN0	IO	CLK7p		DIFFIO_RX_B90p	DIFFOUT_B90p	AP20	DQ30B	DQ8B		
4C	VREFB4CN0	IO			DIFFIO_RX_B91p	DIFFOUT_B91p	AG21	DQS31B	DQ9B/CQn9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B91n	DIFFOUT_B91n	AG20	DQSn31B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B92p	DIFFOUT_B92p	AH21	DQ31B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B92n	DIFFOUT_B92n	AJ21	DQ31B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B93p	DIFFOUT_B93p	AG19	DQS32B	DQS9B/CQ9B	DQ4B/CQn4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B93n	DIFFOUT_B93n	AH20	DQSn32B	DQSn9B/DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B94p	DIFFOUT_B94p	AE21	DQ31B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B94n	DIFFOUT_B94n	AF21	DQ31B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B95p	DIFFOUT_B95p	AE19	DQ32B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B95n	DIFFOUT_B95n	AF19	DQ32B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B96p	DIFFOUT_B96p	AE20	DQ32B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B96n	DIFFOUT_B96n	AD19	DQ32B	DQ9B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B97p	DIFFOUT_B97p	AT22	DQS33B	DQ10B/CQn10B	DQS4B/CQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B97n	DIFFOUT_B97n	AR22	DQSn33B	DQ10B	DQSn4B/DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B98p	DIFFOUT_B98p	AV22	DQ33B	DQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B98n	DIFFOUT_B98n	AW22	DQ33B	DQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AW21	DQS34B	DQS10B/CQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B99n	DIFFOUT_B99n	AV21	DQSn34B	DQSn10B/DQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AU22	DQ33B	DQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	AU21	DQ33B	DQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AR19	DQ34B	DQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	AR20	DQ34B	DQ10B	DQ4B	

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4C	VREFB4CN0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AU20	DQ34B	DQ10B	DQ4B	
4C	VREFB4CN0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	AT20	DQ34B	DQ10B	DQ4B	
4B	VREFB4BN0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AL17	DQS35B	DQ11B/CQn11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AL16	DQSn35B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AL18	DQ35B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B104n	DIFFOUT_B104n	AM18	DQ35B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B105p	DIFFOUT_B105p	AN18	DQS36B	DQS11B/CQ11B	DQ5B/CQn5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B105n	DIFFOUT_B105n	AP18	DQSn36B	DQSn11B/DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B106p	DIFFOUT_B106p	AN16	DQ35B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B106n	DIFFOUT_B106n	AN17	DQ35B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AN15	DQ36B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B107n	DIFFOUT_B107n	AN14	DQ36B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B108p	DIFFOUT_B108p	AM15	DQ36B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B108n	DIFFOUT_B108n	AM16	DQ36B	DQ11B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B109p	DIFFOUT_B109p	AP17	DQS37B	DQ12B/CQn12B	DQS5B/CQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B109n	DIFFOUT_B109n	AR17	DQSn37B	DQ12B	DQSn5B/DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B110p	DIFFOUT_B110p	AT19	DQ37B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B110n	DIFFOUT_B110n	AR18	DQ37B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B111p	DIFFOUT_B111p	AT16	DQS38B	DQS12B/CQ12B	DQ5B	DQ2B/CQn2B
4B	VREFB4BN0	IO			DIFFIO_RX_B111n	DIFFOUT_B111n	AT17	DQSn38B	DQSn12B/DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B112p	DIFFOUT_B112p	AU17	DQ37B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B112n	DIFFOUT_B112n	AV18	DQ37B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AV19	DQ38B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AU19	DQ38B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B114p	DIFFOUT_B114p	AW19	DQ38B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B114n	DIFFOUT_B114n	AW18	DQ38B	DQ12B	DQ5B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B115p	DIFFOUT_B115p	AK16	DQS39B	DQ13B/CQn13B	DQ6B	DQS2B/CQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B115n	DIFFOUT_B115n	AK17	DQSn39B	DQ13B	DQ6B	DQSn2B/DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B116p	DIFFOUT_B116p	AJ17	DQ39B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B116n	DIFFOUT_B116n	AJ18	DQ39B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B117p	DIFFOUT_B117p	AH17	DQS40B	DQS13B/CQ13B	DQ6B/CQn6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B117n	DIFFOUT_B117n	AJ16	DQSn40B	DQSn13B/DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B118p	DIFFOUT_B118p	AG17	DQ39B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B118n	DIFFOUT_B118n	AG18	DQ39B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B119p	DIFFOUT_B119p	AE18	DQ40B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B119n	DIFFOUT_B119n	AF18	DQ40B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B120p	DIFFOUT_B120p	AD17	DQ40B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B120n	DIFFOUT_B120n	AE17	DQ40B	DQ13B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B121p	DIFFOUT_B121p	AW15	DQS41B	DQ14B/CQn14B	DQS6B/CQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B121n	DIFFOUT_B121n	AW16	DQSn41B	DQ14B	DQSn6B/DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B122p	DIFFOUT_B122p	AV16	DQ41B	DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B122n	DIFFOUT_B122n	AU16	DQ41B	DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B123p	DIFFOUT_B123p	AV15	DQS42B	DQS14B/CQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B123n	DIFFOUT_B123n	AU15	DQSn42B	DQSn14B/DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B124p	DIFFOUT_B124p	AR15	DQ41B	DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B124n	DIFFOUT_B124n	AR16	DQ41B	DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B125p	DIFFOUT_B125p	AP14	DQ42B	DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_RX_B125n	DIFFOUT_B125n	AP15	DQ42B	DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B126p	DIFFOUT_B126p	AR14	DQ42B	DQ14B	DQ6B	DQ2B
4B	VREFB4BN0	IO			DIFFIO_TX_B126n	DIFFOUT_B126n	AT14	DQ42B	DQ14B	DQ6B	DQ2B
4A	VREFB4AN0	IO			DIFFIO_RX_B127p	DIFFOUT_B127p	AF15	DQS43B	DQ15B/CQn15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B127n	DIFFOUT_B127n	AE15	DQSn43B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B128p	DIFFOUT_B128p	AF16	DQ43B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B128n	DIFFOUT_B128n	AG16	DQ43B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B129p	DIFFOUT_B129p	AD16	DQS44B	DQS15B/CQ15B	DQ7B/CQn7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B129n	DIFFOUT_B129n	AE16	DQSn44B	DQSn15B/DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B130p	DIFFOUT_B130p	AE14	DQ43B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B130n	DIFFOUT_B130n	AD14	DQ43B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B131p	DIFFOUT_B131p	AF13	DQ44B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B131n	DIFFOUT_B131n	AG13	DQ44B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B132p	DIFFOUT_B132p	AC13	DQ44B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B132n	DIFFOUT_B132n	AD13	DQ44B	DQ15B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B133p	DIFFOUT_B133p	AH15	DQS45B	DQ16B/CQn16B	DQS7B/CQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B133n	DIFFOUT_B133n	AG15	DQSn45B	DQ16B	DQSn7B/DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B134p	DIFFOUT_B134p	AJ13	DQ45B	DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B134n	DIFFOUT_B134n	AK13	DQ45B	DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B135p	DIFFOUT_B135p	AH14	DQS46B	DQS16B/CQ16B	DQ7B	DQ3B/CQn3B
4A	VREFB4AN0	IO			DIFFIO_RX_B135n	DIFFOUT_B135n	AJ14	DQSn46B	DQSn16B/DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B136p	DIFFOUT_B136p	AL14	DQ45B	DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B136n	DIFFOUT_B136n	AL15	DQ45B	DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B137p	DIFFOUT_B137p	AK14	DQ46B	DQ16B	DQ7B	DQ3B

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4A	VREFB4AN0	IO			DIFFIO_RX_B137n	DIFFOUT_B137n	AJ15	DQ46B	DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B138p	DIFFOUT_B138p	AN12	DQ46B	DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B138n	DIFFOUT_B138n	AN13	DQ46B	DQ16B	DQ7B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B139n	DIFFOUT_B139n	AU14	DQ47B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B139p	DIFFOUT_B139p	AU13	DQ47B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B140n	DIFFOUT_B140n	AW13	DQSn47B	DQ17B	DQ8B	DQSn3B/DQ3B
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B140p	DIFFOUT_B140p	AV13	DQS47B	DQ17B/CQn17B	DQ8B	DQS3B/CQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B141n	DIFFOUT_B141n	AW12	DQ47B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B141p	DIFFOUT_B141p	AV12	DQ47B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B142n	DIFFOUT_B142n	AT13	DQSn48B	DQSn17B/DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B142p	DIFFOUT_B142p	AR13	DQS48B	DQS17B/CQ17B	DQ8B/CQn8B	DQ3B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B143n	DIFFOUT_B143n	AR11	DQ48B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B143p	DIFFOUT_B143p	AR12	DQ48B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B144n	DIFFOUT_B144n	AT11	DQ48B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B144p	DIFFOUT_B144p	AU11	DQ48B	DQ17B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B145n	DIFFOUT_B145n	AW9	DQ49B	DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B145p	DIFFOUT_B145p	AW10	DQ49B	DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B146n	DIFFOUT_B146n	AW7	DQSn49B	DQ18B	DQSn8B/DQ8B	DQ3B
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B146p	DIFFOUT_B146p	AV7	DQS49B	DQ18B/CQn18B	DQS8B/CQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B147n	DIFFOUT_B147n	AV10	DQ49B	DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B147p	DIFFOUT_B147p	AV9	DQ49B	DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B148n	DIFFOUT_B148n	AU9	DQSn50B	DQSn18B/DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B148p	DIFFOUT_B148p	AU10	DQS50B	DQS18B/CQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B149n	DIFFOUT_B149n	AT8	DQ50B	DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_TX_B149p	DIFFOUT_B149p	AU8	DQ50B	DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B150n	DIFFOUT_B150n	AT10	DQ50B	DQ18B	DQ8B	DQ3B
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_RX_B150p	DIFFOUT_B150p	AR10	DQ50B	DQ18B	DQ8B	DQ3B
4A		GND					AR9				
4A		nCE		nCE			AT7				
4A		nSTATUS		nSTATUS			AU7				
4A		CONF_DONE		CONF_DONE			AU6				
4A		nIO_PULLUP		nIO_PULLUP			AV6				
4A		MSEL0		MSEL0			AP11				
4A		MSEL1		MSEL1			AN11				
4A		MSEL2		MSEL2			AW6				
4A		MSEL3		MSEL3			AW5				
4A		MSEL4		MSEL4			AV5				
GXB_R0		REFCLK0Rn					AL9				
GXB_R0		REFCLK0Rp					AL10				
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AU2				
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AU1				
GXB_R0		GXB_TX_R0p					AR6				
GXB_R0		GXB_TX_R0n					AR5				
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AT4				
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AT3				
GXB_R0		GXB_TX_R1p					AP8				
GXB_R0		GXB_TX_R1n					AP7				
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AR2				
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AR1				
GXB_R0		GXB_TX_R2p					AN6				
GXB_R0		GXB_TX_R2n					AN5				
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AP4				
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AP3				
GXB_R0		GXB_TX_R3p					AM8				
GXB_R0		GXB_TX_R3n					AM7				
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					AN2				
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					AN1				
GXB_R0		GXB_TX_R4p					AL6				
GXB_R0		GXB_TX_R4n					AL5				
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					AM4				
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					AM3				
GXB_R0		GXB_TX_R5p					AK8				
GXB_R0		GXB_TX_R5n					AK7				
GXB_R0		REFCLK1Rn					AJ10				
GXB_R0		REFCLK1Rp					AJ11				
GXB_R1		REFCLK2Rn					AG9				
GXB_R1		REFCLK2Rp					AG10				
GXB_R1		GXB_RX_R6p,GXB_REFCLK_R6p					AL2				
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					AL1				
GXB_R1		GXB_TX_R6p					AJ6				
GXB_R1		GXB_TX_R6n					AJ5				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					AK4				
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					AK3				
GXB_R1		GXB_TX_R7p					AH8				
GXB_R1		GXB_TX_R7n					AH7				
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					AJ2				
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					AJ1				
GXB_R1		GXB_TX_R8p					AG6				
GXB_R1		GXB_TX_R8n					AG5				
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					AH4				
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					AH3				
GXB_R1		GXB_TX_R9p					AF8				
GXB_R1		GXB_TX_R9n					AF7				
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					AG2				
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					AG1				
GXB_R1		GXB_TX_R10p					AE6				
GXB_R1		GXB_TX_R10n					AE5				
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					AF4				
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					AF3				
GXB_R1		GXB_TX_R11p					AD8				
GXB_R1		GXB_TX_R11n					AD7				
GXB_R1		REFCLK3Rn					AE10				
GXB_R1		REFCLK3Rp					AE11				
GXB_R2		REFCLK4Rn					AC9				
GXB_R2		REFCLK4Rp					AC10				
GXB_R2		GXB_RX_R12p,GXB_REFCLK_R12p					AE2				
GXB_R2		GXB_RX_R12n,GXB_REFCLK_R12n					AE1				
GXB_R2		GXB_TX_R12p					AC6				
GXB_R2		GXB_TX_R12n					AC5				
GXB_R2		GXB_RX_R13p,GXB_REFCLK_R13p					AD4				
GXB_R2		GXB_RX_R13n,GXB_REFCLK_R13n					AD3				
GXB_R2		GXB_TX_R13p					AB8				
GXB_R2		GXB_TX_R13n					AB7				
GXB_R2		GXB_RX_R14p,GXB_REFCLK_R14p					AC2				
GXB_R2		GXB_RX_R14n,GXB_REFCLK_R14n					AC1				
GXB_R2		GXB_TX_R14p					AA6				
GXB_R2		GXB_TX_R14n					AA5				
GXB_R2		GXB_RX_R15p,GXB_REFCLK_R15p					AB4				
GXB_R2		GXB_RX_R15n,GXB_REFCLK_R15n					AB3				
GXB_R2		GXB_TX_R15p					Y4				
GXB_R2		GXB_TX_R15n					Y3				
GXB_R2		GXB_RX_R16p,GXB_REFCLK_R16p					AA2				
GXB_R2		GXB_RX_R16n,GXB_REFCLK_R16n					AA1				
GXB_R2		GXB_TX_R16p					Y8				
GXB_R2		GXB_TX_R16n					Y7				
GXB_R2		GXB_RX_R17p,GXB_REFCLK_R17p					W2				
GXB_R2		GXB_RX_R17n,GXB_REFCLK_R17n					W1				
GXB_R2		GXB_TX_R17p					W6				
GXB_R2		GXB_TX_R17n					W5				
GXB_R2		REFCLK5Rn					AA10				
GXB_R2		REFCLK5Rp					AA11				
GXB_R3		REFCLK6Rn					W9				
GXB_R3		REFCLK6Rp					W10				
GXB_R3		GXB_RX_R18p,GXB_REFCLK_R18p					V4				
GXB_R3		GXB_RX_R18n,GXB_REFCLK_R18n					V3				
GXB_R3		GXB_TX_R18p					V8				
GXB_R3		GXB_TX_R18n					V7				
GXB_R3		GXB_RX_R19p,GXB_REFCLK_R19p					U2				
GXB_R3		GXB_RX_R19n,GXB_REFCLK_R19n					U1				
GXB_R3		GXB_TX_R19p					U6				
GXB_R3		GXB_TX_R19n					U5				
GXB_R3		GXB_RX_R20p,GXB_REFCLK_R20p					T4				
GXB_R3		GXB_RX_R20n,GXB_REFCLK_R20n					T3				
GXB_R3		GXB_TX_R20p					T8				
GXB_R3		GXB_TX_R20n					T7				
GXB_R3		GXB_RX_R21p,GXB_REFCLK_R21p					R2				
GXB_R3		GXB_RX_R21n,GXB_REFCLK_R21n					R1				
GXB_R3		GXB_TX_R21p					R6				
GXB_R3		GXB_TX_R21n					R5				
GXB_R3		GXB_RX_R22p,GXB_REFCLK_R22p					N2				
GXB_R3		GXB_RX_R22n,GXB_REFCLK_R22n					N1				
GXB_R3		GXB_TX_R22p					P4				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_R3		GXB_TX_R22n					P3				
GXB_R3		GXB_RX_R23p,GXB_REFCLK_R23p					M4				
GXB_R3		GXB_RX_R23n,GXB_REFCLK_R23n					M3				
GXB_R3		GXB_TX_R23p					P8				
GXB_R3		GXB_TX_R23n					P7				
GXB_R3		REFCLK7Rn					U10				
GXB_R3		REFCLK7Rp					U11				
GXB_R4		REFCLK8Rn					R9				
GXB_R4		REFCLK8Rp					R10				
GXB_R4		GXB_RX_R24p,GXB_REFCLK_R24p					L2				
GXB_R4		GXB_RX_R24n,GXB_REFCLK_R24n					L1				
GXB_R4		GXB_TX_R24p					N6				
GXB_R4		GXB_TX_R24n					N5				
GXB_R4		GXB_RX_R25p,GXB_REFCLK_R25p					K4				
GXB_R4		GXB_RX_R25n,GXB_REFCLK_R25n					K3				
GXB_R4		GXB_TX_R25p					M8				
GXB_R4		GXB_TX_R25n					M7				
GXB_R4		GXB_RX_R26p,GXB_REFCLK_R26p					J2				
GXB_R4		GXB_RX_R26n,GXB_REFCLK_R26n					J1				
GXB_R4		GXB_TX_R26p					L6				
GXB_R4		GXB_TX_R26n					L5				
GXB_R4		GXB_RX_R27p,GXB_REFCLK_R27p					H4				
GXB_R4		GXB_RX_R27n,GXB_REFCLK_R27n					H3				
GXB_R4		GXB_TX_R27p					K8				
GXB_R4		GXB_TX_R27n					K7				
GXB_R4		GXB_RX_R28p,GXB_REFCLK_R28p					G2				
GXB_R4		GXB_RX_R28n,GXB_REFCLK_R28n					G1				
GXB_R4		GXB_TX_R28p					J6				
GXB_R4		GXB_TX_R28n					J5				
GXB_R4		GXB_RX_R29p,GXB_REFCLK_R29p					F4				
GXB_R4		GXB_RX_R29n,GXB_REFCLK_R29n					F3				
GXB_R4		GXB_TX_R29p					H8				
GXB_R4		GXB_TX_R29n					H7				
GXB_R4		REFCLK9Rn					N10				
GXB_R4		REFCLK9Rp					N11				
GXB_R5		REFCLK10Rn					L10				
GXB_R5		REFCLK10Rp					L11				
GXB_R5		GXB_RX_R30p,GXB_REFCLK_R30p					E2				
GXB_R5		GXB_RX_R30n,GXB_REFCLK_R30n					E1				
GXB_R5		GXB_TX_R30p					G6				
GXB_R5		GXB_TX_R30n					G5				
GXB_R5		GXB_RX_R31p,GXB_REFCLK_R31p					D4				
GXB_R5		GXB_RX_R31n,GXB_REFCLK_R31n					D3				
GXB_R5		GXB_TX_R31p					F8				
GXB_R5		GXB_TX_R31n					F7				
GXB_R5		GXB_RX_R32p,GXB_REFCLK_R32p					C2				
GXB_R5		GXB_RX_R32n,GXB_REFCLK_R32n					C1				
GXB_R5		GXB_TX_R32p					E6				
GXB_R5		GXB_TX_R32n					E5				
7A		GND					A5				
7A	VREFB7AN0	IO	RZQ_4		DIFFIO_RX_T1p	DIFFOUT_T1p	E10	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	D9	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	B6	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	C6	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T3p	DIFFOUT_T3p	D8	DQS1T	DQS1T/CQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T3n	DIFFOUT_T3n	C7	DQSn1T	DQSn1T/DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	B7	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	A7	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T5p	DIFFOUT_T5p	B9	DQS2T	DQ1T/CQn1T	DQS1T/CQ1T	DQ1T
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T5n	DIFFOUT_T5n	A9	DQSn2T	DQ1T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	C8	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	C9	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	E12	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	E11	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	A10	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	B10	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T9p	DIFFOUT_T9p	D11	DQS3T	DQS2T/CQ2T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T9n	DIFFOUT_T9n	C11	DQSn3T	DQSn2T/DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	G10	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	F10	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T11p	DIFFOUT_T11p	F13	DQS4T	DQ2T/CQn2T	DQ1T	DQS1T/CQ1T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T11n	DIFFOUT_T11n	E13	DQSn4T	DQ2T	DQ1T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	G11	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	F11	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T13n	DIFFOUT_T13n	G13	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T13p	DIFFOUT_T13p	G14	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	J13	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	H13	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T15n	DIFFOUT_T15n	G12	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T15p	DIFFOUT_T15p	H12	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	L14	DQSn5T	DQSn3T/DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	L13	DQS5T	DQS3T/CQ3T	DQ2T	DQ1T/CQn1T
7A	VREFB7AN0	IO			DIFFIO_TX_T17n	DIFFOUT_T17n	K15	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T17p	DIFFOUT_T17p	L15	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	K14	DQSn6T	DQ3T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T18p	DIFFOUT_T18p	J14	DQS6T	DQ3T/CQn3T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T19n	DIFFOUT_T19n	R14	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T19p	DIFFOUT_T19p	R15	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	M14	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	M13	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T21n	DIFFOUT_T21n	P13	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T21p	DIFFOUT_T21p	N13	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T22n	DIFFOUT_T22n	P16	DQSn7T	DQSn4T/DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	P15	DQS7T	DQS4T/CQ4T	DQ2T/CQn2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T23n	DIFFOUT_T23n	M16	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T23p	DIFFOUT_T23p	N16	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T24n	N14	DQSn8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T24p	N15	DQS8T	DQ4T/CQn4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T25n	DIFFOUT_T25n	C12	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T25p	DIFFOUT_T25p	D12	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	A12	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	B12	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T27n	DIFFOUT_T27n	A13	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T27p	DIFFOUT_T27p	B13	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	D14	DQSn9T	DQSn5T/DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T28p	DIFFOUT_T28p	C14	DQS9T	DQS5T/CQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T29n	DIFFOUT_T29n	B16	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T29p	DIFFOUT_T29p	A16	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	A15	DQSn10T	DQ5T	DQSn3T/DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	B15	DQS10T	DQ5T/CQn5T	DQS3T/CQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T31n	DIFFOUT_T31n	D15	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T31p	DIFFOUT_T31p	C15	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	E16	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	E15	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T33n	DIFFOUT_T33n	F14	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T33p	DIFFOUT_T33p	E14	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T34n	DIFFOUT_T34n	F16	DQSn11T	DQSn6T/DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T34p	DIFFOUT_T34p	F17	DQS11T	DQS6T/CQ6T	DQ3T/CQn3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T35n	DIFFOUT_T35n	E18	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T35p	DIFFOUT_T35p	E17	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	D17	DQSn12T	DQ6T	DQ3T	DQSn2T/DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T36p	DIFFOUT_T36p	D18	DQS12T	DQ6T/CQn6T	DQ3T	DQS2T/CQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T37n	DIFFOUT_T37n	G16	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T37p	DIFFOUT_T37p	G15	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	G18	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	G17	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T39n	DIFFOUT_T39n	H15	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T39p	DIFFOUT_T39p	H16	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	J19	DQSn13T	DQSn7T/DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	H19	DQS13T	DQS7T/CQ7T	DQ4T	DQ2T/CQn2T
7B	VREFB7BN0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	J18	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	H18	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	G19	DQSn14T	DQ7T	DQSn4T/DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	F19	DQS14T	DQ7T/CQn7T	DQS4T/CQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	J16	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	J15	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	M17	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	L17	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	K17	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	J17	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	N18	DQSn15T	DQSn8T/DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	N17	DQS15T	DQS8T/CQ8T	DQ4T/CQn4T	DQ2T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7B	VREFB7BN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	N19	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	M19	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	L19	DQSn16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	L18	DQS16T	DQ8T/CQn8T	DQ4T	DQ2T
7C	VREFB7CN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	N22	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	P21	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	L22	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	M22	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	N21	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	N20	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	L21	DQSn17T	DQSn9T/DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	K21	DQS17T	DQS9T/CQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	H21	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	J21	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	G22	DQSn18T	DQ9T	DQSn5T/DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	H22	DQS18T	DQ9T/CQn9T	DQS5T/CQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T55n	DIFFOUT_T55n	C17	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T55p	DIFFOUT_T55p	C18	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	C20	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	C19	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T57n	DIFFOUT_T57n	B19	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	B18	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	A19	DQSn19T	DQSn10T/DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	A18	DQS19T	DQS10T/CQ10T	DQ5T/CQn5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T59n	DIFFOUT_T59n	B22	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	B21	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T60n	DIFFOUT_T60n	A22	DQSn20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	A21	DQS20T	DQ10T/CQn10T	DQ5T	
7C	VREFB7CN0	IO	CLK19p		DIFFIO_RX_T61p	DIFFOUT_T61p	D21	DQ21T	DQ11T		
7C	VREFB7CN0	IO	CLK19n		DIFFIO_RX_T61n	DIFFOUT_T61n	D20	DQ21T	DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	E22	DQ21T	DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	E21	DQ21T	DQ11T		
7C	VREFB7CN0	IO	CLK18p		DIFFIO_RX_T63p	DIFFOUT_T63p	C22	DQS21T	DQS11T/CQ11T		
7C	VREFB7CN0	IO	CLK18n		DIFFIO_RX_T63n	DIFFOUT_T63n	C21	DQSn21T	DQSn11T/DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	F20	DQ22T	DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	G20	DQ22T	DQ11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T65p	DIFFOUT_T65p	E20	DQS22T	DQ11T/CQn11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T65n	DIFFOUT_T65n	E19	DQSn22T	DQ11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T66p	DIFFOUT_T66p	F22	DQ22T	DQ11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T66n	DIFFOUT_T66n	G21	DQ22T	DQ11T		
8B	VREFB8BN0	IO			DIFFIO_RX_T109p	DIFFOUT_T109p	G24	DQ37T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T109n	DIFFOUT_T109n	G23	DQ37T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T110p	DIFFOUT_T110p	H25	DQ37T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T110n	DIFFOUT_T110n	H24	DQ37T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T111p	DIFFOUT_T111p	G26	DQS37T	DQS12T/CQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T111n	DIFFOUT_T111n	G25	DQSn37T	DQSn12T/DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T112p	DIFFOUT_T112p	J23	DQ38T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T112n	DIFFOUT_T112n	K23	DQ38T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T113p	DIFFOUT_T113p	K24	DQS38T	DQ12T/CQn12T	DQS6T/CQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T113n	DIFFOUT_T113n	L24	DQSn38T	DQ12T	DQSn6T/DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T114p	DIFFOUT_T114p	J24	DQ38T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T114n	DIFFOUT_T114n	J25	DQ38T	DQ12T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T115p	DIFFOUT_T115p	E23	DQ39T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T115n	DIFFOUT_T115n	F23	DQ39T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T116p	DIFFOUT_T116p	E24	DQ39T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T116n	DIFFOUT_T116n	E25	DQ39T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T117p	DIFFOUT_T117p	D23	DQS39T	DQS13T/CQ13T	DQ6T/CQn6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T117n	DIFFOUT_T117n	D24	DQSn39T	DQSn13T/DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T118p	DIFFOUT_T118p	F26	DQ40T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T118n	DIFFOUT_T118n	F25	DQ40T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T119p	DIFFOUT_T119p	D26	DQS40T	DQ13T/CQn13T	DQ6T	DQS3T/CQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T119n	DIFFOUT_T119n	D27	DQSn40T	DQ13T	DQ6T	DQSn3T/DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T120p	DIFFOUT_T120p	E27	DQ40T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T120n	DIFFOUT_T120n	E26	DQ40T	DQ13T	DQ6T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T121p	DIFFOUT_T121p	L23	DQ41T	DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T121n	DIFFOUT_T121n	M23	DQ41T	DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T122p	DIFFOUT_T122p	N23	DQ41T	DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T122n	DIFFOUT_T122n	N24	DQ41T	DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T123p	DIFFOUT_T123p	R25	DQS41T	DQS14T/CQ14T	DQ7T	DQ3T/CQn3T
8B	VREFB8BN0	IO			DIFFIO_RX_T123n	DIFFOUT_T123n	P24	DQSn41T	DQSn14T/DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T124p	DIFFOUT_T124p	N25	DQ42T	DQ14T	DQ7T	DQ3T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8B	VREFB8BN0	IO			DIFFIO_TX_T124n	DIFFOUT_T124n	P25	DQ42T	DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T125p	DIFFOUT_T125p	M25	DQS42T	DQ14T/CQn14T	DQS7T/CQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T125n	DIFFOUT_T125n	M26	DQSn42T	DQ14T	DQSn7T/DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	L26	DQ42T	DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	K26	DQ42T	DQ14T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T127p	DIFFOUT_T127p	C26	DQ43T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T127n	DIFFOUT_T127n	C27	DQ43T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	C23	DQ43T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T128n	DIFFOUT_T128n	C24	DQ43T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T129p	DIFFOUT_T129p	B24	DQS43T	DQS15T/CQ15T	DQ7T/CQn7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T129n	DIFFOUT_T129n	B25	DQSn43T	DQSn15T/DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T130p	DIFFOUT_T130p	A24	DQ44T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T130n	DIFFOUT_T130n	A25	DQ44T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T131p	DIFFOUT_T131p	A27	DQS44T	DQ15T/CQn15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T131n	DIFFOUT_T131n	A28	DQSn44T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T132p	DIFFOUT_T132p	B27	DQ44T	DQ15T	DQ7T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_TX_T132n	DIFFOUT_T132n	B28	DQ44T	DQ15T	DQ7T	DQ3T
8A	VREFB8AN0	IO	CLK17p		DIFFIO_RX_T133p	DIFFOUT_T133p	G28	DQ45T	DQ16T	DQ8T	
8A	VREFB8AN0	IO	CLK17n		DIFFIO_RX_T133n	DIFFOUT_T133n	G27	DQ45T	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T134p	DIFFOUT_T134p	J27	DQ45T	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T134n	DIFFOUT_T134n	H27	DQ45T	DQ16T	DQ8T	
8A	VREFB8AN0	IO	CLK16p		DIFFIO_RX_T135p	DIFFOUT_T135p	F28	DQS45T	DQS16T/CQ16T	DQ8T	
8A	VREFB8AN0	IO	CLK16n		DIFFIO_RX_T135n	DIFFOUT_T135n	E28	DQSn45T	DQSn16T/DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T136p	DIFFOUT_T136p	L27	DQ46T	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T136n	DIFFOUT_T136n	K27	DQ46T	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T137p	DIFFOUT_T137p	R26	DQS46T	DQ16T/CQn16T	DQS8T/CQ8T	
8A	VREFB8AN0	IO			DIFFIO_RX_T137n	DIFFOUT_T137n	P27	DQSn46T	DQ16T	DQSn8T/DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T138p	DIFFOUT_T138p	N26	DQ46T	DQ16T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T138n	DIFFOUT_T138n	N27	DQ46T	DQ16T	DQ8T	
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T139p	DIFFOUT_T139p	C30	DQ47T	DQ17T	DQ8T	
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T139n	DIFFOUT_T139n	C29	DQ47T	DQ17T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T140p	DIFFOUT_T140p	A30	DQ47T	DQ17T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T140n	DIFFOUT_T140n	A31	DQ47T	DQ17T	DQ8T	
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T141p	DIFFOUT_T141p	B30	DQS47T	DQS17T/CQ17T	DQ8T/CQn8T	
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T141n	DIFFOUT_T141n	B31	DQSn47T	DQSn17T/DQ17T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T142p	DIFFOUT_T142p	E30	DQ48T	DQ17T	DQ8T	
8A	VREFB8AN0	IO			DIFFIO_TX_T142n	DIFFOUT_T142n	E29	DQ48T	DQ17T	DQ8T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T143p	DIFFOUT_T143p	D29	DQS48T	DQ17T/CQn17T	DQ8T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T143n	DIFFOUT_T143n	D30	DQSn48T	DQ17T	DQ8T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T144p	DIFFOUT_T144p	F29	DQ48T	DQ17T	DQ8T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T144n	DIFFOUT_T144n	G29	DQ48T	DQ17T	DQ8T	
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T145p	DIFFOUT_T145p	C31	DQ49T	DQ18T		
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T145n	DIFFOUT_T145n	C32	DQ49T	DQ18T		
8A	VREFB8AN0	IO			DIFFIO_TX_T146p	DIFFOUT_T146p	B33	DQ49T	DQ18T		
8A	VREFB8AN0	IO			DIFFIO_TX_T146n	DIFFOUT_T146n	A33	DQ49T	DQ18T		
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T147p	DIFFOUT_T147p	A34	DQS49T	DQS18T/CQ18T		
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T147n	DIFFOUT_T147n	A35	DQSn49T	DQSn18T/DQ18T		
8A	VREFB8AN0	IO			DIFFIO_TX_T148p	DIFFOUT_T148p	C34	DQ50T	DQ18T		
8A	VREFB8AN0	IO		nPERSTR0	DIFFIO_TX_T148n	DIFFOUT_T148n	B34	DQ50T	DQ18T		
8A	VREFB8AN0	IO		nPERSTR1	DIFFIO_RX_T149p	DIFFOUT_T149p	C33	DQS50T	DQ18T/CQn18T		
8A	VREFB8AN0	IO	RZQ_5		DIFFIO_RX_T149n	DIFFOUT_T149n	D32	DQSn50T	DQ18T		
8A	VREFB8AN0	IO		nPERSTL1	DIFFIO_TX_T150p	DIFFOUT_T150p	A36	DQ50T	DQ18T		
8A	VREFB8AN0	IO		nPERSTL0	DIFFIO_TX_T150n	DIFFOUT_T150n	B36	DQ50T	DQ18T		
		GND					A37				
		GND					AA32				
		GND					AA33				
		GND					AA36				
		GND					AA37				
		GND					AB28				
		GND					AB30				
		GND					AB34				
		GND					AB35				
		GND					AB38				
		GND					AB39				
		GND					AC32				
		GND					AC33				
		GND					AC36				
		GND					AC37				
		GND					AD29				
		GND					AD31				
		GND					AD34				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AD35				
		GND					AD38				
		GND					AD39				
		GND					AE28				
		GND					AE32				
		GND					AE33				
		GND					AE36				
		GND					AE37				
		GND					AF28				
		GND					AF30				
		GND					AF34				
		GND					AF35				
		GND					AF38				
		GND					AF39				
		GND					AG32				
		GND					AG33				
		GND					AG36				
		GND					AG37				
		GND					AH29				
		GND					AH31				
		GND					AH34				
		GND					AH35				
		GND					AH38				
		GND					AH39				
		GND					AJ28				
		GND					AJ32				
		GND					AJ33				
		GND					AJ36				
		GND					AJ37				
		GND					AK28				
		GND					AK30				
		GND					AK34				
		GND					AK35				
		GND					AK38				
		GND					AK39				
		GND					AL32				
		GND					AL33				
		GND					AL36				
		GND					AL37				
		GND					AM29				
		GND					AM31				
		GND					AM34				
		GND					AM35				
		GND					AM38				
		GND					AM39				
		GND					AN31				
		GND					AN32				
		GND					AN33				
		GND					AN36				
		GND					AN37				
		GND					AP31				
		GND					AP34				
		GND					AP35				
		GND					AP38				
		GND					AP39				
		GND					AR32				
		GND					AR33				
		GND					AR36				
		GND					AR37				
		GND					AT34				
		GND					AT35				
		GND					AT38				
		GND					AT39				
		GND					AU35				
		GND					AU36				
		GND					AU37				
		GND					AV37				
		GND					AV38				
		GND					AV39				
		GND					AW37				
		GND					B37				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					B38				
		GND					B39				
		GND					C36				
		GND					C37				
		GND					D34				
		GND					D35				
		GND					D38				
		GND					D39				
		GND					E32				
		GND					E33				
		GND					E36				
		GND					E37				
		GND					F31				
		GND					F34				
		GND					F35				
		GND					F38				
		GND					F39				
		GND					G32				
		GND					G33				
		GND					G36				
		GND					G37				
		GND					H34				
		GND					H35				
		GND					H38				
		GND					H39				
		GND					J29				
		GND					J32				
		GND					J33				
		GND					J36				
		GND					J37				
		GND					K28				
		GND					K29				
		GND					K34				
		GND					K35				
		GND					K38				
		GND					K39				
		GND					L28				
		GND					L31				
		GND					L32				
		GND					L33				
		GND					L36				
		GND					L37				
		GND					M29				
		GND					M31				
		GND					M34				
		GND					M35				
		GND					M38				
		GND					M39				
		GND					N32				
		GND					N33				
		GND					N36				
		GND					N37				
		GND					P30				
		GND					P34				
		GND					P35				
		GND					P38				
		GND					P39				
		GND					R32				
		GND					R33				
		GND					R36				
		GND					R37				
		GND					T29				
		GND					T31				
		GND					T34				
		GND					T35				
		GND					T38				
		GND					T39				
		GND					U32				
		GND					U33				
		GND					U36				
		GND					U37				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					V30				
		GND					V34				
		GND					V35				
		GND					V38				
		GND					V39				
		GND					W28				
		GND					W32				
		GND					W33				
		GND					W36				
		GND					W37				
		GND					Y29				
		GND					Y31				
		GND					Y34				
		GND					Y35				
		GND					Y38				
		GND					Y39				
		GND					A3				
		GND					AA3				
		GND					AA4				
		GND					AA7				
		GND					AA8				
		GND					AB1				
		GND					AB10				
		GND					AB12				
		GND					AB2				
		GND					AB5				
		GND					AB6				
		GND					AC3				
		GND					AC4				
		GND					AC7				
		GND					AC8				
		GND					AD1				
		GND					AD11				
		GND					AD2				
		GND					AD5				
		GND					AD6				
		GND					AD9				
		GND					AE12				
		GND					AE3				
		GND					AE4				
		GND					AE7				
		GND					AE8				
		GND					AF1				
		GND					AF10				
		GND					AF12				
		GND					AF2				
		GND					AF5				
		GND					AF6				
		GND					AG3				
		GND					AG4				
		GND					AG7				
		GND					AG8				
		GND					AH1				
		GND					AH11				
		GND					AH2				
		GND					AH5				
		GND					AH6				
		GND					AH9				
		GND					AJ12				
		GND					AJ3				
		GND					AJ4				
		GND					AJ7				
		GND					AJ8				
		GND					AK1				
		GND					AK10				
		GND					AK12				
		GND					AK2				
		GND					AK5				
		GND					AK6				
		GND					AL3				
		GND					AL4				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AL7				
		GND					AL8				
		GND					AM1				
		GND					AM11				
		GND					AM2				
		GND					AM5				
		GND					AM6				
		GND					AM9				
		GND					AN3				
		GND					AN4				
		GND					AN7				
		GND					AN8				
		GND					AN9				
		GND					AP1				
		GND					AP2				
		GND					AP5				
		GND					AP6				
		GND					AP9				
		GND					AR3				
		GND					AR4				
		GND					AR7				
		GND					AR8				
		GND					AT1				
		GND					AT2				
		GND					AT5				
		GND					AT6				
		GND					AU3				
		GND					AU4				
		GND					AU5				
		GND					AV1				
		GND					AV2				
		GND					AV3				
		GND					AW3				
		GND					B1				
		GND					B2				
		GND					B3				
		GND					C3				
		GND					C4				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					D6				
		GND					E3				
		GND					E4				
		GND					E7				
		GND					E8				
		GND					F1				
		GND					F2				
		GND					F5				
		GND					F6				
		GND					F9				
		GND					G3				
		GND					G4				
		GND					G7				
		GND					G8				
		GND					H1				
		GND					H2				
		GND					H5				
		GND					H6				
		GND					J11				
		GND					J3				
		GND					J4				
		GND					J7				
		GND					J8				
		GND					K1				
		GND					K11				
		GND					K12				
		GND					K2				
		GND					K5				
		GND					K6				
		GND					L12				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					L3				
		GND					L4				
		GND					L7				
		GND					L8				
		GND					L9				
		GND					M1				
		GND					M11				
		GND					M2				
		GND					M5				
		GND					M6				
		GND					M9				
		GND					N3				
		GND					N4				
		GND					N7				
		GND					N8				
		GND					P1				
		GND					P10				
		GND					P2				
		GND					P5				
		GND					P6				
		GND					R3				
		GND					R4				
		GND					R7				
		GND					R8				
		GND					T1				
		GND					T11				
		GND					T2				
		GND					T5				
		GND					T6				
		GND					T9				
		GND					U3				
		GND					U4				
		GND					U7				
		GND					U8				
		GND					V1				
		GND					V10				
		GND					V2				
		GND					V5				
		GND					V6				
		GND					W12				
		GND					W3				
		GND					W4				
		GND					W7				
		GND					W8				
		GND					Y1				
		GND					Y11				
		GND					Y2				
		GND					Y5				
		GND					Y6				
		GND					Y9				
		GND					AA13				
		GND					AA15				
		GND					AA19				
		GND					AA25				
		GND					AA27				
		GND					AB14				
		GND					AB16				
		GND					AB17				
		GND					AB18				
		GND					AB22				
		GND					AB24				
		GND					AB26				
		GND					AC12				
		GND					AC15				
		GND					AC20				
		GND					AC28				
		GND					AD12				
		GND					AD15				
		GND					AD18				
		GND					AD21				
		GND					AD24				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AD26				
		GND					AD28				
		GND					AF14				
		GND					AF17				
		GND					AF20				
		GND					AF23				
		GND					AF26				
		GND					AG12				
		GND					AG28				
		GND					AH12				
		GND					AH13				
		GND					AH16				
		GND					AH19				
		GND					AH22				
		GND					AH25				
		GND					AH28				
		GND					AK15				
		GND					AK18				
		GND					AK21				
		GND					AK24				
		GND					AK27				
		GND					AL12				
		GND					AL28				
		GND					AM12				
		GND					AM14				
		GND					AM17				
		GND					AM20				
		GND					AM23				
		GND					AM26				
		GND					AN10				
		GND					AN29				
		GND					AN30				
		GND					AP10				
		GND					AP13				
		GND					AP16				
		GND					AP19				
		GND					AP22				
		GND					AP25				
		GND					AP28				
		GND					AT12				
		GND					AT15				
		GND					AT18				
		GND					AT21				
		GND					AT24				
		GND					AT27				
		GND					AT30				
		GND					AT9				
		GND					AV11				
		GND					AV14				
		GND					AV17				
		GND					AV20				
		GND					AV23				
		GND					AV26				
		GND					AV29				
		GND					AV32				
		GND					AV8				
		GND					B11				
		GND					B14				
		GND					B17				
		GND					B20				
		GND					B23				
		GND					B26				
		GND					B29				
		GND					B32				
		GND					B35				
		GND					B5				
		GND					B8				
		GND					C35				
		GND					C5				
		GND					D10				
		GND					D13				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					D16				
		GND					D19				
		GND					D22				
		GND					D25				
		GND					D28				
		GND					D31				
		GND					D33				
		GND					D7				
		GND					E31				
		GND					E9				
		GND					F12				
		GND					F15				
		GND					F18				
		GND					F21				
		GND					F24				
		GND					F27				
		GND					F30				
		GND					G31				
		GND					G9				
		GND					H10				
		GND					H11				
		GND					H14				
		GND					H17				
		GND					H20				
		GND					H23				
		GND					H26				
		GND					H28				
		GND					H29				
		GND					H30				
		GND					H31				
		GND					H9				
		GND					K13				
		GND					K16				
		GND					K19				
		GND					K22				
		GND					K25				
		GND					M12				
		GND					M15				
		GND					M18				
		GND					M21				
		GND					M24				
		GND					M27				
		GND					M28				
		GND					P14				
		GND					P17				
		GND					P18				
		GND					P20				
		GND					P22				
		GND					P23				
		GND					P26				
		GND					R12				
		GND					R20				
		GND					R28				
		GND					T12				
		GND					T14				
		GND					T16				
		GND					T19				
		GND					T21				
		GND					T23				
		GND					T24				
		GND					T26				
		GND					T28				
		GND					U13				
		GND					U15				
		GND					U17				
		GND					U22				
		GND					U25				
		GND					U27				
		GND					V14				
		GND					V16				
		GND					V18				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					V20				
		GND					V24				
		GND					V26				
		GND					W13				
		GND					W15				
		GND					W17				
		GND					W19				
		GND					W23				
		GND					W25				
		GND					W27				
		GND					Y14				
		GND					Y16				
		GND					Y24				
		GND					Y26				
		GND					AA21				
		VCC					AC17				
		VCC					AC19				
		VCC					AC21				
		VCC					AC23				
		VCC					R17				
		VCC					R19				
		VCC					R21				
		VCC					R23				
		VCC					AA17				
		VCC					AA18				
		VCC					AA20				
		VCC					AA22				
		VCC					AA23				
		VCC					AB19				
		VCC					AB20				
		VCC					AB21				
		VCC					AB23				
		VCC					AC18				
		VCC					AC22				
		VCC					R18				
		VCC					R22				
		VCC					T17				
		VCC					T18				
		VCC					T20				
		VCC					T22				
		VCC					U18				
		VCC					U19				
		VCC					U20				
		VCC					U21				
		VCC					U23				
		VCC					V17				
		VCC					V19				
		VCC					V21				
		VCC					V22				
		VCC					V23				
		VCC					W18				
		VCC					W20				
		VCC					W21				
		VCC					W22				
		VCC					Y17				
		VCC					Y18				
		VCC					Y19				
		VCC					Y20				
		VCC					Y23				
		VCC					Y21				
		VCCPT					AD20				
		VCCPT					AE13				
		VCCPT					AE27				
		VCCPT					P19				
		VCCPT					R13				
		VCCPT					R27				
		DNU					AW36				
		DNU					AV36				
		DNU					AJ27				
		DNU					AN19				
		DNU					AV4				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		DNU					AW4				
		DNU					A6				
		DNU					J20				
		DNU					Y22				
		VCCPGM					AP29				
		VCCPGM					AP12				
		VCCPGM					G30				
		TEMPDIODEn					B4				
		TEMPDIODEp					A4				
		VCCBAT					AL13				
		VCCIO3A					AU30				
		VCCIO3A					AW32				
		VCCIO3B					AW26				
		VCCIO3B					AW29				
		VCCIO4A					AW11				
		VCCIO4A					AW8				
		VCCIO4B					AW14				
		VCCIO4B					AW17				
		VCCIO4C					AW20				
		VCCIO4C					AW23				
		VCCIO7A					A11				
		VCCIO7A					A8				
		VCCIO7B					A14				
		VCCIO7B					C16				
		VCCIO7C					A17				
		VCCIO7C					A20				
		VCCIO8A					A29				
		VCCIO8A					A32				
		VCCIO8B					A23				
		VCCIO8B					A26				
		VCCPD3AB					AU24				
		VCCPD3AB					AU27				
		VCCPD4					AU12				
		VCCPD4					AU18				
		VCCPD7					C10				
		VCCPD7					C13				
		VCCPD8					C25				
		VCCPD8					C28				
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AG26				
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AJ25				
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AG14				
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AH18				
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AL21				
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				L16				
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				K18				
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				J22				
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				J26				
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				L25				
		VCCH_GXBL0					AK31				
		VCCH_GXBL1					AF31				
		VCCH_GXBL2					AB31				
		VCCH_GXBL3					V31				
		VCCH_GXBL4					P31				
		VCCH_GXBL5					K31				
		VCCH_GXBR0					AK9				
		VCCH_GXBR1					AF9				
		VCCH_GXBR2					AB9				
		VCCH_GXBR3					V9				
		VCCH_GXBR4					P9				
		VCCH_GXBR5					K9				
		VCCR_GXBL0					AM30				
		VCCR_GXBL1					AH30				
		VCCR_GXBL2					AD30				
		VCCR_GXBL3					Y30				
		VCCR_GXBL4					T30				
		VCCR_GXBL5					M30				
		VCCR_GXBR0					AM10				
		VCCR_GXBR1					AH10				
		VCCR_GXBR2					AD10				
		VCCR_GXBR3					Y10				
		VCCR_GXBR4					T10				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCR_GXBR5					M10				
		VCCT_GXBL0					AK29				
		VCCT_GXBL0					AL29				
		VCCT_GXBL1					AF29				
		VCCT_GXBL1					AG29				
		VCCT_GXBL2					AB29				
		VCCT_GXBL2					AC29				
		VCCT_GXBL3					V29				
		VCCT_GXBL3					W29				
		VCCT_GXBL4					P29				
		VCCT_GXBL4					R29				
		VCCT_GXBL5					J30				
		VCCT_GXBL5					K30				
		VCCT_GXBR0					AK11				
		VCCT_GXBR0					AL11				
		VCCT_GXBR1					AF11				
		VCCT_GXBR1					AG11				
		VCCT_GXBR2					AB11				
		VCCT_GXBR2					AC11				
		VCCT_GXBR3					V11				
		VCCT_GXBR3					W11				
		VCCT_GXBR4					P11				
		VCCT_GXBR4					R11				
		VCCT_GXBR5					J10				
		VCCT_GXBR5					K10				
		VCCHIP_L					AA24				
		VCCHIP_L					AB25				
		VCCHIP_L					AC24				
		VCCHIP_L					R24				
		VCCHIP_L					T25				
		VCCHIP_L					U24				
		VCCHIP_L					V25				
		VCCHIP_L					W24				
		VCCHIP_L					Y25				
		VCCHIP_R					AA16				
		VCCHIP_R					AB15				
		VCCHIP_R					AC16				
		VCCHIP_R					R16				
		VCCHIP_R					T15				
		VCCHIP_R					U16				
		VCCHIP_R					V15				
		VCCHIP_R					W16				
		VCCHIP_R					Y15				
		RREF_BL					AW38				
		RREF_BR					AW2				
		RREF_TL					A38				
		RREF_TR					A2				
		VCCA_FPLL					AJ20				
		VCCA_FPLL					M20				
		VCCA_FPLL					AA28				
		VCCA_FPLL					N28				
		VCCA_FPLL					U28				
		VCCA_FPLL					AA12				
		VCCA_FPLL					N12				
		VCCA_FPLL					U12				
		VCCA_GXBL0					AJ31				
		VCCA_GXBL1					AE31				
		VCCA_GXBL2					AA31				
		VCCA_GXBL3					U31				
		VCCA_GXBL4					N31				
		VCCA_GXBL5					J31				
		VCCA_GXBR0					AJ9				
		VCCA_GXBR1					AE9				
		VCCA_GXBR2					AA9				
		VCCA_GXBR3					U9				
		VCCA_GXBR4					N9				
		VCCA_GXBR5					J9				
		VCCHSSI_L					AA26				
		VCCHSSI_L					AB27				
		VCCHSSI_L					AC26				
		VCCHSSI_L					T27				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCHSSI_L					U26				
		VCCHSSI_L					V27				
		VCCHSSI_L					W26				
		VCCHSSI_L					Y27				
		VCCHSSI_R					AA14				
		VCCHSSI_R					AB13				
		VCCHSSI_R					AC14				
		VCCHSSI_R					T13				
		VCCHSSI_R					U14				
		VCCHSSI_R					V13				
		VCCHSSI_R					W14				
		VCCHSSI_R					Y13				
		VCCD_FPLL					AK20				
		VCCD_FPLL					L20				
		VCCD_FPLL					P28				
		VCCD_FPLL					V28				
		VCCD_FPLL					Y28				
		VCCD_FPLL					P12				
		VCCD_FPLL					V12				
		VCCD_FPLL					Y12				
		VCC_AUX					AM19				
		VCC_AUX					AL27				
		VCC_AUX					AM13				
		VCC_AUX					K20				
		VCC_AUX					J28				
		VCC_AUX					J12				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the
Stratix V Device Family Pin Connection Guidelines.
(2) The GXB_REFCLK pin is not supported in the current Quartus II software version, but will be supported in the future Quartus II software release version.

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L5		GXB_TX_L32n					E38				
GXB_L5		GXB_TX_L32p					E37				
GXB_L5		GXB_RX_L32n,GXB_REFCLK_L32n					E42				
GXB_L5		GXB_RX_L32p,GXB_REFCLK_L32p					E41				
GXB_L5		GXB_TX_L31n					F36				
GXB_L5		GXB_TX_L31p					F35				
GXB_L5		GXB_RX_L31n,GXB_REFCLK_L31n					F40				
GXB_L5		GXB_RX_L31p,GXB_REFCLK_L31p					F39				
GXB_L5		GXB_TX_L30n					G38				
GXB_L5		GXB_TX_L30p					G37				
GXB_L5		GXB_RX_L30n,GXB_REFCLK_L30n					G42				
GXB_L5		GXB_RX_L30p,GXB_REFCLK_L30p					G41				
GXB_L5		REFCLK10Lp					N33				
GXB_L5		REFCLK10Ln					N32				
GXB_L4		REFCLK9Lp					R32				
GXB_L4		REFCLK9Ln					R33				
GXB_L4		GXB_TX_L29n					H36				
GXB_L4		GXB_TX_L29p					H35				
GXB_L4		GXB_RX_L29n,GXB_REFCLK_L29n					H40				
GXB_L4		GXB_RX_L29p,GXB_REFCLK_L29p					H39				
GXB_L4		GXB_TX_L28n					J38				
GXB_L4		GXB_TX_L28p					J37				
GXB_L4		GXB_RX_L28n,GXB_REFCLK_L28n					J42				
GXB_L4		GXB_RX_L28p,GXB_REFCLK_L28p					J41				
GXB_L4		GXB_TX_L27n					K36				
GXB_L4		GXB_TX_L27p					K35				
GXB_L4		GXB_RX_L27n,GXB_REFCLK_L27n					K40				
GXB_L4		GXB_RX_L27p,GXB_REFCLK_L27p					K39				
GXB_L4		GXB_TX_L26n					L38				
GXB_L4		GXB_TX_L26p					L37				
GXB_L4		GXB_RX_L26n,GXB_REFCLK_L26n					L42				
GXB_L4		GXB_RX_L26p,GXB_REFCLK_L26p					L41				
GXB_L4		GXB_TX_L25n					M36				
GXB_L4		GXB_TX_L25p					M35				
GXB_L4		GXB_RX_L25n,GXB_REFCLK_L25n					M40				
GXB_L4		GXB_RX_L25p,GXB_REFCLK_L25p					M39				
GXB_L4		GXB_TX_L24n					N38				
GXB_L4		GXB_TX_L24p					N37				
GXB_L4		GXB_RX_L24n,GXB_REFCLK_L24n					N42				
GXB_L4		GXB_RX_L24p,GXB_REFCLK_L24p					N41				
GXB_L4		REFCLK8Lp					U33				
GXB_L4		REFCLK8Ln					U34				
GXB_L3		REFCLK7Lp					W32				
GXB_L3		REFCLK7Ln					W33				
GXB_L3		GXB_TX_L23n					P36				
GXB_L3		GXB_TX_L23p					P35				
GXB_L3		GXB_RX_L23n,GXB_REFCLK_L23n					P40				
GXB_L3		GXB_RX_L23p,GXB_REFCLK_L23p					P39				
GXB_L3		GXB_TX_L22n					R38				
GXB_L3		GXB_TX_L22p					R37				
GXB_L3		GXB_RX_L22n,GXB_REFCLK_L22n					R42				
GXB_L3		GXB_RX_L22p,GXB_REFCLK_L22p					R41				
GXB_L3		GXB_TX_L21n					T36				
GXB_L3		GXB_TX_L21p					T35				
GXB_L3		GXB_RX_L21n,GXB_REFCLK_L21n					T40				
GXB_L3		GXB_RX_L21p,GXB_REFCLK_L21p					T39				
GXB_L3		GXB_TX_L20n					U38				
GXB_L3		GXB_TX_L20p					U37				
GXB_L3		GXB_RX_L20n,GXB_REFCLK_L20n					U42				
GXB_L3		GXB_RX_L20p,GXB_REFCLK_L20p					U41				
GXB_L3		GXB_TX_L19n					V36				
GXB_L3		GXB_TX_L19p					V35				
GXB_L3		GXB_RX_L19n,GXB_REFCLK_L19n					V40				
GXB_L3		GXB_RX_L19p,GXB_REFCLK_L19p					V39				
GXB_L3		GXB_TX_L18n					W38				
GXB_L3		GXB_TX_L18p					W37				
GXB_L3		GXB_RX_L18n,GXB_REFCLK_L18n					W42				
GXB_L3		GXB_RX_L18p,GXB_REFCLK_L18p					W41				
GXB_L3		REFCLK6Lp					AA33				
GXB_L3		REFCLK6Ln					AA34				
GXB_L2		REFCLK5Lp					AC32				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L2		REFCLK5Ln					AC33				
GXB_L2		GXB_TX_L17n					Y36				
GXB_L2		GXB_TX_L17p					Y35				
GXB_L2		GXB_RX_L17n,GXB_REFCLK_L17n					Y40				
GXB_L2		GXB_RX_L17p,GXB_REFCLK_L17p					Y39				
GXB_L2		GXB_TX_L16n					AA38				
GXB_L2		GXB_TX_L16p					AA37				
GXB_L2		GXB_RX_L16n,GXB_REFCLK_L16n					AA42				
GXB_L2		GXB_RX_L16p,GXB_REFCLK_L16p					AA41				
GXB_L2		GXB_TX_L15n					AB36				
GXB_L2		GXB_TX_L15p					AB35				
GXB_L2		GXB_RX_L15n,GXB_REFCLK_L15n					AB40				
GXB_L2		GXB_RX_L15p,GXB_REFCLK_L15p					AB39				
GXB_L2		GXB_TX_L14n					AC38				
GXB_L2		GXB_TX_L14p					AC37				
GXB_L2		GXB_RX_L14n,GXB_REFCLK_L14n					AC42				
GXB_L2		GXB_RX_L14p,GXB_REFCLK_L14p					AC41				
GXB_L2		GXB_TX_L13n					AD36				
GXB_L2		GXB_TX_L13p					AD35				
GXB_L2		GXB_RX_L13n,GXB_REFCLK_L13n					AD40				
GXB_L2		GXB_RX_L13p,GXB_REFCLK_L13p					AD39				
GXB_L2		GXB_TX_L12n					AE38				
GXB_L2		GXB_TX_L12p					AE37				
GXB_L2		GXB_RX_L12n,GXB_REFCLK_L12n					AE42				
GXB_L2		GXB_RX_L12p,GXB_REFCLK_L12p					AE41				
GXB_L2		REFCLK4Lp					AE33				
GXB_L2		REFCLK4Ln					AE34				
GXB_L1		REFCLK3Lp					AG32				
GXB_L1		REFCLK3Ln					AG33				
GXB_L1		GXB_TX_L11n					AF36				
GXB_L1		GXB_TX_L11p					AF35				
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					AF40				
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					AF39				
GXB_L1		GXB_TX_L10n					AG38				
GXB_L1		GXB_TX_L10p					AG37				
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					AG42				
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					AG41				
GXB_L1		GXB_TX_L9n					AH36				
GXB_L1		GXB_TX_L9p					AH35				
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					AH40				
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					AH39				
GXB_L1		GXB_TX_L8n					AJ38				
GXB_L1		GXB_TX_L8p					AJ37				
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					AJ42				
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					AJ41				
GXB_L1		GXB_TX_L7n					AK36				
GXB_L1		GXB_TX_L7p					AK35				
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					AK40				
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					AK39				
GXB_L1		GXB_TX_L6n					AL38				
GXB_L1		GXB_TX_L6p					AL37				
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					AL42				
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					AL41				
GXB_L1		REFCLK2Lp					AJ33				
GXB_L1		REFCLK2Ln					AJ34				
GXB_L0		REFCLK1Lp					AL32				
GXB_L0		REFCLK1Ln					AL33				
GXB_L0		GXB_TX_L5n					AM36				
GXB_L0		GXB_TX_L5p					AM35				
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					AM40				
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					AM39				
GXB_L0		GXB_TX_L4n					AN38				
GXB_L0		GXB_TX_L4p					AN37				
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AN42				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AN41				
GXB_L0		GXB_TX_L3n					AP36				
GXB_L0		GXB_TX_L3p					AP35				
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AP40				
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AP39				
GXB_L0		GXB_TX_L2n					AR38				
GXB_L0		GXB_TX_L2p					AR37				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AR42				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AR41				
GXB_L0		GXB_TX_L1n					AT36				
GXB_L0		GXB_TX_L1p					AT35				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AT40				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AT39				
GXB_L0		GXB_TX_L0n					AU38				
GXB_L0		GXB_TX_L0p					AU37				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AU42				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AU41				
GXB_L0		REFCLK0Lp					AN33				
GXB_L0		REFCLK0Ln					AN34				
3A		nCONFIG		nCONFIG			AU34				
3A		TRST		TRST			AU32				
3A		TMS		TMS			AT32				
3A		TCK		TCK			AR31				
3A		TDI		TDI			AP30				
3A		TDO		TDO			AG30				
3A		nCSO		nCSO			AU33				
3A		AS_DATA3		AS_DATA3			AV33				
3A		AS_DATA2		AS_DATA2			AT31				
3A		AS_DATA1		AS_DATA1			AT30				
3A		AS_DATA0,ASDO		AS_DATA0,ASDO			AT33				
3A		DCLK		DCLK			AH30				
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_TX_B1n	DIFFOUT_B1n	AW37	DQ1B	DQ1B		
3A	VREFB3AN0	IO		CRC_ERROR	DIFFIO_TX_B1p	DIFFOUT_B1p	AW36	DQ1B	DQ1B		
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_RX_B2n	DIFFOUT_B2n	AW35	DQSn1B	DQ1B		
3A	VREFB3AN0	IO		DEV_OE	DIFFIO_RX_B2p	DIFFOUT_B2p	AV35	DQS1B	DQ1B/CQn1B		
3A	VREFB3AN0	IO		DEV_CLRn	DIFFIO_TX_B3n	DIFFOUT_B3n	AY37	DQ1B	DQ1B		
3A	VREFB3AN0	IO		INIT_DONE	DIFFIO_TX_B3p	DIFFOUT_B3p	AY36	DQ1B	DQ1B		
3A	VREFB3AN0	IO		nCEO	DIFFIO_RX_B4n	DIFFOUT_B4n	AY33	DQSn2B	DQSn1B/DQ1B		
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B4p	DIFFOUT_B4p	AW34	DQS2B	DQS1B/CQ1B		
3A	VREFB3AN0	IO		PR_REQUEST	DIFFIO_TX_B5n	DIFFOUT_B5n	AW33	DQ2B	DQ1B		
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B5p	DIFFOUT_B5p	AV32	DQ2B	DQ1B		
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B6n	DIFFOUT_B6n	AW31	DQ2B	DQ1B		
3A	VREFB3AN0	IO		CvP_CONFDONE	DIFFIO_RX_B6p	DIFFOUT_B6p	AV31	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B7n	DIFFOUT_B7n	AW39	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B7p	DIFFOUT_B7p	AW38	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA0	DIFFIO_RX_B8n	DIFFOUT_B8n	AY40	DQSn3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA1	DIFFIO_RX_B8p	DIFFOUT_B8p	AW40	DQS3B	DQ2B/CQn2B	DQ1B	
3A	VREFB3AN0	IO		DATA2	DIFFIO_TX_B9n	DIFFOUT_B9n	AY39	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA3	DIFFIO_TX_B9p	DIFFOUT_B9p	AY38	DQ3B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA4	DIFFIO_RX_B10n	DIFFOUT_B10n	BB41	DQSn4B	DQSn2B/DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA5	DIFFIO_RX_B10p	DIFFOUT_B10p	BB40	DQS4B	DQS2B/CQ2B	DQ1B/CQn1B	
3A	VREFB3AN0	IO		DATA6	DIFFIO_TX_B11n	DIFFOUT_B11n	BB39	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B11p	DIFFOUT_B11p	BB38	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B12n	DIFFOUT_B12n	BB37	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA9	DIFFIO_RX_B12p	DIFFOUT_B12p	BB36	DQ4B	DQ2B	DQ1B	
3A	VREFB3AN0	IO		DATA10	DIFFIO_TX_B13n	DIFFOUT_B13n	AH29	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B13p	DIFFOUT_B13p	AH28	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B14n	DIFFOUT_B14n	AM29	DQSn5B	DQ3B	DQSn1B/DQ1B	
3A	VREFB3AN0	IO		DATA13	DIFFIO_RX_B14p	DIFFOUT_B14p	AL29	DQS5B	DQ3B/CQn3B	DQS1B/CQ1B	
3A	VREFB3AN0	IO		DATA14	DIFFIO_TX_B15n	DIFFOUT_B15n	AK29	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B15p	DIFFOUT_B15p	AJ29	DQ5B	DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B16n	AT29	DQSn6B	DQSn3B/DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B16p	AR29	DQS6B	DQS3B/CQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AP29	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AP28	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK5n		DIFFIO_RX_B18n	DIFFOUT_B18n	AV30	DQ6B	DQ3B	DQ1B	
3A	VREFB3AN0	IO	CLK5p		DIFFIO_RX_B18p	DIFFOUT_B18p	AU30	DQ6B	DQ3B	DQ1B	
3B	VREFB3BN0	IO		DATA16	DIFFIO_TX_B19n	DIFFOUT_B19n	AR26	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA17	DIFFIO_TX_B19p	DIFFOUT_B19p	AP26	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA18	DIFFIO_RX_B20n	DIFFOUT_B20n	AU29	DQSn7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA19	DIFFIO_RX_B20p	DIFFOUT_B20p	AT28	DQS7B	DQ4B/CQn4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA20	DIFFIO_TX_B21n	DIFFOUT_B21n	AU27	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA21	DIFFIO_TX_B21p	DIFFOUT_B21p	AT27	DQ7B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK0n		DIFFIO_RX_B22n	DIFFOUT_B22n	AN28	DQSn8B	DQSn4B/DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK0p		DIFFIO_RX_B22p	DIFFOUT_B22p	AM28	DQS8B	DQS4B/CQ4B	DQ2B/CQn2B	DQ1B
3B	VREFB3BN0	IO		DATA22	DIFFIO_TX_B23n	DIFFOUT_B23n	AM27	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA23	DIFFIO_TX_B23p	DIFFOUT_B23p	AM26	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B24n	DIFFOUT_B24n	AR28	DQ8B	DQ4B	DQ2B	DQ1B

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B24p	DIFFOUT_B24p	AP27	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B25n	DIFFOUT_B25n	AK28	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B25p	DIFFOUT_B25p	AJ28	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B26n	DIFFOUT_B26n	AH27	DQSn9B	DQ5B	DQSn2B/DQ2B	DQ1B
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B26p	DIFFOUT_B26p	AG27	DQS9B	DQ5B/CQn5B	DQS2B/CQ2B	DQ1B
3B	VREFB3BN0	IO		DATA24	DIFFIO_TX_B27n	DIFFOUT_B27n	AG28	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA25	DIFFIO_TX_B27p	DIFFOUT_B27p	AF28	DQ9B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK2n		DIFFIO_RX_B28n	DIFFOUT_B28n	AL27	DQSn10B	DQSn5B/DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK2p		DIFFIO_RX_B28p	DIFFOUT_B28p	AK27	DQS10B	DQS5B/CQ5B	DQ2B	DQ1B/CQn1B
3B	VREFB3BN0	IO		DATA26	DIFFIO_TX_B29n	DIFFOUT_B29n	AJ26	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA27	DIFFIO_TX_B29p	DIFFOUT_B29p	AH26	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK3n		DIFFIO_RX_B30n	DIFFOUT_B30n	AL26	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO	CLK3p		DIFFIO_RX_B30p	DIFFOUT_B30p	AK26	DQ10B	DQ5B	DQ2B	DQ1B
3B	VREFB3BN0	IO		DATA28	DIFFIO_TX_B31n	DIFFOUT_B31n	AW30	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO		DATA29	DIFFIO_TX_B31p	DIFFOUT_B31p	AV29	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO		DATA30	DIFFIO_RX_B32n	DIFFOUT_B32n	AY31	DQSn11B	DQ6B	DQ3B	DQSn1B/DQ1B
3B	VREFB3BN0	IO		DATA31	DIFFIO_RX_B32p	DIFFOUT_B32p	AY30	DQS11B	DQ6B/CQn6B	DQ3B	DQS1B/CQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	BB31	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	BA31	DQ11B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	BA34	DQSn12B	DQSn6B/DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AY34	DQS12B	DQS6B/CQ6B	DQ3B/CQn3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	BB32	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	BA32	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	BB35	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	BB34	DQ12B	DQ6B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AY28	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AW28	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AV28	DQSn13B	DQ7B	DQSn3B/DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AV27	DQS13B	DQ7B/CQn7B	DQS3B/CQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AY27	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AW27	DQ13B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	BB29	DQSn14B	DQSn7B/DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	BA29	DQS14B	DQS7B/CQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	BB28	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	BA28	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	BB26	DQ14B	DQ7B	DQ3B	DQ1B
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	BB25	DQ14B	DQ7B	DQ3B	DQ1B
3C	VREFB3CN0	IO			DIFFIO_TX_B43n	DIFFOUT_B43n	AD29	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AC29	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AF29	DQSn15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AE28	DQS15B	DQ8B/CQn8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AC27	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AD28	DQ15B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AF27	DQSn16B	DQSn8B/DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AF26	DQS16B	DQS8B/CQ8B	DQ4B/CQn4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	AE26	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AD25	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AD27	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AD26	DQ16B	DQ8B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AM25	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AM24	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AM23	DQSn17B	DQ9B	DQSn4B/DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AL23	DQS17B	DQ9B/CQn9B	DQS4B/CQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AL24	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AK24	DQ17B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AR25	DQSn18B	DQSn9B/DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AP25	DQS18B	DQS9B/CQ9B	DQ4B	DQ2B/CQn2B
3C	VREFB3CN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AT26	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AT25	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AP24	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AN25	DQ18B	DQ9B	DQ4B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B55n	DIFFOUT_B55n	AV26	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B55p	DIFFOUT_B55p	AU26	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B56n	DIFFOUT_B56n	AU24	DQSn19B	DQ10B	DQ5B	DQSn2B/DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B56p	DIFFOUT_B56p	AT24	DQS19B	DQ10B/CQn10B	DQ5B	DQS2B/CQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AV25	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AV24	DQ19B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	BA26	DQSn20B	DQSn10B/DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	BA25	DQS20B	DQS10B/CQ10B	DQ5B/CQn5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B59n	DIFFOUT_B59n	AY25	DQ20B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B59p	DIFFOUT_B59p	AW25	DQ20B	DQ10B	DQ5B	DQ2B

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
3C	VREFB3CN0	IO			DIFFIO_RX_B60n	DIFFOUT_B60n	AY24	DQ20B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B60p	DIFFOUT_B60p	AW24	DQ20B	DQ10B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AH25	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AG25	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AK25	DQSn21B	DQ11B	DQSn5B/DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AJ25	DQS21B	DQ11B/CQn11B	DQS5B/CQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B63n	DIFFOUT_B63n	AF25	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B63p	DIFFOUT_B63p	AF24	DQ21B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B64n	DIFFOUT_B64n	AK23	DQSn22B	DQSn11B/DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B64p	DIFFOUT_B64p	AJ23	DQS22B	DQS11B/CQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AF23	DQ22B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AF22	DQ22B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AH24	DQ22B	DQ11B	DQ5B	DQ2B
3C	VREFB3CN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AG24	DQ22B	DQ11B	DQ5B	DQ2B
3D	VREFB3DN0	IO			DIFFIO_TX_B67n	DIFFOUT_B67n	AT23	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B67p	DIFFOUT_B67p	AR23	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B68n	DIFFOUT_B68n	AU21	DQSn23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B68p	DIFFOUT_B68p	AT21	DQS23B	DQ12B/CQn12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AT22	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AR22	DQ23B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AP22	DQSn24B	DQSn12B/DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AP23	DQS24B	DQS12B/CQ12B	DQ6B/CQn6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B71n	DIFFOUT_B71n	AM21	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B71p	DIFFOUT_B71p	AM22	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B72n	DIFFOUT_B72n	AP21	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B72p	DIFFOUT_B72p	AN22	DQ24B	DQ12B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	BB23	DQ25B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	BA23	DQ25B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AY22	DQSn25B	DQ13B	DQSn6B/DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AY21	DQS25B	DQ13B/CQn13B	DQS6B/CQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B75n	DIFFOUT_B75n	BB22	DQ25B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B75p	DIFFOUT_B75p	BA22	DQ25B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B76n	DIFFOUT_B76n	AV23	DQSn26B	DQSn13B/DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B76p	DIFFOUT_B76p	AU23	DQS26B	DQS13B/CQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AW21	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AV21	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AW22	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AV22	DQ26B	DQ13B	DQ6B	
3D	VREFB3DN0	IO			DIFFIO_TX_B79n	DIFFOUT_B79n	AG22	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B79p	DIFFOUT_B79p	AH23	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B80n	DIFFOUT_B80n	AH22	DQSn27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B80p	DIFFOUT_B80p	AH21	DQS27B	DQ14B/CQn14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AG21	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AF20	DQ27B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B82n	DIFFOUT_B82n	AL21	DQSn28B	DQSn14B/DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B82p	DIFFOUT_B82p	AK21	DQS28B	DQS14B/CQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B83n	DIFFOUT_B83n	AJ20	DQ28B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_TX_B83p	DIFFOUT_B83p	AH20	DQ28B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B84n	DIFFOUT_B84n	AL20	DQ28B	DQ14B		
3D	VREFB3DN0	IO			DIFFIO_RX_B84p	DIFFOUT_B84p	AK20	DQ28B	DQ14B		
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B85n	DIFFOUT_B85n	AG19	DQ29B	DQ15B		
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B85p	DIFFOUT_B85p	AF19	DQ29B	DQ15B		
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B86n	DIFFOUT_B86n	AJ19	DQSn29B	DQ15B		
4C	VREFB4CN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B86p	DIFFOUT_B86p	AH19	DQS29B	DQ15B/CQn15B		
4C	VREFB4CN0	IO			DIFFIO_TX_B87n	DIFFOUT_B87n	AK19	DQ29B	DQ15B		
4C	VREFB4CN0	IO			DIFFIO_TX_B87p	DIFFOUT_B87p	AK18	DQ29B	DQ15B		
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B88n	DIFFOUT_B88n	AM18	DQSn30B	DQSn15B/DQ15B		
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B88p	DIFFOUT_B88p	AL18	DQS30B	DQS15B/CQ15B		
4C	VREFB4CN0	IO			DIFFIO_TX_B89n	DIFFOUT_B89n	AN18	DQ30B	DQ15B		
4C	VREFB4CN0	IO			DIFFIO_TX_B89p	DIFFOUT_B89p	AM19	DQ30B	DQ15B		
4C	VREFB4CN0	IO	CLK7n		DIFFIO_RX_B90n	DIFFOUT_B90n	AP19	DQ30B	DQ15B		
4C	VREFB4CN0	IO	CLK7p		DIFFIO_RX_B90p	DIFFOUT_B90p	AP18	DQ30B	DQ15B		
4C	VREFB4CN0	IO			DIFFIO_RX_B91p	DIFFOUT_B91p	AR19	DQS31B	DQ16B/CQn16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B91n	DIFFOUT_B91n	AT19	DQSn31B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B92p	DIFFOUT_B92p	AR20	DQ31B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B92n	DIFFOUT_B92n	AT20	DQ31B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B93p	DIFFOUT_B93p	AU20	DQS32B	DQS16B/CQ16B	DQ7B/CQn7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B93n	DIFFOUT_B93n	AV20	DQSn32B	DQSn16B/DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B94p	DIFFOUT_B94p	AW18	DQ31B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B94n	DIFFOUT_B94n	AW19	DQ31B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B95p	DIFFOUT_B95p	AV18	DQ32B	DQ16B	DQ7B	

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4C	VREFB4CN0	IO			DIFFIO_RX_B95n	DIFFOUT_B95n	AV19	DQ32B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B96p	DIFFOUT_B96p	AT18	DQ32B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B96n	DIFFOUT_B96n	AU18	DQ32B	DQ16B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B97p	DIFFOUT_B97p	AY20	DQS33B	DQ17B/CQn17B	DQS7B/CQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B97n	DIFFOUT_B97n	BA20	DQSn33B	DQ17B	DQSn7B/DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B98p	DIFFOUT_B98p	BB19	DQ33B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B98n	DIFFOUT_B98n	BB20	DQ33B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AY19	DQS34B	DQS17B/CQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B99n	DIFFOUT_B99n	BA19	DQSn34B	DQSn17B/DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	BB16	DQ33B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	BB17	DQ33B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AY18	DQ34B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	BA17	DQ34B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AY16	DQ34B	DQ17B	DQ7B	
4C	VREFB4CN0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	BA16	DQ34B	DQ17B	DQ7B	
4B	VREFB4BN0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AC17	DQS35B	DQ18B/CQn18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AD17	DQSn35B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AF18	DQ35B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B104n	DIFFOUT_B104n	AG18	DQ35B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B105p	DIFFOUT_B105p	AE17	DQS36B	DQS18B/CQ18B	DQ8B/CQn8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B105n	DIFFOUT_B105n	AF17	DQSn36B	DQSn18B/DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B106p	DIFFOUT_B106p	AH18	DQ35B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B106n	DIFFOUT_B106n	AH17	DQ35B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AG16	DQ36B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B107n	DIFFOUT_B107n	AH16	DQ36B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B108p	DIFFOUT_B108p	AG15	DQ36B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B108n	DIFFOUT_B108n	AF16	DQ36B	DQ18B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B109p	DIFFOUT_B109p	AV15	DQS37B	DQ19B/CQn19B	DQS8B/CQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B109n	DIFFOUT_B109n	AV16	DQSn37B	DQ19B	DQSn8B/DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B110p	DIFFOUT_B110p	AV17	DQ37B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B110n	DIFFOUT_B110n	AW16	DQ37B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B111p	DIFFOUT_B111p	AT17	DQS38B	DQS19B/CQ19B	DQ8B	DQ3B/CQn3B
4B	VREFB4BN0	IO			DIFFIO_RX_B111n	DIFFOUT_B111n	AU17	DQSn38B	DQSn19B/DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B112p	DIFFOUT_B112p	AT15	DQ37B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B112n	DIFFOUT_B112n	AU15	DQ37B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AR16	DQ38B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AT16	DQ38B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B114p	DIFFOUT_B114p	AP17	DQ38B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B114n	DIFFOUT_B114n	AR17	DQ38B	DQ19B	DQ8B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B115p	DIFFOUT_B115p	AL17	DQS39B	DQ20B/CQn20B	DQ9B	DQS3B/CQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B115n	DIFFOUT_B115n	AM17	DQSn39B	DQ20B	DQ9B	DQSn3B/DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B116p	DIFFOUT_B116p	AJ17	DQ39B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B116n	DIFFOUT_B116n	AK17	DQ39B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B117p	DIFFOUT_B117p	AJ16	DQS40B	DQS20B/CQ20B	DQ9B/CQn9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B117n	DIFFOUT_B117n	AK16	DQSn40B	DQSn20B/DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B118p	DIFFOUT_B118p	AM15	DQ39B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B118n	DIFFOUT_B118n	AM16	DQ39B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B119p	DIFFOUT_B119p	AK15	DQ40B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B119n	DIFFOUT_B119n	AL15	DQ40B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B120p	DIFFOUT_B120p	AN15	DQ40B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B120n	DIFFOUT_B120n	AP16	DQ40B	DQ20B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B121p	DIFFOUT_B121p	BA13	DQS41B	DQ21B/CQn21B	DQS9B/CQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B121n	DIFFOUT_B121n	BB13	DQSn41B	DQ21B	DQSn9B/DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B122p	DIFFOUT_B122p	BA14	DQ41B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B122n	DIFFOUT_B122n	BB14	DQ41B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B123p	DIFFOUT_B123p	AW15	DQS42B	DQS21B/CQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B123n	DIFFOUT_B123n	AY15	DQSn42B	DQSn21B/DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B124p	DIFFOUT_B124p	BA11	DQ41B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B124n	DIFFOUT_B124n	BB11	DQ41B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B125p	DIFFOUT_B125p	BA10	DQ42B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_RX_B125n	DIFFOUT_B125n	BB10	DQ42B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B126p	DIFFOUT_B126p	AY12	DQ42B	DQ21B	DQ9B	DQ3B
4B	VREFB4BN0	IO			DIFFIO_TX_B126n	DIFFOUT_B126n	AY13	DQ42B	DQ21B	DQ9B	DQ3B
4A	VREFB4AN0	IO			DIFFIO_RX_B127p	DIFFOUT_B127p	BA7	DQS43B	DQ22B/CQn22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B127n	DIFFOUT_B127n	BB7	DQSn43B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B128p	DIFFOUT_B128p	BB2	DQ43B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B128n	DIFFOUT_B128n	BB3	DQ43B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B129p	DIFFOUT_B129p	BB4	DQS44B	DQS22B/CQ22B	DQ10B/CQn10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B129n	DIFFOUT_B129n	BB5	DQSn44B	DQSn22B/DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B130p	DIFFOUT_B130p	BA8	DQ43B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B130n	DIFFOUT_B130n	BB8	DQ43B	DQ22B	DQ10B	DQ4B

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
4A	VREFB4AN0	IO			DIFFIO_RX_B131p	DIFFOUT_B131p	AW10	DQ44B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B131n	DIFFOUT_B131n	AY11	DQ44B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B132p	DIFFOUT_B132p	AY9	DQ44B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B132n	DIFFOUT_B132n	AY10	DQ44B	DQ22B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B133p	DIFFOUT_B133p	AD15	DQS45B	DQ23B/CQn23B	DQS10B/CQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B133n	DIFFOUT_B133n	AE15	DQSn45B	DQ23B	DQSn10B/DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B134p	DIFFOUT_B134p	AF13	DQ45B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B134n	DIFFOUT_B134n	AF14	DQ45B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B135p	DIFFOUT_B135p	AG13	DQS46B	DQS23B/CQ23B	DQ10B	DQ4B/CQn4B
4A	VREFB4AN0	IO			DIFFIO_RX_B135n	DIFFOUT_B135n	AH13	DQSn46B	DQSn23B/DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B136p	DIFFOUT_B136p	AJ14	DQ45B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B136n	DIFFOUT_B136n	AK14	DQ45B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B137p	DIFFOUT_B137p	AH14	DQ46B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B137n	DIFFOUT_B137n	AH15	DQ46B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B138p	DIFFOUT_B138p	AJ13	DQ46B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B138n	DIFFOUT_B138n	AK13	DQ46B	DQ23B	DQ10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B139n	DIFFOUT_B139n	AP15	DQ47B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B139p	DIFFOUT_B139p	AP14	DQ47B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B140n	DIFFOUT_B140n	AT14	DQSn47B	DQ24B	DQ11B	DQSn4B/DQ4B
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B140p	DIFFOUT_B140p	AR14	DQS47B	DQ24B/CQn24B	DQ11B	DQS4B/CQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B141n	DIFFOUT_B141n	AM14	DQ47B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B141p	DIFFOUT_B141p	AL14	DQ47B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B142n	DIFFOUT_B142n	AW13	DQSn48B	DQSn24B/DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B142p	DIFFOUT_B142p	AW12	DQS48B	DQS24B/CQ24B	DQ11B/CQn11B	DQ4B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B143n	DIFFOUT_B143n	AU14	DQ48B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B143p	DIFFOUT_B143p	AT13	DQ48B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B144n	DIFFOUT_B144n	AV14	DQ48B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B144p	DIFFOUT_B144p	AV13	DQ48B	DQ24B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B145n	DIFFOUT_B145n	BA5	DQ49B	DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B145p	DIFFOUT_B145p	AY6	DQ49B	DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B146n	DIFFOUT_B146n	AY3	DQSn49B	DQ25B	DQSn11B/DQ11B	DQ4B
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B146p	DIFFOUT_B146p	AW3	DQS49B	DQ25B/CQn25B	DQS11B/CQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B147n	DIFFOUT_B147n	AY4	DQ49B	DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B147p	DIFFOUT_B147p	AW4	DQ49B	DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B148n	DIFFOUT_B148n	AY7	DQSn50B	DQSn25B/DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B148p	DIFFOUT_B148p	AW7	DQS50B	DQS25B/CQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B149n	DIFFOUT_B149n	AW6	DQ50B	DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B149p	DIFFOUT_B149p	AW5	DQ50B	DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_RX_B150n	DIFFOUT_B150n	AW9	DQ50B	DQ25B	DQ11B	DQ4B
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_RX_B150p	DIFFOUT_B150p	AW8	DQ50B	DQ25B	DQ11B	DQ4B
4A		GND					AV12				
4A		nCE		nCE			AU12				
4A		nSTATUS		nSTATUS			AV11				
4A		CONF_DONE		CONF_DONE			AU10				
4A		nIO_PULLUP		nIO_PULLUP			AV8				
4A		MSEL0		MSEL0			AR12				
4A		MSEL1		MSEL1			AT11				
4A		MSEL2		MSEL2			AU11				
4A		MSEL3		MSEL3			AT10				
4A		MSEL4		MSEL4			AV9				
GXB_R0		REFCLK0Rn					AN9				
GXB_R0		REFCLK0Rp					AN10				
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AU2				
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AU1				
GXB_R0		GXB_TX_R0p					AU6				
GXB_R0		GXB_TX_R0n					AU5				
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AT4				
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AT3				
GXB_R0		GXB_TX_R1p					AT8				
GXB_R0		GXB_TX_R1n					AT7				
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AR2				
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AR1				
GXB_R0		GXB_TX_R2p					AR6				
GXB_R0		GXB_TX_R2n					AR5				
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AP4				
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AP3				
GXB_R0		GXB_TX_R3p					AP8				
GXB_R0		GXB_TX_R3n					AP7				
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					AN2				
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					AN1				
GXB_R0		GXB_TX_R4p					AN6				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_R0		GXB_TX_R4n					AN5				
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					AM4				
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					AM3				
GXB_R0		GXB_TX_R5p					AM8				
GXB_R0		GXB_TX_R5n					AM7				
GXB_R0		REFCLK1Rn					AL10				
GXB_R0		REFCLK1Rp					AL11				
GXB_R1		REFCLK2Rn					AJ9				
GXB_R1		REFCLK2Rp					AJ10				
GXB_R1		GXB_RX_R6p,GXB_REFCLK_R6p					AL2				
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					AL1				
GXB_R1		GXB_TX_R6p					AL6				
GXB_R1		GXB_TX_R6n					AL5				
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					AK4				
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					AK3				
GXB_R1		GXB_TX_R7p					AK8				
GXB_R1		GXB_TX_R7n					AK7				
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					AJ2				
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					AJ1				
GXB_R1		GXB_TX_R8p					AJ6				
GXB_R1		GXB_TX_R8n					AJ5				
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					AH4				
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					AH3				
GXB_R1		GXB_TX_R9p					AH8				
GXB_R1		GXB_TX_R9n					AH7				
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					AG2				
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					AG1				
GXB_R1		GXB_TX_R10p					AG6				
GXB_R1		GXB_TX_R10n					AG5				
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					AF4				
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					AF3				
GXB_R1		GXB_TX_R11p					AF8				
GXB_R1		GXB_TX_R11n					AF7				
GXB_R1		REFCLK3Rn					AG10				
GXB_R1		REFCLK3Rp					AG11				
GXB_R2		REFCLK4Rn					AE9				
GXB_R2		REFCLK4Rp					AE10				
GXB_R2		GXB_RX_R12p,GXB_REFCLK_R12p					AE2				
GXB_R2		GXB_RX_R12n,GXB_REFCLK_R12n					AE1				
GXB_R2		GXB_TX_R12p					AE6				
GXB_R2		GXB_TX_R12n					AE5				
GXB_R2		GXB_RX_R13p,GXB_REFCLK_R13p					AD4				
GXB_R2		GXB_RX_R13n,GXB_REFCLK_R13n					AD3				
GXB_R2		GXB_TX_R13p					AD8				
GXB_R2		GXB_TX_R13n					AD7				
GXB_R2		GXB_RX_R14p,GXB_REFCLK_R14p					AC2				
GXB_R2		GXB_RX_R14n,GXB_REFCLK_R14n					AC1				
GXB_R2		GXB_TX_R14p					AC6				
GXB_R2		GXB_TX_R14n					AC5				
GXB_R2		GXB_RX_R15p,GXB_REFCLK_R15p					AB4				
GXB_R2		GXB_RX_R15n,GXB_REFCLK_R15n					AB3				
GXB_R2		GXB_TX_R15p					AB8				
GXB_R2		GXB_TX_R15n					AB7				
GXB_R2		GXB_RX_R16p,GXB_REFCLK_R16p					AA2				
GXB_R2		GXB_RX_R16n,GXB_REFCLK_R16n					AA1				
GXB_R2		GXB_TX_R16p					AA6				
GXB_R2		GXB_TX_R16n					AA5				
GXB_R2		GXB_RX_R17p,GXB_REFCLK_R17p					Y4				
GXB_R2		GXB_RX_R17n,GXB_REFCLK_R17n					Y3				
GXB_R2		GXB_TX_R17p					Y8				
GXB_R2		GXB_TX_R17n					Y7				
GXB_R2		REFCLK5Rn					AC10				
GXB_R2		REFCLK5Rp					AC11				
GXB_R3		REFCLK6Rn					AA9				
GXB_R3		REFCLK6Rp					AA10				
GXB_R3		GXB_RX_R18p,GXB_REFCLK_R18p					W2				
GXB_R3		GXB_RX_R18n,GXB_REFCLK_R18n					W1				
GXB_R3		GXB_TX_R18p					W6				
GXB_R3		GXB_TX_R18n					W5				
GXB_R3		GXB_RX_R19p,GXB_REFCLK_R19p					V4				
GXB_R3		GXB_RX_R19n,GXB_REFCLK_R19n					V3				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
GXB_R3		GXB_TX_R19p					V8				
GXB_R3		GXB_TX_R19n					V7				
GXB_R3		GXB_RX_R20p,GXB_REFCLK_R20p					U2				
GXB_R3		GXB_RX_R20n,GXB_REFCLK_R20n					U1				
GXB_R3		GXB_TX_R20p					U6				
GXB_R3		GXB_TX_R20n					U5				
GXB_R3		GXB_RX_R21p,GXB_REFCLK_R21p					T4				
GXB_R3		GXB_RX_R21n,GXB_REFCLK_R21n					T3				
GXB_R3		GXB_TX_R21p					T8				
GXB_R3		GXB_TX_R21n					T7				
GXB_R3		GXB_RX_R22p,GXB_REFCLK_R22p					R2				
GXB_R3		GXB_RX_R22n,GXB_REFCLK_R22n					R1				
GXB_R3		GXB_TX_R22p					R6				
GXB_R3		GXB_TX_R22n					R5				
GXB_R3		GXB_RX_R23p,GXB_REFCLK_R23p					P4				
GXB_R3		GXB_RX_R23n,GXB_REFCLK_R23n					P3				
GXB_R3		GXB_TX_R23p					P8				
GXB_R3		GXB_TX_R23n					P7				
GXB_R3		REFCLK7Rn					W10				
GXB_R3		REFCLK7Rp					W11				
GXB_R4		REFCLK8Rn					U9				
GXB_R4		REFCLK8Rp					U10				
GXB_R4		GXB_RX_R24p,GXB_REFCLK_R24p					N2				
GXB_R4		GXB_RX_R24n,GXB_REFCLK_R24n					N1				
GXB_R4		GXB_TX_R24p					N6				
GXB_R4		GXB_TX_R24n					N5				
GXB_R4		GXB_RX_R25p,GXB_REFCLK_R25p					M4				
GXB_R4		GXB_RX_R25n,GXB_REFCLK_R25n					M3				
GXB_R4		GXB_TX_R25p					M8				
GXB_R4		GXB_TX_R25n					M7				
GXB_R4		GXB_RX_R26p,GXB_REFCLK_R26p					L2				
GXB_R4		GXB_RX_R26n,GXB_REFCLK_R26n					L1				
GXB_R4		GXB_TX_R26p					L6				
GXB_R4		GXB_TX_R26n					L5				
GXB_R4		GXB_RX_R27p,GXB_REFCLK_R27p					K4				
GXB_R4		GXB_RX_R27n,GXB_REFCLK_R27n					K3				
GXB_R4		GXB_TX_R27p					K8				
GXB_R4		GXB_TX_R27n					K7				
GXB_R4		GXB_RX_R28p,GXB_REFCLK_R28p					J2				
GXB_R4		GXB_RX_R28n,GXB_REFCLK_R28n					J1				
GXB_R4		GXB_TX_R28p					J6				
GXB_R4		GXB_TX_R28n					J5				
GXB_R4		GXB_RX_R29p,GXB_REFCLK_R29p					H4				
GXB_R4		GXB_RX_R29n,GXB_REFCLK_R29n					H3				
GXB_R4		GXB_TX_R29p					H8				
GXB_R4		GXB_TX_R29n					H7				
GXB_R4		REFCLK9Rn					R10				
GXB_R4		REFCLK9Rp					R11				
GXB_R5		REFCLK10Rn					N11				
GXB_R5		REFCLK10Rp					N10				
GXB_R5		GXB_RX_R30p,GXB_REFCLK_R30p					G2				
GXB_R5		GXB_RX_R30n,GXB_REFCLK_R30n					G1				
GXB_R5		GXB_TX_R30p					G6				
GXB_R5		GXB_TX_R30n					G5				
GXB_R5		GXB_RX_R31p,GXB_REFCLK_R31p					F4				
GXB_R5		GXB_RX_R31n,GXB_REFCLK_R31n					F3				
GXB_R5		GXB_TX_R31p					F8				
GXB_R5		GXB_TX_R31n					F7				
GXB_R5		GXB_RX_R32p,GXB_REFCLK_R32p					E2				
GXB_R5		GXB_RX_R32n,GXB_REFCLK_R32n					E1				
GXB_R5		GXB_TX_R32p					E6				
GXB_R5		GXB_TX_R32n					E5				
7A		GND					M12				
7A	VREFB7AN0	IO	RZQ_4		DIFFIO_RX_T1p	DIFFOUT_T1p	C7	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	C6	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	B6	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	A6	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T3p	DIFFOUT_T3p	D8	DQS1T	DQS1T/CQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T3n	DIFFOUT_T3n	E9	DQSn1T	DQSn1T/DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	B5	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	A5	DQ2T	DQ1T	DQ1T	DQ1T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T5p	DIFFOUT_T5p	C4	DQS2T	DQ1T/CQn1T	DQS1T/CQ1T	DQ1T
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T5n	DIFFOUT_T5n	C5	DQSn2T	DQ1T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	C3	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	B3	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	B8	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	A8	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	C8	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	C9	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T9p	DIFFOUT_T9p	B9	DQS3T	DQS2T/CQ2T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T9n	DIFFOUT_T9n	A9	DQSn3T	DQSn2T/DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	E11	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	E10	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T11p	DIFFOUT_T11p	G10	DQS4T	DQ2T/CQn2T	DQ1T	DQS1T/CQ1T
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T11n	DIFFOUT_T11n	F10	DQSn4T	DQ2T	DQ1T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	D10	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C10	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T13n	DIFFOUT_T13n	G13	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T13p	DIFFOUT_T13p	H13	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	G12	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	H12	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T15n	DIFFOUT_T15n	J13	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T15p	DIFFOUT_T15p	J12	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	F11	DQSn5T	DQSn3T/DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	G11	DQS5T	DQS3T/CQ3T	DQ2T	DQ1T/CQn1T
7A	VREFB7AN0	IO			DIFFIO_TX_T17n	DIFFOUT_T17n	D12	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T17p	DIFFOUT_T17p	E12	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	H10	DQSn6T	DQ3T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T18p	DIFFOUT_T18p	J10	DQS6T	DQ3T/CQn3T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T19n	DIFFOUT_T19n	J11	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T19p	DIFFOUT_T19p	K12	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	L13	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	M13	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T21n	DIFFOUT_T21n	N13	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T21p	DIFFOUT_T21p	N14	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T22n	DIFFOUT_T22n	P13	DQSn7T	DQSn4T/DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	R13	DQS7T	DQS4T/CQ4T	DQ2T/CQn2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T23n	DIFFOUT_T23n	T14	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_TX_T23p	DIFFOUT_T23p	T13	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T24n	R15	DQSn8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T24p	R14	DQS8T	DQ4T/CQn4T	DQ2T	DQ1T
7B	VREFB7BN0	IO			DIFFIO_TX_T25n	DIFFOUT_T25n	L15	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T25p	DIFFOUT_T25p	L14	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	J15	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	J14	DQ9T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T27n	DIFFOUT_T27n	K16	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T27p	DIFFOUT_T27p	L16	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	H15	DQSn9T	DQSn5T/DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T28p	DIFFOUT_T28p	G16	DQS9T	DQS5T/CQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T29n	DIFFOUT_T29n	J17	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T29p	DIFFOUT_T29p	K17	DQ10T	DQ5T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	H16	DQSn10T	DQ5T	DQSn3T/DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	J16	DQS10T	DQ5T/CQn5T	DQS3T/CQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T31n	DIFFOUT_T31n	U16	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T31p	DIFFOUT_T31p	V17	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	R16	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	P15	DQ11T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T33n	DIFFOUT_T33n	R17	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T33p	DIFFOUT_T33p	T17	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T34n	DIFFOUT_T34n	M15	DQSn11T	DQSn6T/DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T34p	DIFFOUT_T34p	N15	DQS11T	DQS6T/CQ6T	DQ3T/CQn3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T35n	DIFFOUT_T35n	N16	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T35p	DIFFOUT_T35p	P16	DQ12T	DQ6T	DQ3T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T36n	DIFFOUT_T36n	M17	DQSn12T	DQ6T	DQ3T	DQSn2T/DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T36p	DIFFOUT_T36p	N17	DQS12T	DQ6T/CQn6T	DQ3T	DQS2T/CQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T37n	DIFFOUT_T37n	G15	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T37p	DIFFOUT_T37p	G14	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	F14	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	F13	DQ13T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T39n	DIFFOUT_T39n	D13	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T39p	DIFFOUT_T39p	E13	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	E15	DQSn13T	DQSn7T/DQ7T	DQ4T	DQ2T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7B	VREFB7BN0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	E14	DQS13T	DQS7T/CQ7T	DQ4T	DQ2T/CQn2T
7B	VREFB7BN0	IO			DIFFIO_TX_T41n	DIFFOUT_T41n	D16	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T41p	DIFFOUT_T41p	D15	DQ14T	DQ7T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T42n	DIFFOUT_T42n	E16	DQSn14T	DQ7T	DQSn4T/DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	F16	DQS14T	DQ7T/CQn7T	DQS4T/CQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T43n	DIFFOUT_T43n	A11	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T43p	DIFFOUT_T43p	B11	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T44n	DIFFOUT_T44n	C13	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T44p	DIFFOUT_T44p	C12	DQ15T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T45n	DIFFOUT_T45n	A12	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T45p	DIFFOUT_T45p	B12	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	C15	DQSn15T	DQSn8T/DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	C14	DQS15T	DQS8T/CQ8T	DQ4T/CQn4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T47n	DIFFOUT_T47n	A15	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_TX_T47p	DIFFOUT_T47p	B15	DQ16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T48n	A14	DQSn16T	DQ8T	DQ4T	DQ2T
7B	VREFB7BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	B14	DQS16T	DQ8T/CQn8T	DQ4T	DQ2T
7C	VREFB7CN0	IO			DIFFIO_TX_T49n	DIFFOUT_T49n	J20	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T49p	DIFFOUT_T49p	J19	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T50n	DIFFOUT_T50n	H18	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T50p	DIFFOUT_T50p	J18	DQ17T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T51n	DIFFOUT_T51n	L19	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T51p	DIFFOUT_T51p	L18	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	M18	DQSn17T	DQSn9T/DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	N19	DQS17T	DQS9T/CQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T53n	DIFFOUT_T53n	N18	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T53p	DIFFOUT_T53p	P18	DQ18T	DQ9T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T54n	DIFFOUT_T54n	R18	DQSn18T	DQ9T	DQSn5T/DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T54p	DIFFOUT_T54p	T18	DQS18T	DQ9T/CQn9T	DQS5T/CQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T55n	DIFFOUT_T55n	F17	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T55p	DIFFOUT_T55p	G17	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	E17	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	E18	DQ19T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T57n	DIFFOUT_T57n	G18	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	G19	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	E19	DQSn19T	DQSn10T/DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	F19	DQS19T	DQS10T/CQ10T	DQ5T/CQn5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T59n	DIFFOUT_T59n	G20	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	H19	DQ20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T60n	DIFFOUT_T60n	E20	DQSn20T	DQ10T	DQ5T	
7C	VREFB7CN0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	F20	DQS20T	DQ10T/CQn10T	DQ5T	
7C	VREFB7CN0	IO	CLK19p		DIFFIO_RX_T61p	DIFFOUT_T61p	D18	DQ21T	DQ11T		
7C	VREFB7CN0	IO	CLK19n		DIFFIO_RX_T61n	DIFFOUT_T61n	D19	DQ21T	DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	C18	DQ21T	DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	B18	DQ21T	DQ11T		
7C	VREFB7CN0	IO	CLK18p		DIFFIO_RX_T63p	DIFFOUT_T63p	C16	DQS21T	DQS11T/CQ11T		
7C	VREFB7CN0	IO	CLK18n		DIFFIO_RX_T63n	DIFFOUT_T63n	B17	DQSn21T	DQSn11T/DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	C19	DQ22T	DQ11T		
7C	VREFB7CN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	C20	DQ22T	DQ11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T65p	DIFFOUT_T65p	A17	DQS22T	DQ11T/CQn11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T65n	DIFFOUT_T65n	A18	DQSn22T	DQ11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T66p	DIFFOUT_T66p	B20	DQ22T	DQ11T		
7C	VREFB7CN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T66n	DIFFOUT_T66n	A20	DQ22T	DQ11T		
8D	VREFB8DN0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	C21	DQ23T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_RX_T67n	DIFFOUT_T67n	C22	DQ23T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	B21	DQ23T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	A21	DQ23T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	D21	DQS23T	DQS12T/CQ12T		
8D	VREFB8DN0	IO			DIFFIO_RX_T69n	DIFFOUT_T69n	D22	DQSn23T	DQSn12T/DQ12T		
8D	VREFB8DN0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	B23	DQ24T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_TX_T70n	DIFFOUT_T70n	A23	DQ24T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	D24	DQS24T	DQ12T/CQn12T		
8D	VREFB8DN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	C24	DQSn24T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	B24	DQ24T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_TX_T72n	DIFFOUT_T72n	A24	DQ24T	DQ12T		
8D	VREFB8DN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	F22	DQ25T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	E21	DQ25T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	H21	DQ25T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	G21	DQ25T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	E22	DQS25T	DQS13T/CQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	E23	DQSn25T	DQSn13T/DQ13T	DQ6T	

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8D	VREFB8DN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	H22	DQ26T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	G22	DQ26T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	G23	DQS26T	DQ13T/CQn13T	DQS6T/CQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	F23	DQSn26T	DQ13T	DQSn6T/DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	J22	DQ26T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	J23	DQ26T	DQ13T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	L20	DQ27T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	K20	DQ27T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	N20	DQ27T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	M20	DQ27T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	P21	DQS27T	DQS14T/CQ14T	DQ6T/CQn6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	N21	DQSn27T	DQSn14T/DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	R19	DQ28T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	P19	DQ28T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	T20	DQS28T	DQ14T/CQn14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	R20	DQSn28T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	R21	DQ28T	DQ14T	DQ6T	
8D	VREFB8DN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	R22	DQ28T	DQ14T	DQ6T	
8C	VREFB8CN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	B26	DQ29T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	A26	DQ29T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T86p	DIFFOUT_T86p	D25	DQ29T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T86n	DIFFOUT_T86n	C25	DQ29T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T87p	DIFFOUT_T87p	B27	DQS29T	DQS15T/CQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T87n	DIFFOUT_T87n	A27	DQSn29T	DQSn15T/DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T88p	DIFFOUT_T88p	D27	DQ30T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T88n	DIFFOUT_T88n	C27	DQ30T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T89p	DIFFOUT_T89p	E26	DQS30T	DQ15T/CQn15T	DQS7T/CQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T89n	DIFFOUT_T89n	E27	DQSn30T	DQ15T	DQSn7T/DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T90p	DIFFOUT_T90p	D28	DQ30T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T90n	DIFFOUT_T90n	C28	DQ30T	DQ15T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T91p	DIFFOUT_T91p	G25	DQ31T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T91n	DIFFOUT_T91n	F25	DQ31T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T92p	DIFFOUT_T92p	E24	DQ31T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T92n	DIFFOUT_T92n	E25	DQ31T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T93p	DIFFOUT_T93p	G26	DQS31T	DQS16T/CQ16T	DQ7T/CQn7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T93n	DIFFOUT_T93n	F26	DQSn31T	DQSn16T/DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T94p	DIFFOUT_T94p	H24	DQ32T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T94n	DIFFOUT_T94n	G24	DQ32T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T95p	DIFFOUT_T95p	H25	DQS32T	DQ16T/CQn16T	DQ7T	DQS3T/CQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T95n	DIFFOUT_T95n	J24	DQSn32T	DQ16T	DQ7T	DQSn3T/DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T96p	DIFFOUT_T96p	H27	DQ32T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T96n	DIFFOUT_T96n	G27	DQ32T	DQ16T	DQ7T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T97p	DIFFOUT_T97p	M23	DQ33T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T97n	DIFFOUT_T97n	L23	DQ33T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T98p	DIFFOUT_T98p	L22	DQ33T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T98n	DIFFOUT_T98n	M21	DQ33T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T99p	DIFFOUT_T99p	N24	DQS33T	DQS17T/CQ17T	DQ8T	DQ3T/CQn3T
8C	VREFB8CN0	IO			DIFFIO_RX_T99n	DIFFOUT_T99n	N23	DQSn33T	DQSn17T/DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T100p	DIFFOUT_T100p	L25	DQ34T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T100n	DIFFOUT_T100n	K25	DQ34T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T101p	DIFFOUT_T101p	J26	DQS34T	DQ17T/CQn17T	DQS8T/CQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T101n	DIFFOUT_T101n	J25	DQSn34T	DQ17T	DQSn8T/DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T102p	DIFFOUT_T102p	M24	DQ34T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T102n	DIFFOUT_T102n	L24	DQ34T	DQ17T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T103p	DIFFOUT_T103p	T23	DQ35T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T103n	DIFFOUT_T103n	R23	DQ35T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T104p	DIFFOUT_T104p	V25	DQ35T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T104n	DIFFOUT_T104n	U25	DQ35T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T105p	DIFFOUT_T105p	R25	DQS35T	DQS18T/CQ18T	DQ8T/CQn8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T105n	DIFFOUT_T105n	T24	DQSn35T	DQSn18T/DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T106p	DIFFOUT_T106p	R24	DQ36T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T106n	DIFFOUT_T106n	P24	DQ36T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T107p	DIFFOUT_T107p	P25	DQS36T	DQ18T/CQn18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_RX_T107n	DIFFOUT_T107n	N25	DQSn36T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T108p	DIFFOUT_T108p	N26	DQ36T	DQ18T	DQ8T	DQ3T
8C	VREFB8CN0	IO			DIFFIO_TX_T108n	DIFFOUT_T108n	M26	DQ36T	DQ18T	DQ8T	DQ3T
8B	VREFB8BN0	IO			DIFFIO_RX_T109p	DIFFOUT_T109p	B30	DQ37T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T109n	DIFFOUT_T109n	A30	DQ37T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T110p	DIFFOUT_T110p	B29	DQ37T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T110n	DIFFOUT_T110n	A29	DQ37T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T111p	DIFFOUT_T111p	D30	DQS37T	DQS19T/CQ19T	DQ9T	DQ4T

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8B	VREFB8BN0	IO			DIFFIO_RX_T111n	DIFFOUT_T111n	C30	DQSn37T	DQSn19T/DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T112p	DIFFOUT_T112p	A32	DQ38T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T112n	DIFFOUT_T112n	A33	DQ38T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T113p	DIFFOUT_T113p	C33	DQS38T	DQ19T/CQn19T	DQS9T/CQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T113n	DIFFOUT_T113n	B33	DQSn38T	DQ19T	DQSn9T/DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T114p	DIFFOUT_T114p	C31	DQ38T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T114n	DIFFOUT_T114n	B32	DQ38T	DQ19T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T115p	DIFFOUT_T115p	F28	DQ39T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T115n	DIFFOUT_T115n	E28	DQ39T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T116p	DIFFOUT_T116p	E31	DQ39T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T116n	DIFFOUT_T116n	D31	DQ39T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T117p	DIFFOUT_T117p	E29	DQS39T	DQS20T/CQ20T	DQ9T/CQn9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T117n	DIFFOUT_T117n	E30	DQSn39T	DQSn20T/DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T118p	DIFFOUT_T118p	H30	DQ40T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T118n	DIFFOUT_T118n	G30	DQ40T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T119p	DIFFOUT_T119p	G29	DQS40T	DQ20T/CQn20T	DQ9T	DQS4T/CQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T119n	DIFFOUT_T119n	F29	DQSn40T	DQ20T	DQ9T	DQSn4T/DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T120p	DIFFOUT_T120p	H28	DQ40T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T120n	DIFFOUT_T120n	G28	DQ40T	DQ20T	DQ9T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T121p	DIFFOUT_T121p	J29	DQ41T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T121n	DIFFOUT_T121n	J30	DQ41T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T122p	DIFFOUT_T122p	L28	DQ41T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T122n	DIFFOUT_T122n	K28	DQ41T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T123p	DIFFOUT_T123p	J27	DQS41T	DQS21T/CQ21T	DQ10T	DQ4T/CQn4T
8B	VREFB8BN0	IO			DIFFIO_RX_T123n	DIFFOUT_T123n	J28	DQSn41T	DQSn21T/DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T124p	DIFFOUT_T124p	N27	DQ42T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T124n	DIFFOUT_T124n	M27	DQ42T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T125p	DIFFOUT_T125p	L27	DQS42T	DQ21T/CQn21T	DQS10T/CQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T125n	DIFFOUT_T125n	L26	DQSn42T	DQ21T	DQSn10T/DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	N29	DQ42T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	M29	DQ42T	DQ21T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T127p	DIFFOUT_T127p	R27	DQ43T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T127n	DIFFOUT_T127n	P27	DQ43T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	T26	DQ43T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T128n	DIFFOUT_T128n	R26	DQ43T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T129p	DIFFOUT_T129p	U28	DQS43T	DQS22T/CQ22T	DQ10T/CQn10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T129n	DIFFOUT_T129n	T27	DQSn43T	DQSn22T/DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T130p	DIFFOUT_T130p	P28	DQ44T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T130n	DIFFOUT_T130n	N28	DQ44T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T131p	DIFFOUT_T131p	T30	DQS44T	DQ22T/CQn22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_RX_T131n	DIFFOUT_T131n	R30	DQSn44T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T132p	DIFFOUT_T132p	R28	DQ44T	DQ22T	DQ10T	DQ4T
8B	VREFB8BN0	IO			DIFFIO_TX_T132n	DIFFOUT_T132n	R29	DQ44T	DQ22T	DQ10T	DQ4T
8A	VREFB8AN0	IO	CLK17p		DIFFIO_RX_T133p	DIFFOUT_T133p	H31	DQ45T	DQ23T	DQ11T	
8A	VREFB8AN0	IO	CLK17n		DIFFIO_RX_T133n	DIFFOUT_T133n	G31	DQ45T	DQ23T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T134p	DIFFOUT_T134p	H33	DQ45T	DQ23T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T134n	DIFFOUT_T134n	G33	DQ45T	DQ23T	DQ11T	
8A	VREFB8AN0	IO	CLK16p		DIFFIO_RX_T135p	DIFFOUT_T135p	J33	DQS45T	DQS23T/CQ23T	DQ11T	
8A	VREFB8AN0	IO	CLK16n		DIFFIO_RX_T135n	DIFFOUT_T135n	J32	DQSn45T	DQSn23T/DQ23T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T136p	DIFFOUT_T136p	P30	DQ46T	DQ23T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T136n	DIFFOUT_T136n	N30	DQ46T	DQ23T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_RX_T137p	DIFFOUT_T137p	M30	DQS46T	DQ23T/CQn23T	DQS11T/CQ11T	
8A	VREFB8AN0	IO			DIFFIO_RX_T137n	DIFFOUT_T137n	L31	DQSn46T	DQ23T	DQSn11T/DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T138p	DIFFOUT_T138p	L29	DQ46T	DQ23T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T138n	DIFFOUT_T138n	L30	DQ46T	DQ23T	DQ11T	
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T139p	DIFFOUT_T139p	F32	DQ47T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T139n	DIFFOUT_T139n	E32	DQ47T	DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T140p	DIFFOUT_T140p	E33	DQ47T	DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T140n	DIFFOUT_T140n	D33	DQ47T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T141p	DIFFOUT_T141p	F31	DQS47T	DQS24T/CQ24T	DQ11T/CQn11T	
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T141n	DIFFOUT_T141n	G32	DQSn47T	DQSn24T/DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T142p	DIFFOUT_T142p	B35	DQ48T	DQ24T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_TX_T142n	DIFFOUT_T142n	A35	DQ48T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T143p	DIFFOUT_T143p	C34	DQS48T	DQ24T/CQn24T	DQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T143n	DIFFOUT_T143n	C35	DQSn48T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T144p	DIFFOUT_T144p	D34	DQ48T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T144n	DIFFOUT_T144n	D35	DQ48T	DQ24T	DQ11T	
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T145p	DIFFOUT_T145p	A41	DQ49T	DQ25T		
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T145n	DIFFOUT_T145n	A40	DQ49T	DQ25T		
8A	VREFB8AN0	IO			DIFFIO_TX_T146p	DIFFOUT_T146p	C40	DQ49T	DQ25T		
8A	VREFB8AN0	IO			DIFFIO_TX_T146n	DIFFOUT_T146n	B40	DQ49T	DQ25T		

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T147p	DIFFOUT_T147p	C38	DQS49T	DQS25T/CQ25T		
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T147n	DIFFOUT_T147n	C39	DQSn49T	DQSn25T/DQ25T		
8A	VREFB8AN0	IO			DIFFIO_TX_T148p	DIFFOUT_T148p	B36	DQ50T	DQ25T		
8A	VREFB8AN0	IO		nPERSTR0	DIFFIO_TX_T148n	DIFFOUT_T148n	A36	DQ50T	DQ25T		
8A	VREFB8AN0	IO		nPERSTR1	DIFFIO_RX_T149p	DIFFOUT_T149p	C37	DQS50T	DQ25T/CQn25T		
8A	VREFB8AN0	IO	RZQ_5		DIFFIO_RX_T149n	DIFFOUT_T149n	C36	DQSn50T	DQ25T		
8A	VREFB8AN0	IO		nPERSTL1	DIFFIO_TX_T150p	DIFFOUT_T150p	B38	DQ50T	DQ25T		
8A	VREFB8AN0	IO		nPERSTL0	DIFFIO_TX_T150n	DIFFOUT_T150n	A38	DQ50T	DQ25T		
		GND					AA35				
		GND					AA36				
		GND					AA39				
		GND					AA40				
		GND					AB32				
		GND					AB34				
		GND					AB37				
		GND					AB38				
		GND					AB41				
		GND					AB42				
		GND					AC31				
		GND					AC35				
		GND					AC36				
		GND					AC39				
		GND					AC40				
		GND					AD33				
		GND					AD37				
		GND					AD38				
		GND					AD41				
		GND					AD42				
		GND					AE35				
		GND					AE36				
		GND					AE39				
		GND					AE40				
		GND					AF31				
		GND					AF32				
		GND					AF34				
		GND					AF37				
		GND					AF38				
		GND					AF41				
		GND					AF42				
		GND					AG35				
		GND					AG36				
		GND					AG39				
		GND					AG40				
		GND					AH33				
		GND					AH37				
		GND					AH38				
		GND					AH41				
		GND					AH42				
		GND					AJ31				
		GND					AJ35				
		GND					AJ36				
		GND					AJ39				
		GND					AJ40				
		GND					AK32				
		GND					AK34				
		GND					AK37				
		GND					AK38				
		GND					AK41				
		GND					AK42				
		GND					AL31				
		GND					AL35				
		GND					AL36				
		GND					AL39				
		GND					AL40				
		GND					AM31				
		GND					AM33				
		GND					AM37				
		GND					AM38				
		GND					AM41				
		GND					AM42				
		GND					AN31				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AN35				
		GND					AN36				
		GND					AN39				
		GND					AN40				
		GND					AP32				
		GND					AP34				
		GND					AP37				
		GND					AP38				
		GND					AP41				
		GND					AP42				
		GND					AR33				
		GND					AR34				
		GND					AR35				
		GND					AR36				
		GND					AR39				
		GND					AR40				
		GND					AT34				
		GND					AT37				
		GND					AT38				
		GND					AT41				
		GND					AT42				
		GND					AU35				
		GND					AU36				
		GND					AU39				
		GND					AU40				
		GND					AV37				
		GND					AV38				
		GND					AV41				
		GND					AV42				
		GND					AW41				
		GND					AY41				
		GND					AY42				
		GND					B41				
		GND					B42				
		GND					C41				
		GND					D37				
		GND					D38				
		GND					D41				
		GND					D42				
		GND					E35				
		GND					E36				
		GND					E39				
		GND					E40				
		GND					F34				
		GND					F37				
		GND					F38				
		GND					F41				
		GND					F42				
		GND					G35				
		GND					G36				
		GND					G39				
		GND					G40				
		GND					H34				
		GND					H37				
		GND					H38				
		GND					H41				
		GND					H42				
		GND					J35				
		GND					J36				
		GND					J39				
		GND					J40				
		GND					K33				
		GND					K34				
		GND					K37				
		GND					K38				
		GND					K41				
		GND					K42				
		GND					L32				
		GND					L35				
		GND					L36				
		GND					L39				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					L40				
		GND					M32				
		GND					M37				
		GND					M38				
		GND					M41				
		GND					M42				
		GND					N34				
		GND					N35				
		GND					N36				
		GND					N39				
		GND					N40				
		GND					P32				
		GND					P34				
		GND					P37				
		GND					P38				
		GND					P41				
		GND					P42				
		GND					R31				
		GND					R35				
		GND					R36				
		GND					R39				
		GND					R40				
		GND					T31				
		GND					T33				
		GND					T37				
		GND					T38				
		GND					T41				
		GND					T42				
		GND					U31				
		GND					U35				
		GND					U36				
		GND					U39				
		GND					U40				
		GND					V32				
		GND					V34				
		GND					V37				
		GND					V38				
		GND					V41				
		GND					V42				
		GND					W31				
		GND					W35				
		GND					W36				
		GND					W39				
		GND					W40				
		GND					Y31				
		GND					Y33				
		GND					Y37				
		GND					Y38				
		GND					Y41				
		GND					Y42				
		GND					AA3				
		GND					AA4				
		GND					AA7				
		GND					AA8				
		GND					AB1				
		GND					AB11				
		GND					AB2				
		GND					AB5				
		GND					AB6				
		GND					AB9				
		GND					AC12				
		GND					AC3				
		GND					AC4				
		GND					AC7				
		GND					AC8				
		GND					AD1				
		GND					AD10				
		GND					AD2				
		GND					AD5				
		GND					AD6				
		GND					AE3				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AE4				
		GND					AE7				
		GND					AE8				
		GND					AF1				
		GND					AF11				
		GND					AF12				
		GND					AF2				
		GND					AF5				
		GND					AF6				
		GND					AF9				
		GND					AG3				
		GND					AG4				
		GND					AG7				
		GND					AG8				
		GND					AH1				
		GND					AH10				
		GND					AH2				
		GND					AH5				
		GND					AH6				
		GND					AJ12				
		GND					AJ3				
		GND					AJ4				
		GND					AJ7				
		GND					AJ8				
		GND					AK1				
		GND					AK11				
		GND					AK2				
		GND					AK5				
		GND					AK6				
		GND					AK9				
		GND					AL12				
		GND					AL3				
		GND					AL4				
		GND					AL7				
		GND					AL8				
		GND					AM1				
		GND					AM10				
		GND					AM12				
		GND					AM2				
		GND					AM5				
		GND					AM6				
		GND					AN12				
		GND					AN3				
		GND					AN4				
		GND					AN7				
		GND					AN8				
		GND					AP1				
		GND					AP11				
		GND					AP2				
		GND					AP5				
		GND					AP6				
		GND					AP9				
		GND					AR10				
		GND					AR3				
		GND					AR4				
		GND					AR7				
		GND					AR8				
		GND					AR9				
		GND					AT1				
		GND					AT2				
		GND					AT5				
		GND					AT6				
		GND					AT9				
		GND					AU3				
		GND					AU4				
		GND					AU7				
		GND					AU8				
		GND					AV1				
		GND					AV2				
		GND					AV5				
		GND					AV6				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AW2				
		GND					AY1				
		GND					AY2				
		GND					B1				
		GND					B2				
		GND					C2				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					D6				
		GND					E3				
		GND					E4				
		GND					E7				
		GND					E8				
		GND					F1				
		GND					F2				
		GND					F5				
		GND					F6				
		GND					F9				
		GND					G3				
		GND					G4				
		GND					G7				
		GND					G8				
		GND					H1				
		GND					H2				
		GND					H5				
		GND					H6				
		GND					H9				
		GND					J3				
		GND					J4				
		GND					J7				
		GND					J8				
		GND					K1				
		GND					K10				
		GND					K2				
		GND					K5				
		GND					K6				
		GND					K9				
		GND					L11				
		GND					L3				
		GND					L4				
		GND					L7				
		GND					L8				
		GND					M1				
		GND					M11				
		GND					M2				
		GND					M5				
		GND					M6				
		GND					N3				
		GND					N4				
		GND					N7				
		GND					N8				
		GND					N9				
		GND					P1				
		GND					P11				
		GND					P2				
		GND					P5				
		GND					P6				
		GND					P9				
		GND					R12				
		GND					R3				
		GND					R4				
		GND					R7				
		GND					R8				
		GND					T1				
		GND					T10				
		GND					T12				
		GND					T2				
		GND					T5				
		GND					T6				
		GND					U12				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					U3				
		GND					U4				
		GND					U7				
		GND					U8				
		GND					V1				
		GND					V11				
		GND					V2				
		GND					V5				
		GND					V6				
		GND					V9				
		GND					W12				
		GND					W3				
		GND					W4				
		GND					W7				
		GND					W8				
		GND					Y1				
		GND					Y10				
		GND					Y12				
		GND					Y2				
		GND					Y5				
		GND					Y6				
		GND					AA14				
		GND					AA16				
		GND					AA18				
		GND					AA20				
		GND					AA23				
		GND					AA25				
		GND					AA26				
		GND					AA28				
		GND					AA29				
		GND					AB13				
		GND					AB15				
		GND					AB19				
		GND					AB24				
		GND					AB27				
		GND					AB30				
		GND					AC14				
		GND					AC16				
		GND					AC18				
		GND					AC20				
		GND					AC23				
		GND					AC25				
		GND					AC26				
		GND					AC28				
		GND					AD13				
		GND					AD30				
		GND					AE14				
		GND					AE16				
		GND					AE19				
		GND					AE21				
		GND					AE23				
		GND					AE25				
		GND					AE27				
		GND					AE29				
		GND					AG14				
		GND					AG17				
		GND					AG20				
		GND					AG23				
		GND					AG26				
		GND					AG29				
		GND					AJ15				
		GND					AJ18				
		GND					AJ21				
		GND					AJ24				
		GND					AJ27				
		GND					AJ30				
		GND					AK12				
		GND					AK31				
		GND					AL13				
		GND					AL16				
		GND					AL19				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					AL22				
		GND					AL25				
		GND					AL28				
		GND					AN14				
		GND					AN17				
		GND					AN20				
		GND					AN23				
		GND					AN26				
		GND					AN29				
		GND					AP12				
		GND					AP31				
		GND					AR11				
		GND					AR15				
		GND					AR18				
		GND					AR21				
		GND					AR24				
		GND					AR27				
		GND					AR30				
		GND					AR32				
		GND					AT12				
		GND					AU13				
		GND					AU16				
		GND					AU19				
		GND					AU22				
		GND					AU25				
		GND					AU28				
		GND					AU31				
		GND					AU9				
		GND					AV10				
		GND					AV3				
		GND					AV34				
		GND					AV36				
		GND					AV39				
		GND					AV4				
		GND					AV40				
		GND					AV7				
		GND					AW11				
		GND					AW14				
		GND					AW17				
		GND					AW20				
		GND					AW23				
		GND					AW26				
		GND					AW29				
		GND					AW32				
		GND					AY35				
		GND					AY5				
		GND					AY8				
		GND					B10				
		GND					B13				
		GND					B16				
		GND					B19				
		GND					B22				
		GND					B25				
		GND					B28				
		GND					B31				
		GND					B34				
		GND					B37				
		GND					B39				
		GND					B4				
		GND					B7				
		GND					BA12				
		GND					BA15				
		GND					BA18				
		GND					BA21				
		GND					BA24				
		GND					BA27				
		GND					BA3				
		GND					BA30				
		GND					BA33				
		GND					BA36				
		GND					BA38				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					BA40				
		GND					BA6				
		GND					BA9				
		GND					D11				
		GND					D14				
		GND					D17				
		GND					D20				
		GND					D23				
		GND					D26				
		GND					D29				
		GND					D3				
		GND					D32				
		GND					D36				
		GND					D39				
		GND					D4				
		GND					D40				
		GND					D7				
		GND					D9				
		GND					E34				
		GND					F12				
		GND					F15				
		GND					F18				
		GND					F21				
		GND					F24				
		GND					F27				
		GND					F30				
		GND					F33				
		GND					G34				
		GND					G9				
		GND					H11				
		GND					H14				
		GND					H17				
		GND					H20				
		GND					H23				
		GND					H26				
		GND					H29				
		GND					H32				
		GND					J34				
		GND					J9				
		GND					K11				
		GND					K13				
		GND					K15				
		GND					K18				
		GND					K21				
		GND					K24				
		GND					K27				
		GND					K30				
		GND					K32				
		GND					M14				
		GND					M16				
		GND					M19				
		GND					M22				
		GND					M25				
		GND					M28				
		GND					M31				
		GND					N12				
		GND					N31				
		GND					P14				
		GND					P17				
		GND					P20				
		GND					P23				
		GND					P26				
		GND					P29				
		GND					P31				
		GND					T16				
		GND					T19				
		GND					T22				
		GND					T25				
		GND					T28				
		GND					U14				
		GND					U17				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		GND					U19				
		GND					U21				
		GND					U23				
		GND					U26				
		GND					U29				
		GND					V12				
		GND					V13				
		GND					V15				
		GND					V20				
		GND					V22				
		GND					V24				
		GND					V27				
		GND					V30				
		GND					V31				
		GND					W14				
		GND					W16				
		GND					W18				
		GND					W23				
		GND					W26				
		GND					W28				
		GND					W29				
		GND					Y13				
		GND					Y15				
		GND					Y17				
		GND					Y19				
		GND					Y21				
		GND					Y24				
		GND					Y27				
		GND					Y30				
		GND					AC22				
		VCC					AE18				
		VCC					AE20				
		VCC					AE22				
		VCC					AE24				
		VCC					U18				
		VCC					U20				
		VCC					U22				
		VCC					U24				
		VCC					AA17				
		VCC					AA19				
		VCC					AA21				
		VCC					AA22				
		VCC					AA24				
		VCC					AB17				
		VCC					AB18				
		VCC					AB20				
		VCC					AB23				
		VCC					AB25				
		VCC					AC19				
		VCC					AC21				
		VCC					AC24				
		VCC					AD18				
		VCC					AD19				
		VCC					AD20				
		VCC					AD21				
		VCC					AD22				
		VCC					AD23				
		VCC					AD24				
		VCC					V18				
		VCC					V19				
		VCC					V21				
		VCC					V23				
		VCC					W17				
		VCC					W19				
		VCC					W20				
		VCC					W21				
		VCC					W22				
		VCC					W24				
		VCC					W25				
		VCC					Y18				
		VCC					Y20				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCC					Y22				
		VCC					Y23				
		VCC					Y25				
		VCC					AB21				
		VCCPT					AF15				
		VCCPT					AF21				
		VCCPT					AF30				
		VCCPT					T15				
		VCCPT					T21				
		VCCPT					T29				
		DNU					BA41				
		DNU					BA42				
		DNU					AK30				
		DNU					AP20				
		DNU					BA1				
		DNU					BA2				
		DNU					P12				
		DNU					J21				
		DNU					AB22				
		VCCPGM					AM30				
		VCCPGM					AP13				
		VCCPGM					J31				
		TEMPDIODEn					A2				
		TEMPDIODEp					A3				
		VCCBAT					AM13				
		VCCIO3A					BA37				
		VCCIO3A					BA39				
		VCCIO3B					BA35				
		VCCIO3B					BB33				
		VCCIO3C					BB27				
		VCCIO3C					BB30				
		VCCIO3D					BB21				
		VCCIO3D					BB24				
		VCCIO4A					BA4				
		VCCIO4A					BB6				
		VCCIO4B					BB12				
		VCCIO4B					BB9				
		VCCIO4C					BB15				
		VCCIO4C					BB18				
		VCCIO7A					A4				
		VCCIO7A					A7				
		VCCIO7B					A10				
		VCCIO7B					A13				
		VCCIO7C					A16				
		VCCIO7C					A19				
		VCCIO8A					A37				
		VCCIO8A					A39				
		VCCIO8B					A31				
		VCCIO8B					A34				
		VCCIO8C					A25				
		VCCIO8C					A28				
		VCCIO8D					A22				
		VCCIO8D					C23				
		VCCPD3AB					AY29				
		VCCPD3AB					AY32				
		VCCPD3CD					AY23				
		VCCPD3CD					AY26				
		VCCPD4					AY14				
		VCCPD4					AY17				
		VCCPD7					C11				
		VCCPD7					C17				
		VCCPD8					C26				
		VCCPD8					C29				
		VCCPD8					C32				
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AN30				
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AN27				
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AN24				
3D	VREFB3DN0	VREFB3DN0	VREFB3DN0				AN21				
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AR13				
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AN16				
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AN19				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				K14				
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				L17				
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				K19				
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				K29				
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				K26				
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				K23				
8D	VREFB8DN0	VREFB8DN0	VREFB8DN0				L21				
		VCCH_GXBL0					AM34				
		VCCH_GXBL1					AH34				
		VCCH_GXBL2					AD34				
		VCCH_GXBL3					Y34				
		VCCH_GXBL4					T34				
		VCCH_GXBL5					M34				
		VCCH_GXBR0					AM9				
		VCCH_GXBR1					AH9				
		VCCH_GXBR2					AD9				
		VCCH_GXBR3					Y9				
		VCCH_GXBR4					T9				
		VCCH_GXBR5					M9				
		VCCR_GXBL0					AP33				
		VCCR_GXBL1					AK33				
		VCCR_GXBL2					AF33				
		VCCR_GXBL3					AB33				
		VCCR_GXBL4					V33				
		VCCR_GXBL5					P33				
		VCCR_GXBR0					AP10				
		VCCR_GXBR1					AK10				
		VCCR_GXBR2					AF10				
		VCCR_GXBR3					AB10				
		VCCR_GXBR4					V10				
		VCCR_GXBR5					P10				
		VCCT_GXBL0					AM32				
		VCCT_GXBL0					AN32				
		VCCT_GXBL1					AH32				
		VCCT_GXBL1					AJ32				
		VCCT_GXBL2					AD32				
		VCCT_GXBL2					AE32				
		VCCT_GXBL3					AA32				
		VCCT_GXBL3					Y32				
		VCCT_GXBL4					T32				
		VCCT_GXBL4					U32				
		VCCT_GXBL5					L33				
		VCCT_GXBL5					M33				
		VCCT_GXBR0					AM11				
		VCCT_GXBR0					AN11				
		VCCT_GXBR1					AH11				
		VCCT_GXBR1					AJ11				
		VCCT_GXBR2					AD11				
		VCCT_GXBR2					AE11				
		VCCT_GXBR3					AA11				
		VCCT_GXBR3					Y11				
		VCCT_GXBR4					T11				
		VCCT_GXBR4					U11				
		VCCT_GXBR5					L10				
		VCCT_GXBR5					M10				
		VCCHIP_L					AA27				
		VCCHIP_L					AB26				
		VCCHIP_L					AB28				
		VCCHIP_L					U27				
		VCCHIP_L					V26				
		VCCHIP_L					V28				
		VCCHIP_L					W27				
		VCCHIP_L					Y26				
		VCCHIP_L					Y28				
		VCCHIP_R					AA15				
		VCCHIP_R					AB16				
		VCCHIP_R					AC15				
		VCCHIP_R					AD14				
		VCCHIP_R					AD16				
		VCCHIP_R					U15				
		VCCHIP_R					V16				

Bank Number	VREF	Pin Name/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1760	DQS for X4	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36
		VCCHIP_R					W15				
		VCCHIP_R					Y16				
		RREF_BL					AW42				
		RREF_BR					AW1				
		RREF_TL					C42				
		RREF_TR					C1				
		VCCA_FPLL					AJ22				
		VCCA_FPLL					P22				
		VCCA_FPLL					AA31				
		VCCA_FPLL					AD31				
		VCCA_FPLL					AG31				
		VCCA_FPLL					AA12				
		VCCA_FPLL					AD12				
		VCCA_FPLL					AG12				
		VCCA_GXBL0					AL34				
		VCCA_GXBL1					AG34				
		VCCA_GXBL2					AC34				
		VCCA_GXBL3					W34				
		VCCA_GXBL4					R34				
		VCCA_GXBL5					L34				
		VCCA_GXBR0					AL9				
		VCCA_GXBR1					AG9				
		VCCA_GXBR2					AC9				
		VCCA_GXBR3					W9				
		VCCA_GXBR4					R9				
		VCCA_GXBR5					L9				
		VCCHSSI_L					AA30				
		VCCHSSI_L					AB29				
		VCCHSSI_L					AC30				
		VCCHSSI_L					AE30				
		VCCHSSI_L					U30				
		VCCHSSI_L					V29				
		VCCHSSI_L					W30				
		VCCHSSI_L					Y29				
		VCCHSSI_R					AA13				
		VCCHSSI_R					AB14				
		VCCHSSI_R					AC13				
		VCCHSSI_R					AE13				
		VCCHSSI_R					U13				
		VCCHSSI_R					V14				
		VCCHSSI_R					W13				
		VCCHSSI_R					Y14				
		VCCD_FPLL					AK22				
		VCCD_FPLL					N22				
		VCCD_FPLL					AB31				
		VCCD_FPLL					AE31				
		VCCD_FPLL					AH31				
		VCCD_FPLL					AB12				
		VCCD_FPLL					AE12				
		VCCD_FPLL					AH12				
		VCC_AUX					AL30				
		VCC_AUX					AM20				
		VCC_AUX					AN13				
		VCC_AUX					K22				
		VCC_AUX					K31				
		VCC_AUX					L12				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the
Stratix V Device Family Pin Connection Guidelines.
(2) The GXB_REFCLK pin is not supported in the current Quartus II software version, but will be supported in the future Quartus II software release version.

Pin Information for the Stratix® V 5SGXB5 Device
Version 1.1

Version Number	Date	Changes Made
1.0	7/22/2011	Initial release.
1.1	9/12/2011	Reassigned DQ/DQS pins for Banks 3A, 4, 7, and 8A.