TYPE	BANK	HF35 Package
Transceiver I/O	1C	28
Transceiver I/O	1D	28
Transceiver I/O	1E	28
Transceiver I/O	1F	28
LVDS I/O	2K	48
HPS shared LVDS I/O	2L	48
HPS shared LVDS I/O	2M	48
HPS shared LVDS I/O	2N	48
LVDS I/O	3A	8
LVDS I/O	3B	48
3.3V I/O	3C	48
LVDS I/O	3D	8
3V I/O	6A	8
HPS shared LVDS I/O	HPS	48
SDM shared LVDS I/O	SDM	29

i. Total LVDS channels per bank supporting SERDES Non-DPA and DPA mode is equivalent to (LVDS I/O per bank)/2, inclusive of clock pair. Please refer to Dedicated Tx/Rx Channel column in the pin-out table for the channel availability.
ii. Total LVDS channels supporting SERDES Soft-CDR mode is 12 pairs per bank. Please refer to Soft CDR column in the pin out table for the channel availability.

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
3C		VREFB3CN0	IO	IO33_LS5_0						AM1				
3C		VREFB3CN0	IO	IO33_LS5_1						AM2				
3C		VREFB3CN0	IO	IO33_LS5_2						Y5				
3C		VREFB3CN0	IO	IO33_LS5_3						AA5				
3C		VREFB3CN0	IO	IO33_LS5_4						AC4				
3C		VREFB3CN0	IO	IO33_LS5_5						AB5				
3C		VREFB3CN0	IO	IO33_LS5_6						AC5				
3C		VREFB3CN0	IO	IO33_LS5_7						AB6				
3C		VREFB3CN0	IO	IO33_LS4_0						AE4				
3C		VREFB3CN0	IO	IO33_LS4_1						AE5				
3C		VREFB3CN0	IO	IO33_LS4_2						Y4				
3C		VREFB3CN0	IO	IO33_LS4_3						AA4				
3C		VREFB3CN0	IO	IO33_LS4_4						AA3				
3C		VREFB3CN0	IO	IO33_LS4_5						AB3				
3C		VREFB3CN0	IO	IO33_LS4_6						AC3				
3C		VREFB3CN0	IO	IO33_LS4_7						AD4				
3C		VREFB3CN0	IO	IO33_LS3_0						AG1				
3C		VREFB3CN0	IO	IO33_LS3_1						AH1				
3C		VREFB3CN0	IO	IO33_LS3_2						AJ1				
3C		VREFB3CN0	IO	IO33_LS3_3						AK1				
3C		VREFB3CN0	IO	IO33_LS3_4						AJ2				
3C		VREFB3CN0	IO	IO33_LS3_5						AJ3				
3C		VREFB3CN0	IO	IO33_LS3_6						AK2				
3C		VREFB3CN0	IO	IO33_LS3_7						AL2				
3C		VREFB3CN0	IO	IO33_LS2_0						AE1				
3C		VREFB3CN0	IO	IO33_LS2_1						AE2				
3C		VREFB3CN0	IO	IO33_LS2_2						AD2				
3C		VREFB3CN0	IO	IO33_LS2_3						AD3				
3C		VREFB3CN0	IO	IO33_LS2_4						AF3				
3C		VREFB3CN0	IO	IO33_LS2_5						AF4				
3C		VREFB3CN0	IO	IO33_LS2_6						AG3				
3C		VREFB3CN0	IO	IO33_LS2_7						AH3				
3C		VREFB3CN0	IO	IO33_LS1_0						Y2				
3C		VREFB3CN0	IO	IO33_LS1_1						AA2				
3C		VREFB3CN0	IO	IO33_LS1_2						AB1				
3C		VREFB3CN0	IO	IO33_LS1_3						AB2				
3C		VREFB3CN0	IO	IO33_LS1_4						AC1				
3C		VREFB3CN0	IO	IO33_LS1_5						AD1				
3C		VREFB3CN0	IO	IO33_LS1_6						AF2				
3C		VREFB3CN0	IO	IO33_LS1_7						AG2				
3C		VREFB3CN0	IO	IO33_LS0_0						U3				
3C		VREFB3CN0	IO	IO33_LS0_1						V3				
3C		VREFB3CN0	IO	IO33_LS0_2						U5				
3C		VREFB3CN0	IO	IO33_LS0_3						V4				
3C		VREFB3CN0	IO	IO33_LS0_4						W2				
3C		VREFB3CN0	IO	IO33_LS0_5						Y1				
3C		VREFB3CN0	IO	IO33_LS0_6						W3				
3C		VREFB3CN0	IO	IO33_LS0_7						W4				
1F			REFCLK_GXBL1F_CHTp							L28				
1F			REFCLK_GXBL1F_CHTn							L27				
1F			GXBL1F_TX_CH5n							A31				
1F			GXBL1F_TX_CH5p							A32				
1F			GXBL1F_RX_CH5n,GXBL1F_REFCLK5n							B29				
1F			GXBL1F_RX_CH5p,GXBL1F_REFCLK5p							B30				
1F			GXBL1F_TX_CH4n						Yes	C31				
1F			GXBL1F_TX_CH4p						Yes	C32				
1F			GXBL1F_RX_CH4n,GXBL1F_REFCLK4n						Yes	D29				
1F			GXBL1F_RX_CH4p,GXBL1F_REFCLK4p						Yes	D30				
1F			GXBL1F_TX_CH3n						Yes	D33				
1F			GXBL1F_TX_CH3p						Yes	D34				
1F			GXBL1F_RX_CH3n,GXBL1F_REFCLK3n						Yes	F29				
1F			GXBL1F_RX_CH3p,GXBL1F_REFCLK3p						Yes	F30				
1F			GXBL1F_TX_CH2n							E31				
1F			GXBL1F_TX_CH2p							E32				
1F			GXBL1F_RX_CH2n,GXBL1F_REFCLK2n							H29				
1F			GXBL1F_RX_CH2p,GXBL1F_REFCLK2p							H30				
1F			GXBL1F_TX_CH1n						Yes	F33				
1F			GXBL1F_TX_CH1p						Yes	F34				
1F			GXBL1F_RX_CH1n,GXBL1F_REFCLK1n						Yes	K29				
1F			GXBL1F_RX_CH1p,GXBL1F_REFCLK1p						Yes	K30				
1F			GXBL1F_TX_CH0n						Yes	G31				
1F			GXBL1F_TX_CH0p						Yes	G32				
1F			GXBL1F_RX_CH0n,GXBL1F_REFCLK0n						Yes	L31				
1F			GXBL1F_RX_CH0p,GXBL1F_REFCLK0p						Yes	L32				
1F			REFCLK_GXBL1F_CHBp							N28				
1F			REFCLK_GXBL1F_CHBn							N27				
1E			REFCLK_GXBL1E_CHTp							R28				
1E			REFCLK_GXBL1E_CHTn							R27				
1E			GXBL1E_TX_CH5n							H33				
1E			GXBL1E_TX_CH5p							H34				
1E			GXBL1E_RX_CH5n,GXBL1E_REFCLK5n							M29				
1E			GXBL1E_RX_CH5p,GXBL1E_REFCLK5p							M30				
1E			GXBL1E_TX_CH4n						Yes	J31				
1E			GXBL1E_TX_CH4p						Yes	J32				
1E			GXBL1E_RX_CH4n,GXBL1E_REFCLK4n						Yes	N31				
1E			GXBL1E_RX_CH4p,GXBL1E_REFCLK4p						Yes	N32				
1E			GXBL1E_TX_CH3n						Yes	K33				
1E			GXBL1E_TX_CH3p						Yes	K34				
1E			GXBL1E_RX_CH3n,GXBL1E_REFCLK3n						Yes	P29				
1E			GXBL1E_RX_CH3p,GXBL1E_REFCLK3p						Yes	P30				
1E			GXBL1E_TX_CH2n							M33				
1E			GXBL1E_TX_CH2p							M34				
1E			GXBL1E_RX_CH2n,GXBL1E_REFCLK2n							R31				
1E			GXBL1E_RX_CH2p,GXBL1E_REFCLK2p							R32				
1E			GXBL1E_TX_CH1n						Yes	P33				
1E			GXBL1E_TX_CH1p						Yes	P34				
1E			GXBL1E_RX_CH1n,GXBL1E_REFCLK1n						Yes	T29				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
1E			GXBL1E_RX_CH1p,GXBL1E_REFCLK1p						Yes	T30				
1E			GXBL1E_TX_CH0n						Yes	T33				
1E			GXBL1E_TX_CH0p						Yes	T34				
1E			GXBL1E_RX_CH0n,GXBL1E_REFCLK0n						Yes	U31				
1E			GXBL1E_RX_CH0p,GXBL1E_REFCLK0p						Yes	U32				
1E			REFCLK_GXBL1E_CHBp							U28				
1E			REFCLK_GXBL1E_CHBn							U27				
1D			REFCLK_GXBL1D_CHTp							W28				
1D			REFCLK_GXBL1D_CHTn							W27				
1D			GXBL1D_TX_CH5n							V33				
1D			GXBL1D_TX_CH5p							V34				
1D			GXBL1D_RX_CH5n,GXBL1D_REFCLK5n							V29				
1D			GXBL1D_RX_CH5p,GXBL1D_REFCLK5p							V30				
1D			GXBL1D_TX_CH4n						Yes	Y33				
1D			GXBL1D_TX_CH4p						Yes	Y34				
1D			GXBL1D_RX_CH4n,GXBL1D_REFCLK4n						Yes	W31				
1D			GXBL1D_RX_CH4p,GXBL1D_REFCLK4p						Yes	W32				
1D			GXBL1D_TX_CH3n						Yes	AB33				
1D			GXBL1D_TX_CH3p						Yes	AB34				
1D			GXBL1D_RX_CH3n,GXBL1D_REFCLK3n						Yes	Y29				
1D			GXBL1D_RX_CH3p,GXBL1D_REFCLK3p						Yes	Y30				
1D			GXBL1D_TX_CH2n							AD33				
1D			GXBL1D_TX_CH2p							AD34				
1D			GXBL1D_RX_CH2n,GXBL1D_REFCLK2n							AA31				
1D			GXBL1D_RX_CH2p,GXBL1D_REFCLK2p							AA32				
1D			GXBL1D_TX_CH1n						Yes	AF33				
1D			GXBL1D_TX_CH1p						Yes	AF34				
1D			GXBL1D_RX_CH1n,GXBL1D_REFCLK1n						Yes	AB29				
1D			GXBL1D_RX_CH1p,GXBL1D_REFCLK1p						Yes	AB30				
1D			GXBL1D_TX_CH0n						Yes	AG31				
1D			GXBL1D_TX_CH0p						Yes	AG32				
1D			GXBL1D_RX_CH0n,GXBL1D_REFCLK0n						Yes	AC31				
1D			GXBL1D_RX_CH0p,GXBL1D_REFCLK0p						Yes	AC32				
1D			REFCLK_GXBL1D_CHBp							AA28				
1D			REFCLK_GXBL1D_CHBn							AA27				
1C			REFCLK_GXBL1C_CHTp							AC28				
1C			REFCLK_GXBL1C_CHTn							AC27				
1C			GXBL1C_TX_CH5n							AH33				
1C			GXBL1C_TX_CH5p							AH34				
1C			GXBL1C_RX_CH5n,GXBL1C_REFCLK5n							AD29				
1C			GXBL1C_RX_CH5p,GXBL1C_REFCLK5p							AD30				
1C			GXBL1C_TX_CH4n						Yes	AJ31				
1C			GXBL1C_TX_CH4p						Yes	AJ32				
1C			GXBL1C_RX_CH4n,GXBL1C_REFCLK4n						Yes	AE31				
1C			GXBL1C_RX_CH4p,GXBL1C_REFCLK4p						Yes	AE32				
1C			GXBL1C_TX_CH3n						Yes	AK33				
1C			GXBL1C_TX_CH3p						Yes	AK34				
1C			GXBL1C_RX_CH3n,GXBL1C_REFCLK3n						Yes	AF29				
1C			GXBL1C_RX_CH3p,GXBL1C_REFCLK3p						Yes	AF30				
1C			GXBL1C_TX_CH2n							AL31				
1C			GXBL1C_TX_CH2p							AL32				
1C			GXBL1C_RX_CH2n,GXBL1C_REFCLK2n							AH29				
1C			GXBL1C_RX_CH2p,GXBL1C_REFCLK2p							AH30				
1C			GXBL1C_TX_CH1n						Yes	AM33				
1C			GXBL1C_TX_CH1p						Yes	AM34				
1C			GXBL1C_RX_CH1n,GXBL1C_REFCLK1n						Yes	AE29				
1C			GXBL1C_RX_CH1p,GXBL1C_REFCLK1p						Yes	AK30				
1C			GXBL1C_TX_CH0n						Yes	AN31				
1C			GXBL1C_TX_CH0p						Yes	AN32				
1C			GXBL1C_RX_CH0n,GXBL1C_REFCLK0n						Yes	AM29				
1C			GXBL1C_RX_CH0p,GXBL1C_REFCLK0p						Yes	AM30				
1C			REFCLK_GXBL1C_CHBp							AE28				
1C			REFCLK_GXBL1C_CHBn							AE27				
6A			IO3V0_10		nPERSTL0					AP26				
6A			IO3V1_10							AN26				
6A			IO3V2_10							AM26				
6A			IO3V3_10							AM27				
6A			IO3V4_10							AL27				
6A			IO3V5_10							AK27				
6A			IO3V6_10							AK26				
6A			IO3V7_10							AJ26				
2N	47	VREFB2NN0	IO			HPS_DDR	LVDS2N_1n	No		A9	DQ0	DQ0	DQ0	DQ0
2N	46	VREFB2NN0	IO			HPS_DDR	LVDS2N_1p	No		A10	DQ0	DQ0	DQ0	DQ0
2N	45	VREFB2NN0	IO			HPS_DDR	LVDS2N_2n	Yes		B15	DQSn0	DQ0	DQ0	DQ0
2N	44	VREFB2NN0	IO			HPS_DDR	LVDS2N_2p	Yes		C15	DQS0	DQ0	DQ0	DQ0
2N	43	VREFB2NN0	IO			HPS_DDR	LVDS2N_3n	No		A8	DQ0	DQ0	DQ0	DQ0
2N	42	VREFB2NN0	IO			HPS_DDR	LVDS2N_3p	No		B8	DQ0	DQ0	DQ0	DQ0
2N	41	VREFB2NN0	IO			HPS_DDR	LVDS2N_4n	Yes		A13	DQSn1	DQSn0/CQn0	DQ0	DQ0
2N	40	VREFB2NN0	IO			HPS_DDR	LVDS2N_4p	Yes		B13	DQS1	DQS0/CQ0	DQ0	DQ0
2N	39	VREFB2NN0	IO			HPS_DDR	LVDS2N_5n	No		J14	DQ1	DQ0	DQ0	DQ0
2N	38	VREFB2NN0	IO			HPS_DDR	LVDS2N_5p	No		H14	DQ1	DQ0	DQ0	DQ0
2N	37	VREFB2NN0	IO			HPS_DDR	LVDS2N_6n	Yes		B12	DQ1	DQ0	DQ0	DQ0
2N	36	VREFB2NN0	IO			HPS_DDR	LVDS2N_6p	Yes		A12	DQ1	DQ0	DQ0	DQ0
2N	35	VREFB2NN0	IO			HPS_DDR	LVDS2N_7n	No		K15	DQ2	DQ1	DQ0	DQ0
2N	34	VREFB2NN0	IO			HPS_DDR	LVDS2N_7p	No		L15	DQ2	DQ1	DQ0	DQ0
2N	33	VREFB2NN0	IO			HPS_DDR	LVDS2N_8n	Yes		C14	DQSn2	DQ1	DQSn0/CQn0	DQ0
2N	32	VREFB2NN0	IO			HPS_DDR	LVDS2N_8p	Yes		D14	DQS2	DQ1	DQS0/CQ0	DQ0
2N	31	VREFB2NN0	IO			HPS_DDR	LVDS2N_9n	No		H13	DQ2	DQ1	DQ0	DQ0
2N	30	VREFB2NN0	IO			HPS_DDR	LVDS2N_9p	No		J13	DQ2	DQ1	DQ0	DQ0
2N	29	VREFB2NN0	IO	PLL_2N_CLKOUT1n		HPS_DDR	LVDS2N_10n	Yes		E15	DQSn3	DQSn1/CQn1	DQ0	DQ0
2N	28	VREFB2NN0	IO	PLL_2N_CLKOUT1p,PLL_2N_CLKOUT1,PLL_2N_FB1		HPS_DDR	LVDS2N_10p	Yes		F15	DQS3	DQS1/CQ1	DQ0	DQ0
2N	27	VREFB2NN0	IO			HPS_DDR	LVDS2N_11n	No		F12	DQ3	DQ1	DQ0	DQ0
2N	26	VREFB2NN0	IO	RZQ_2N		HPS_DDR	LVDS2N_11p	No		G12	DQ3	DQ1	DQ0	DQ0
2N	25	VREFB2NN0	IO	CLK_2N_1n		HPS_DDR	LVDS2N_12n	Yes		E14	DQ3	DQ1	DQ0	DQ0
2N	24	VREFB2NN0	IO	CLK_2N_1p		HPS_DDR	LVDS2N_12p	Yes		F14	DQ3	DQ1	DQ0	DQ0
2N	23	VREFB2NN0	IO	CLK_2N_0n		HPS_DDR	LVDS2N_13n	No		C10	DQ4	DQ2	DQ1	DQ0
2N	22	VREFB2NN0	IO	CLK_2N_0p		HPS_DDR	LVDS2N_13p	No		B10	DQ4	DQ2	DQ1	DQ0

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
2N	21	VREFB2NN0	IO			HPS_DDR	LVDS2N_14n	Yes		H15	DQSn4	DQ2	DQ1	DQSn0/CQn0
2N	20	VREFB2NN0	IO			HPS_DDR	LVDS2N_14p	Yes		G15	DQS4	DQ2	DQ1	DQS0/CQ0
2N	19	VREFB2NN0	IO	PLL_2N_CLKOUT0n		HPS_DDR	LVDS2N_15n	No		D9	DQ4	DQ2	DQ1	DQ0
2N	18	VREFB2NN0	IO	PLL_2N_CLKOUT0p,PLL_2N_CLKOUT0,PLL_2N_FB0		HPS_DDR	LVDS2N_15p	No		C9	DQ4	DQ2	DQ1	DQ0
2N	17	VREFB2NN0	IO			HPS_DDR	LVDS2N_16n	Yes		D13	DQSn5	DQSn2/CQn2	DQ1	DQ0
2N	16	VREFB2NN0	IO			HPS_DDR	LVDS2N_16p	Yes		C13	DQS5	DQS2/CQ2	DQ1	DQ0
2N	15	VREFB2NN0	IO			HPS_DDR	LVDS2N_17n	No		K12	DQ5	DQ2	DQ1	DQ0
2N	14	VREFB2NN0	IO			HPS_DDR	LVDS2N_17p	No		J12	DQ5	DQ2	DQ1	DQ0
2N	13	VREFB2NN0	IO			HPS_DDR	LVDS2N_18n	Yes		C11	DQ5	DQ2	DQ1	DQ0
2N	12	VREFB2NN0	IO			HPS_DDR	LVDS2N_18p	Yes		B11	DQ5	DQ2	DQ1	DQ0
2N	11	VREFB2NN0	IO			HPS_DDR	LVDS2N_19n	No		E10	DQ6	DQ3	DQ1	DQ0
2N	10	VREFB2NN0	IO			HPS_DDR	LVDS2N_19p	No		F10	DQ6	DQ3	DQ1	DQ0
2N	9	VREFB2NN0	IO			HPS_DDR	LVDS2N_20n	Yes		F13	DQSn6	DQ3	DQSn1/CQn1	DQ0
2N	8	VREFB2NN0	IO			HPS_DDR	LVDS2N_20p	Yes		G13	DQS6	DQ3	DQS1/CQ1	DQ0
2N	7	VREFB2NN0	IO			HPS_DDR	LVDS2N_21n	No		H11	DQ6	DQ3	DQ1	DQ0
2N	6	VREFB2NN0	IO			HPS_DDR	LVDS2N_21p	No		G11	DQ6	DQ3	DQ1	DQ0
2N	5	VREFB2NN0	IO			HPS_DDR	LVDS2N_22n	Yes		D12	DQSn7	DQSn3/CQn3	DQ1	DQ0
2N	4	VREFB2NN0	IO			HPS_DDR	LVDS2N_22p	Yes		E12	DQS7	DQS3/CQ3	DQ1	DQ0
2N	3	VREFB2NN0	IO			HPS_DDR	LVDS2N_23n	No		H10	DQ7	DQ3	DQ1	DQ0
2N	2	VREFB2NN0	IO			HPS_DDR	LVDS2N_23p	No		G10	DQ7	DQ3	DQ1	DQ0
2N	1	VREFB2NN0	IO			HPS_DDR	LVDS2N_24n	Yes		D11	DQ7	DQ3	DQ1	DQ0
2N	0	VREFB2NN0	IO			HPS_DDR	LVDS2N_24p	Yes		E11	DQ7	DQ3	DQ1	DQ0
2M	47	VREFB2MN0	IO			HPS_DDR	LVDS2M_1n	No		C18	DQ8	DQ4	DQ2	DQ1
2M	46	VREFB2MN0	IO			HPS_DDR	LVDS2M_1p	No		D18	DQ8	DQ4	DQ2	DQ1
2M	45	VREFB2MN0	IO			HPS_DDR	LVDS2M_2n	Yes		K16	DQSn8	DQ4	DQ2	DQ1
2M	44	VREFB2MN0	IO			HPS_DDR	LVDS2M_2p	Yes		J16	DQS8	DQ4	DQ2	DQ1
2M	43	VREFB2MN0	IO			HPS_DDR	LVDS2M_3n	No		G17	DQ8	DQ4	DQ2	DQ1
2M	42	VREFB2MN0	IO			HPS_DDR	LVDS2M_3p	No		F18	DQ8	DQ4	DQ2	DQ1
2M	41	VREFB2MN0	IO			HPS_DDR	LVDS2M_4n	Yes		K17	DQSn9	DQSn4/CQn4	DQ2	DQ1
2M	40	VREFB2MN0	IO			HPS_DDR	LVDS2M_4p	Yes		J17	DQS9	DQS4/CQ4	DQ2	DQ1
2M	39	VREFB2MN0	IO			HPS_DDR	LVDS2M_5n	No		B20	DQ9	DQ4	DQ2	DQ1
2M	38	VREFB2MN0	IO			HPS_DDR	LVDS2M_5p	No		A20	DQ9	DQ4	DQ2	DQ1
2M	37	VREFB2MN0	IO			HPS_DDR	LVDS2M_6n	Yes		G16	DQ9	DQ4	DQ2	DQ1
2M	36	VREFB2MN0	IO			HPS_DDR	LVDS2M_6p	Yes		H16	DQ9	DQ4	DQ2	DQ1
2M	35	VREFB2MN0	IO			HPS_DDR	LVDS2M_7n	No		C19	DQ10	DQ5	DQ2	DQ1
2M	34	VREFB2MN0	IO			HPS_DDR	LVDS2M_7p	No		C20	DQ10	DQ5	DQ2	DQ1
2M	33	VREFB2MN0	IO			HPS_DDR	LVDS2M_8n	Yes		A14	DQSn10	DQ5	DQSn2/CQn2	DQ1
2M	32	VREFB2MN0	IO			HPS_DDR	LVDS2M_8p	Yes		A15	DQS10	DQ5	DQS2/CQ2	DQ1
2M	31	VREFB2MN0	IO			HPS_DDR	LVDS2M_9n	No		D19	DQ10	DQ5	DQ2	DQ1
2M	30	VREFB2MN0	IO			HPS_DDR	LVDS2M_9p	No		E19	DQ10	DQ5	DQ2	DQ1
2M	29	VREFB2MN0	IO	PLL_2M_CLKOUT1n		HPS_DDR	LVDS2M_10n	Yes		D16	DQSn11	DQSn5/CQn5	DQ2	DQ1
2M	28	VREFB2MN0	IO	PLL_2M_CLKOUT1p,PLL_2M_CLKOUT1,PLL_2M_FB1		HPS_DDR	LVDS2M_10p	Yes		C16	DQS11	DQS5/CQ5	DQ2	DQ1
2M	27	VREFB2MN0	IO			HPS_DDR	LVDS2M_11n	No		G18	DQ11	DQ5	DQ2	DQ1
2M	26	VREFB2MN0	IO	RZQ_2M		HPS_DDR	LVDS2M_11p	No		F19	DQ11	DQ5	DQ2	DQ1
2M	25	VREFB2MN0	IO	CLK_2M_1n		HPS_DDR	LVDS2M_12n	Yes		J18	DQ11	DQ5	DQ2	DQ1
2M	24	VREFB2MN0	IO	CLK_2M_1p		HPS_DDR	LVDS2M_12p	Yes		H18	DQ11	DQ5	DQ2	DQ1
2M	23	VREFB2MN0	IO	CLK_2M_0n		HPS_DDR	LVDS2M_13n	No		H19	DQ12	DQ6	DQ3	DQ1
2M	22	VREFB2MN0	IO	CLK_2M_0p		HPS_DDR	LVDS2M_13p	No		J19	DQ12	DQ6	DQ3	DQ1
2M	21	VREFB2MN0	IO			HPS_DDR	LVDS2M_14n	Yes		E16	DQSn12	DQ6	DQ3	DQSn1/CQn1
2M	20	VREFB2MN0	IO			HPS_DDR	LVDS2M_14p	Yes		F17	DQS12	DQ6	DQ3	DQS1/CQ1
2M	19	VREFB2MN0	IO	PLL_2M_CLKOUT0n		HPS_DDR	LVDS2M_15n	No		A22	DQ12	DQ6	DQ3	DQ1
2M	18	VREFB2MN0	IO	PLL_2M_CLKOUT0p,PLL_2M_CLKOUT0,PLL_2M_FB0		HPS_DDR	LVDS2M_15p	No		B22	DQ12	DQ6	DQ3	DQ1
2M	17	VREFB2MN0	IO			HPS_DDR	LVDS2M_16n	Yes		D17	DQSn13	DQSn6/CQn6	DQ3	DQ1
2M	16	VREFB2MN0	IO			HPS_DDR	LVDS2M_16p	Yes		E17	DQS13	DQS6/CQ6	DQ3	DQ1
2M	15	VREFB2MN0	IO			HPS_DDR	LVDS2M_17n	No		B21	DQ13	DQ6	DQ3	DQ1
2M	14	VREFB2MN0	IO			HPS_DDR	LVDS2M_17p	No		C21	DQ13	DQ6	DQ3	DQ1
2M	13	VREFB2MN0	IO			HPS_DDR	LVDS2M_18n	Yes		A17	DQ13	DQ6	DQ3	DQ1
2M	12	VREFB2MN0	IO			HPS_DDR	LVDS2M_18p	Yes		B16	DQ13	DQ6	DQ3	DQ1
2M	11	VREFB2MN0	IO			HPS_DDR	LVDS2M_19n	No		D21	DQ14	DQ7	DQ3	DQ1
2M	10	VREFB2MN0	IO			HPS_DDR	LVDS2M_19p	No		E21	DQ14	DQ7	DQ3	DQ1
2M	9	VREFB2MN0	IO			HPS_DDR	LVDS2M_20n	Yes		B17	DQSn14	DQ7	DQSn3/CQn3	DQ1
2M	8	VREFB2MN0	IO			HPS_DDR	LVDS2M_20p	Yes		A18	DQS14	DQ7	DQS3/CQ3	DQ1
2M	7	VREFB2MN0	IO			HPS_DDR	LVDS2M_21n	No		E20	DQ14	DQ7	DQ3	DQ1
2M	6	VREFB2MN0	IO			HPS_DDR	LVDS2M_21p	No		F20	DQ14	DQ7	DQ3	DQ1
2M	5	VREFB2MN0	IO			HPS_DDR	LVDS2M_22n	Yes		B18	DQSn15	DQSn7/CQn7	DQ3	DQ1
2M	4	VREFB2MN0	IO			HPS_DDR	LVDS2M_22p	Yes		A19	DQS15	DQS7/CQ7	DQ3	DQ1
2M	3	VREFB2MN0	IO			HPS_DDR	LVDS2M_23n	No		H20	DQ15	DQ7	DQ3	DQ1
2M	2	VREFB2MN0	IO			HPS_DDR	LVDS2M_23p	No		G20	DQ15	DQ7	DQ3	DQ1
2M	1	VREFB2MN0	IO			HPS_DDR	LVDS2M_24n	Yes		G21	DQ15	DQ7	DQ3	DQ1
2M	0	VREFB2MN0	IO			HPS_DDR	LVDS2M_24p	Yes		H21	DQ15	DQ7	DQ3	DQ1
2L	47	VREFB2LN0	IO			HPS_DDR	LVDS2L_1n	No		A23	DQ16	DQ8	DQ4	DQ2
2L	46	VREFB2LN0	IO			HPS_DDR	LVDS2L_1p	No		B23	DQ16	DQ8	DQ4	DQ2
2L	45	VREFB2LN0	IO			HPS_DDR	LVDS2L_2n	Yes		H23	DQSn16	DQ8	DQ4	DQ2
2L	44	VREFB2LN0	IO			HPS_DDR	LVDS2L_2p	Yes		H24	DQS16	DQ8	DQ4	DQ2
2L	43	VREFB2LN0	IO			HPS_DDR	LVDS2L_3n	No		D22	DQ16	DQ8	DQ4	DQ2
2L	42	VREFB2LN0	IO			HPS_DDR	LVDS2L_3p	No		E22	DQ16	DQ8	DQ4	DQ2
2L	41	VREFB2LN0	IO			HPS_DDR	LVDS2L_4n	Yes		K21	DQSn17	DQSn8/CQn8	DQ4	DQ2
2L	40	VREFB2LN0	IO			HPS_DDR	LVDS2L_4p	Yes		J21	DQS17	DQS8/CQ8	DQ4	DQ2
2L	39	VREFB2LN0	IO			HPS_DDR	LVDS2L_5n	No		D23	DQ17	DQ8	DQ4	DQ2
2L	38	VREFB2LN0	IO			HPS_DDR	LVDS2L_5p	No		C23	DQ17	DQ8	DQ4	DQ2
2L	37	VREFB2LN0	IO			HPS_DDR	LVDS2L_6n	Yes		J23	DQ17	DQ8	DQ4	DQ2
2L	36	VREFB2LN0	IO			HPS_DDR	LVDS2L_6p	Yes		J22	DQ17	DQ8	DQ4	DQ2
2L	35	VREFB2LN0	IO			HPS_DDR	LVDS2L_7n	No		F22	DQ18	DQ9	DQ4	DQ2
2L	34	VREFB2LN0	IO			HPS_DDR	LVDS2L_7p	No		G22	DQ18	DQ9	DQ4	DQ2
2L	33	VREFB2LN0	IO			HPS_DDR	LVDS2L_8n	Yes		A27	DQSn18	DQ9	DQSn4/CQn4	DQ2
2L	32	VREFB2LN0	IO			HPS_DDR	LVDS2L_8p	Yes		B27	DQS18	DQ9	DQS4/CQ4	DQ2
2L	31	VREFB2LN0	IO			HPS_DDR	LVDS2L_9n	No		A24	DQ18	DQ9	DQ4	DQ2
2L	30	VREFB2LN0	IO			HPS_DDR	LVDS2L_9p	No		B25	DQ18	DQ9	DQ4	DQ2
2L	29	VREFB2LN0	IO	PLL_2L_CLKOUT1n		HPS_DDR	LVDS2L_10n	Yes		L22	DQSn19	DQSn9/CQn9	DQ4	DQ2
2L	28	VREFB2LN0	IO	PLL_2L_CLKOUT1p,PLL_2L_CLKOUT1,PLL_2L_FB1		HPS_DDR	LVDS2L_10p	Yes		K22	DQS19	DQS9/CQ9	DQ4	DQ2
2L	27	VREFB2LN0	IO			HPS_DDR	LVDS2L_11n	No		D24	DQ19	DQ9	DQ4	DQ2
2L	26	VREFB2LN0	IO	RZQ_2L		HPS_DDR	LVDS2L_11p	No		E24	DQ19	DQ9	DQ4	DQ2
2L	25	VREFB2LN0	IO	CLK_2L_1n		HPS_DDR	LVDS2L_12n	Yes		J24	DQ19	DQ9	DQ4	DQ2
2L	24	VREFB2LN0	IO	CLK_2L_1p		HPS_DDR	LVDS2L_12p	Yes		K24	DQ19	DQ9	DQ4	DQ2
2L	23	VREFB2LN0	IO	CLK_2L_0n		HPS_DDR	LVDS2L_13n	No		F23	DQ20	DQ10	DQ5	DQ2
2L	22	VREFB2LN0	IO	CLK_2L_0p		HPS_DDR	LVDS2L_13p	No		G23	DQ20	DQ10	DQ5	DQ2
2L	21	VREFB2LN0	IO			HPS_DDR	LVDS2L_14n	Yes		H26	DQSn20	DQ10	DQ5	DQSn2/CQn2

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
2L	20	VREFB2LN0	IO			HPS_DDR	LVDS2L_14p	Yes		H25	DQS20	DQ10	DQ5	DQS2/CQ2
2L	19	VREFB2LN0	IO	PLL_2L_CLKOUT0n		HPS_DDR	LVDS2L_15n	No		C24	DQ20	DQ10	DQ5	DQ2
2L	18	VREFB2LN0	IO	PLL_2L_CLKOUT0p,PLL_2L_CLKOUT0,PLL_2L_FB0		HPS_DDR	LVDS2L_15p	No		C25	DQ20	DQ10	DQ5	DQ2
2L	17	VREFB2LN0	IO			HPS_DDR	LVDS2L_16n	Yes		D27	DQSn21	DQSn10/CQn10	DQ5	DQ2
2L	16	VREFB2LN0	IO			HPS_DDR	LVDS2L_16p	Yes		E26	DQS21	DQS10/CQ10	DQ5	DQ2
2L	15	VREFB2LN0	IO			HPS_DDR	LVDS2L_17n	No		A25	DQ21	DQ10	DQ5	DQ2
2L	14	VREFB2LN0	IO			HPS_DDR	LVDS2L_17p	No		B26	DQ21	DQ10	DQ5	DQ2
2L	13	VREFB2LN0	IO			HPS_DDR	LVDS2L_18n	Yes		M23	DQ21	DQ10	DQ5	DQ2
2L	12	VREFB2LN0	IO			HPS_DDR	LVDS2L_18p	Yes		M22	DQ21	DQ10	DQ5	DQ2
2L	11	VREFB2LN0	IO			HPS_DDR	LVDS2L_19n	No		C26	DQ22	DQ11	DQ5	DQ2
2L	10	VREFB2LN0	IO			HPS_DDR	LVDS2L_19p	No		D26	DQ22	DQ11	DQ5	DQ2
2L	9	VREFB2LN0	IO			HPS_DDR	LVDS2L_20n	Yes		L23	DQSn22	DQ11	DQSn5/CQn5	DQ2
2L	8	VREFB2LN0	IO			HPS_DDR	LVDS2L_20p	Yes		L24	DQS22	DQ11	DQS5/CQ5	DQ2
2L	7	VREFB2LN0	IO			HPS_DDR	LVDS2L_21n	No		E25	DQ22	DQ11	DQ5	DQ2
2L	6	VREFB2LN0	IO			HPS_DDR	LVDS2L_21p	No		F25	DQ22	DQ11	DQ5	DQ2
2L	5	VREFB2LN0	IO			HPS_DDR	LVDS2L_22n	Yes		G26	DQSn23	DQSn11/CQn11	DQ5	DQ2
2L	4	VREFB2LN0	IO			HPS_DDR	LVDS2L_22p	Yes		G27	DQS23	DQS11/CQ11	DQ5	DQ2
2L	3	VREFB2LN0	IO			HPS_DDR	LVDS2L_23n	No		F24	DQ23	DQ11	DQ5	DQ2
2L	2	VREFB2LN0	IO			HPS_DDR	LVDS2L_23p	No		G25	DQ23	DQ11	DQ5	DQ2
2L	1	VREFB2LN0	IO			HPS_DDR	LVDS2L_24n	Yes		F27	DQ23	DQ11	DQ5	DQ2
2L	0	VREFB2LN0	IO			HPS_DDR	LVDS2L_24p	Yes		E27	DQ23	DQ11	DQ5	DQ2
2K	47	VREFB2KN0	IO				LVDS2K_1n	No		AJ24	DQ24	DQ12	DQ6	DQ3
2K	46	VREFB2KN0	IO				LVDS2K_1p	No		AH24	DQ24	DQ12	DQ6	DQ3
2K	45	VREFB2KN0	IO				LVDS2K_2n	Yes		AG25	DQSn24	DQ12	DQ6	DQ3
2K	44	VREFB2KN0	IO				LVDS2K_2p	Yes		AH25	DQS24	DQ12	DQ6	DQ3
2K	43	VREFB2KN0	IO				LVDS2K_3n	No		AJ23	DQ24	DQ12	DQ6	DQ3
2K	42	VREFB2KN0	IO				LVDS2K_3p	No		AH23	DQ24	DQ12	DQ6	DQ3
2K	41	VREFB2KN0	IO				LVDS2K_4n	Yes		AF25	DQSn25	DQSn12/CQn12	DQ6	DQ3
2K	40	VREFB2KN0	IO				LVDS2K_4p	Yes		AF24	DQS25	DQS12/CQ12	DQ6	DQ3
2K	39	VREFB2KN0	IO				LVDS2K_5n	No		AF23	DQ25	DQ12	DQ6	DQ3
2K	38	VREFB2KN0	IO				LVDS2K_5p	No		AG23	DQ25	DQ12	DQ6	DQ3
2K	37	VREFB2KN0	IO				LVDS2K_6n	Yes		AD24	DQ25	DQ12	DQ6	DQ3
2K	36	VREFB2KN0	IO				LVDS2K_6p	Yes		AE24	DQ25	DQ12	DQ6	DQ3
2K	35	VREFB2KN0	IO				LVDS2K_7n	No		AK25	DQ26	DQ13	DQ6	DQ3
2K	34	VREFB2KN0	IO				LVDS2K_7p	No		AL25	DQ26	DQ13	DQ6	DQ3
2K	33	VREFB2KN0	IO				LVDS2K_8n	Yes		AN24	DQSn26	DQ13	DQSn6/CQn6	DQ3
2K	32	VREFB2KN0	IO				LVDS2K_8p	Yes		AP24	DQS26	DQ13	DQS6/CQ6	DQ3
2K	31	VREFB2KN0	IO				LVDS2K_9n	No		AK24	DQ26	DQ13	DQ6	DQ3
2K	30	VREFB2KN0	IO				LVDS2K_9p	No		AL24	DQ26	DQ13	DQ6	DQ3
2K	29	VREFB2KN0	IO	PLL_2K_CLKOUT1n			LVDS2K_10n	Yes		AM23	DQSn27	DQSn13/CQn13	DQ6	DQ3
2K	28	VREFB2KN0	IO	PLL_2K_CLKOUT1p,PLL_2K_CLKOUT1,PLL_2K_FB1			LVDS2K_10p	Yes		AL23	DQS27	DQS13/CQ13	DQ6	DQ3
2K	27	VREFB2KN0	IO				LVDS2K_11n	No		AM22	DQ27	DQ13	DQ6	DQ3
2K	26	VREFB2KN0	IO	RZQ_2K			LVDS2K_11p	No		AL22	DQ27	DQ13	DQ6	DQ3
2K	25	VREFB2KN0	IO	CLK_2K_1n			LVDS2K_12n	Yes		AN23	DQ27	DQ13	DQ6	DQ3
2K	24	VREFB2KN0	IO	CLK_2K_1p			LVDS2K_12p	Yes		AP23	DQ27	DQ13	DQ6	DQ3
2K	23	VREFB2KN0	IO	CLK_2K_0n			LVDS2K_13n	No		AG22	DQ28	DQ14	DQ7	DQ3
2K	22	VREFB2KN0	IO	CLK_2K_0p			LVDS2K_13p	No		AG21	DQ28	DQ14	DQ7	DQ3
2K	21	VREFB2KN0	IO				LVDS2K_14n	Yes		AD23	DQSn28	DQ14	DQ7	DQSn3/CQn3
2K	20	VREFB2KN0	IO				LVDS2K_14p	Yes		AD22	DQS28	DQ14	DQ7	DQS3/CQ3
2K	19	VREFB2KN0	IO	PLL_2K_CLKOUT0n			LVDS2K_15n	No		AH20	DQ28	DQ14	DQ7	DQ3
2K	18	VREFB2KN0	IO	PLL_2K_CLKOUT0p,PLL_2K_CLKOUT0,PLL_2K_FB0			LVDS2K_15p	No		AG20	DQ28	DQ14	DQ7	DQ3
2K	17	VREFB2KN0	IO				LVDS2K_16n	Yes		AE22	DQSn29	DQSn14/CQn14	DQ7	DQ3
2K	16	VREFB2KN0	IO				LVDS2K_16p	Yes		AF22	DQS29	DQS14/CQ14	DQ7	DQ3
2K	15	VREFB2KN0	IO				LVDS2K_17n	No		AF20	DQ29	DQ14	DQ7	DQ3
2K	14	VREFB2KN0	IO				LVDS2K_17p	No		AE20	DQ29	DQ14	DQ7	DQ3
2K	13	VREFB2KN0	IO				LVDS2K_18n	Yes		AD21	DQ29	DQ14	DQ7	DQ3
2K	12	VREFB2KN0	IO				LVDS2K_18p	Yes		AE21	DQ29	DQ14	DQ7	DQ3
2K	11	VREFB2KN0	IO				LVDS2K_19n	No		AP22	DQ30	DQ15	DQ7	DQ3
2K	10	VREFB2KN0	IO				LVDS2K_19p	No		AP21	DQ30	DQ15	DQ7	DQ3
2K	9	VREFB2KN0	IO				LVDS2K_20n	Yes		AJ22	DQSn30	DQ15	DQSn7/CQn7	DQ3
2K	8	VREFB2KN0	IO				LVDS2K_20p	Yes		AK22	DQS30	DQ15	DQS7/CQ7	DQ3
2K	7	VREFB2KN0	IO				LVDS2K_21n	No		AM21	DQ30	DQ15	DQ7	DQ3
2K	6	VREFB2KN0	IO				LVDS2K_21p	No		AN21	DQ30	DQ15	DQ7	DQ3
2K	5	VREFB2KN0	IO				LVDS2K_22n	Yes		AJ21	DQSn31	DQSn15/CQn15	DQ7	DQ3
2K	4	VREFB2KN0	IO				LVDS2K_22p	Yes		AH21	DQS31	DQS15/CQ15	DQ7	DQ3
2K	3	VREFB2KN0	IO				LVDS2K_23n	No		AM20	DQ31	DQ15	DQ7	DQ3
2K	2	VREFB2KN0	IO				LVDS2K_23p	No		AL20	DQ31	DQ15	DQ7	DQ3
2K	1	VREFB2KN0	IO				LVDS2K_24n	Yes		AK21	DQ31	DQ15	DQ7	DQ3
2K	0	VREFB2KN0	IO				LVDS2K_24p	Yes		AK20	DQ31	DQ15	DQ7	DQ3
3D		VREFB3DN0	IO	DIFF_3D_1n						M5				
3D		VREFB3DN0	IO	DIFF_3D_1p						M6				
3D		VREFB3DN0	IO	DIFF_3D_2n						L8				
3D		VREFB3DN0	IO	DIFF_3D_2p						K7				
3D		VREFB3DN0	IO	DIFF_3D_3n						M3				
3D		VREFB3DN0	IO	DIFF_3D_3p						N3				
3D		VREFB3DN0	IO	DIFF_3D_4n						L7				
3D		VREFB3DN0	IO	DIFF_3D_4p						M7				
3D		VREFB3DN0	IO	DIFF_3D_5n						N1				
3D		VREFB3DN0	IO	DIFF_3D_5p						M1				
3D		VREFB3DN0	IO	DIFF_3D_6n						H5				
3D		VREFB3DN0	IO	DIFF_3D_6p						G5				
3D		VREFB3DN0	IO	DIFF_3D_7n						N5				
3D		VREFB3DN0	IO	DIFF_3D_7p						N4				
3D		VREFB3DN0	IO	DIFF_3D_8n						J6				
3D		VREFB3DN0	IO	DIFF_3D_8p						K5				
3D		VREFB3DN0	IO	DIFF_3D_9n						P1				
3D		VREFB3DN0	IO	DIFF_3D_9p						P2				
3D		VREFB3DN0	IO	PLL_3D_CLKOUT1n			LVDS3D_10n	Yes		K6				
3D		VREFB3DN0	IO	PLL_3D_CLKOUT1p,PLL_3D_CLKOUT1,PLL_3D_FB1			LVDS3D_10p	Yes		L5				
3D		VREFB3DN0	IO	DIFF_3D_11n						P3				
3D		VREFB3DN0	IO	RZQ_3D,DIFF_3D_11p						P4				
3D		VREFB3DN0	IO	CLK_3D_1n			LVDS3D_12n	Yes		H4				
3D		VREFB3DN0	IO	CLK_3D_1p			LVDS3D_12p	Yes		H3				
3D		VREFB3DN0	IO	CLK_3D_0n			LVDS3D_13n	No		R1				
3D		VREFB3DN0	IO	CLK_3D_0p			LVDS3D_13p	No		R2				
3D		VREFB3DN0	IO	DIFF_3D_14n						K4				
3D		VREFB3DN0	IO	DIFF_3D_14p						J4				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
3D		VREFB3DN0	IO	PLL_3D_CLKOUT0n			LVDS3D_15n	No		R4				
3D		VREFB3DN0	IO	PLL_3D_CLKOUT0p,PLL_3D_CLKOUT0,PLL_3D_FB0			LVDS3D_15p	No		R5				
3B	47	VREFB3BN0	IO				LVDS3B_1n	No		AF5	DQ48	DQ24	DQ12	DQ6
3B	46	VREFB3BN0	IO				LVDS3B_1p	No		AG5	DQ48	DQ24	DQ12	DQ6
3B	45	VREFB3BN0	IO				LVDS3B_2n	Yes		AJ4	DQSn48	DQ24	DQ12	DQ6
3B	44	VREFB3BN0	IO				LVDS3B_2p	Yes		AK4	DQS48	DQ24	DQ12	DQ6
3B	43	VREFB3BN0	IO				LVDS3B_3n	No		AH4	DQ48	DQ24	DQ12	DQ6
3B	42	VREFB3BN0	IO				LVDS3B_3p	No		AH5	DQ48	DQ24	DQ12	DQ6
3B	41	VREFB3BN0	IO				LVDS3B_4n	Yes		AK6	DQSn49	DQSn24/CQn24	DQ12	DQ6
3B	40	VREFB3BN0	IO				LVDS3B_4p	Yes		AJ6	DQS49	DQS24/CQ24	DQ12	DQ6
3B	39	VREFB3BN0	IO				LVDS3B_5n	No		AE6	DQ49	DQ24	DQ12	DQ6
3B	38	VREFB3BN0	IO				LVDS3B_5p	No		AD6	DQ49	DQ24	DQ12	DQ6
3B	37	VREFB3BN0	IO				LVDS3B_6n	Yes		AG6	DQ49	DQ24	DQ12	DQ6
3B	36	VREFB3BN0	IO				LVDS3B_6p	Yes		AH6	DQ49	DQ24	DQ12	DQ6
3B	35	VREFB3BN0	IO				LVDS3B_7n	No		AL3	DQ50	DQ25	DQ12	DQ6
3B	34	VREFB3BN0	IO				LVDS3B_7p	No		AM3	DQ50	DQ25	DQ12	DQ6
3B	33	VREFB3BN0	IO				LVDS3B_8n	Yes		AK5	DQSn50	DQ25	DQSn12/CQn12	DQ6
3B	32	VREFB3BN0	IO				LVDS3B_8p	Yes		AL4	DQS50	DQ25	DQS12/CQ12	DQ6
3B	31	VREFB3BN0	IO				LVDS3B_9n	No		AN3	DQ50	DQ25	DQ12	DQ6
3B	30	VREFB3BN0	IO				LVDS3B_9p	No		AP3	DQ50	DQ25	DQ12	DQ6
3B	29	VREFB3BN0	IO	PLL_3B_CLKOUT1n			LVDS3B_10n	Yes		AL5	DQSn51	DQSn25/CQn25	DQ12	DQ6
3B	28	VREFB3BN0	IO	PLL_3B_CLKOUT1p,PLL_3B_CLKOUT1,PLL_3B_FB1			LVDS3B_10p	Yes		AM5	DQS51	DQS25/CQ25	DQ12	DQ6
3B	27	VREFB3BN0	IO				LVDS3B_11n	No		AN5	DQ51	DQ25	DQ12	DQ6
3B	26	VREFB3BN0	IO	RZQ_3B			LVDS3B_11p	No		AP6	DQ51	DQ25	DQ12	DQ6
3B	25	VREFB3BN0	IO	CLK_3B_1n			LVDS3B_12n	Yes		AN4	DQ51	DQ25	DQ12	DQ6
3B	24	VREFB3BN0	IO	CLK_3B_1p			LVDS3B_12p	Yes		AP4	DQ51	DQ25	DQ12	DQ6
3B	23	VREFB3BN0	IO	CLK_3B_0n			LVDS3B_13n	No		AL7	DQ52	DQ26	DQ13	DQ6
3B	22	VREFB3BN0	IO	CLK_3B_0p			LVDS3B_13p	No		AM6	DQ52	DQ26	DQ13	DQ6
3B	21	VREFB3BN0	IO				LVDS3B_14n	Yes		AP7	DQSn52	DQ26	DQ13	DQSn6/CQn6
3B	20	VREFB3BN0	IO				LVDS3B_14p	Yes		AN6	DQS52	DQ26	DQ13	DQS6/CQ6
3B	19	VREFB3BN0	IO	PLL_3B_CLKOUT0n			LVDS3B_15n	No		AP9	DQ52	DQ26	DQ13	DQ6
3B	18	VREFB3BN0	IO	PLL_3B_CLKOUT0p,PLL_3B_CLKOUT0,PLL_3B_FB0			LVDS3B_15p	No		AN9	DQ52	DQ26	DQ13	DQ6
3B	17	VREFB3BN0	IO				LVDS3B_16n	Yes		AL8	DQSn53	DQSn26/CQn26	DQ13	DQ6
3B	16	VREFB3BN0	IO				LVDS3B_16p	Yes		AM7	DQS53	DQS26/CQ26	DQ13	DQ6
3B	15	VREFB3BN0	IO				LVDS3B_17n	No		AM8	DQ53	DQ26	DQ13	DQ6
3B	14	VREFB3BN0	IO				LVDS3B_17p	No		AL9	DQ53	DQ26	DQ13	DQ6
3B	13	VREFB3BN0	IO				LVDS3B_18n	Yes		AN8	DQ53	DQ26	DQ13	DQ6
3B	12	VREFB3BN0	IO				LVDS3B_18p	Yes		AP8	DQ53	DQ26	DQ13	DQ6
3B	11	VREFB3BN0	IO				LVDS3B_19n	No		AJ7	DQ54	DQ27	DQ13	DQ6
3B	10	VREFB3BN0	IO				LVDS3B_19p	No		AK7	DQ54	DQ27	DQ13	DQ6
3B	9	VREFB3BN0	IO				LVDS3B_20n	Yes		AD7	DQSn54	DQ27	DQSn13/CQn13	DQ6
3B	8	VREFB3BN0	IO				LVDS3B_20p	Yes		AE7	DQS54	DQ27	DQS13/CQ13	DQ6
3B	7	VREFB3BN0	IO				LVDS3B_21n	No		AJ8	DQ54	DQ27	DQ13	DQ6
3B	6	VREFB3BN0	IO				LVDS3B_21p	No		AH8	DQ54	DQ27	DQ13	DQ6
3B	5	VREFB3BN0	IO				LVDS3B_22n	Yes		AF7	DQSn55	DQSn27/CQn27	DQ13	DQ6
3B	4	VREFB3BN0	IO				LVDS3B_22p	Yes		AG7	DQS55	DQS27/CQ27	DQ13	DQ6
3B	3	VREFB3BN0	IO				LVDS3B_23n	No		AD8	DQ55	DQ27	DQ13	DQ6
3B	2	VREFB3BN0	IO				LVDS3B_23p	No		AD9	DQ55	DQ27	DQ13	DQ6
3B	1	VREFB3BN0	IO				LVDS3B_24n	Yes		AG8	DQ55	DQ27	DQ13	DQ6
3B	0	VREFB3BN0	IO				LVDS3B_24p	Yes		AF8	DQ55	DQ27	DQ13	DQ6
3A		VREFB3AN0	IO	DIFF_3A_1n	AVST_DATA0					AK9				
3A		VREFB3AN0	IO	DIFF_3A_1p	AVST_DATA1					AK10				
3A		VREFB3AN0	IO	DIFF_3A_2n	AVST_DATA2					AH9				
3A		VREFB3AN0	IO	DIFF_3A_2p	AVST_DATA3					AJ9				
3A		VREFB3AN0	IO	DIFF_3A_3n	AVST_DATA4					AL10				
3A		VREFB3AN0	IO	DIFF_3A_3p	AVST_DATA5					AM10				
3A		VREFB3AN0	IO	DIFF_3A_4n	AVST_DATA6					AK11				
3A		VREFB3AN0	IO	DIFF_3A_4p	AVST_DATA7					AJ11				
3A		VREFB3AN0	IO	DIFF_3A_5n	AVST_DATA8					AP11				
3A		VREFB3AN0	IO	DIFF_3A_5p	AVST_DATA9					AN10				
3A		VREFB3AN0	IO	DIFF_3A_6n	AVST_DATA10					AJ12				
3A		VREFB3AN0	IO	DIFF_3A_6p	AVST_DATA11					AK12				
3A		VREFB3AN0	IO	DIFF_3A_7n	AVST_DATA12					AG10				
3A		VREFB3AN0	IO	DIFF_3A_7p	AVST_DATA13					AH10				
3A		VREFB3AN0	IO	DIFF_3A_8n	AVST_DATA14					AE9				
3A		VREFB3AN0	IO	DIFF_3A_8p	AVST_DATA15					AF9				
3A		VREFB3AN0	IO	DIFF_3A_9n	AVST_DATA16					AH11				
3A		VREFB3AN0	IO	DIFF_3A_9p	AVST_DATA17					AG11				
3A		VREFB3AN0	IO	PLL_3A_CLKOUT1n	AVST_DATA18		LVDS3A_10n	Yes		AE10				
3A		VREFB3AN0	IO	PLL_3A_CLKOUT1p,PLL_3A_CLKOUT1,PLL_3A_FB1	AVST_DATA19		LVDS3A_10p	Yes		AF10				
3A		VREFB3AN0	IO	DIFF_3A_11n						AG12				
3A		VREFB3AN0	IO	RZQ_3A,DIFF_3A_11p	AVST_VALID					AF12				
3A		VREFB3AN0	IO	CLK_3A_1n	AVST_DATA20		LVDS3A_12n	Yes		AE11				
3A		VREFB3AN0	IO	CLK_3A_1p	AVST_DATA21		LVDS3A_12p	Yes		AD11				
3A		VREFB3AN0	IO	CLK_3A_0n	AVST_DATA22		LVDS3A_13n	No		AP13				
3A		VREFB3AN0	IO	CLK_3A_0p	AVST_DATA23		LVDS3A_13p	No		AN13				
3A		VREFB3AN0	IO	DIFF_3A_14n	AVST_DATA24					AM11				
3A		VREFB3AN0	IO	DIFF_3A_14p	AVST_DATA25					AL12				
3A		VREFB3AN0	IO	PLL_3A_CLKOUT0n	AVST_DATA26		LVDS3A_15n	No		AP14				
3A		VREFB3AN0	IO	PLL_3A_CLKOUT0p,PLL_3A_CLKOUT0,PLL_3A_FB0	AVST_DATA27		LVDS3A_15p	No		AN14				
3A		VREFB3AN0	IO	DIFF_3A_16n	AVST_DATA28					AL13				
3A		VREFB3AN0	IO	DIFF_3A_16p	AVST_DATA29					AM12				
3A		VREFB3AN0	IO	DIFF_3A_17n	AVST_DATA30					AM13				
3A		VREFB3AN0	IO	DIFF_3A_17p	AVST_DATA31					AL14				
3A		VREFB3AN0	IO	DIFF_3A_18n						AP12				
3A		VREFB3AN0	IO	DIFF_3A_18p						AN11				
3A		VREFB3AN0	IO	DIFF_3A_19n						AG13				
3A		VREFB3AN0	IO	DIFF_3A_19p						AH14				
3A		VREFB3AN0	IO	DIFF_3A_20n						AF13				
3A		VREFB3AN0	IO	DIFF_3A_20p						AE12				
3A		VREFB3AN0	IO	DIFF_3A_21n						AF14				
3A		VREFB3AN0	IO	DIFF_3A_21p						AE14				
3A		VREFB3AN0	IO	DIFF_3A_22n						AH13				
3A		VREFB3AN0	IO	DIFF_3A_22p						AJ13				
3A		VREFB3AN0	IO	DIFF_3A_23n						AD13				
3A		VREFB3AN0	IO	DIFF_3A_23p						AD14				
3A		VREFB3AN0	IO	DIFF_3A_24n						AK14				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
3A		VREFB3AN0	IO	DIFF_3A_24p	AVST_CLK					AJ14				
HPS			HPS_IOA_1	GPIO0_IO0,SPIM0_SS1_N,SPIS0_CLK,UART0_CTS_N,NAND_ADQ0,USB0_CLK,SDMMC_CCLK		HPS_IOA_1				C5				
HPS			HPS_IOA_2	GPIO0_IO1,SPIM1_SS1_N,SPIS0_MOSI,UART0_RTS_N,NAND_ADQ1,USB0_STP,SDMMC_CMD		HPS_IOA_2				D4				
HPS			HPS_IOA_3	GPIO0_IO2,SPIS0_SS0_N,UART0_TX,I2C1_SDA,NAND_WE_N,USB0_DIR,SDMMC_DATA0		HPS_IOA_3				C8				
HPS			HPS_IOA_4	GPIO0_IO3,SPIS0_MISO,UART0_RX,I2C1_SCL,NAND_RE_N,USB0_DATA0,SDMMC_DATA1		HPS_IOA_4				E4				
HPS			HPS_IOA_5	GPIO0_IO4,SPIM0_CLK,UART1_CTS_N,I2C0_SDA,NAND_WP_N,USB0_DATA1,SDMMC_DATA2		HPS_IOA_5				D1				
HPS			HPS_IOA_6	GPIO0_IO5,SPIM0_MOSI,UART1_RTS_N,I2C0_SCL,NAND_ADQ2,USB0_NXT,SDMMC_DATA3		HPS_IOA_6				C1				
HPS			HPS_IOA_7	GPIO0_IO6,SPIM0_MISO,MDIO2_MDIO,UART1_TX,I2C_EMAC2_SDA,NAND_ADQ3,USB0_DATA2,SDMMC_DATA4		HPS_IOA_7				D3				
HPS			HPS_IOA_8	GPIO0_IO7,SPIM0_SS0_N,MDIO2_MDC,UART1_RX,I2C_EMAC2_SCL,NAND_CLE,USB0_DATA3,SDMMC_DATA5		HPS_IOA_8				B3				
HPS			HPS_IOA_9	GPIO0_IO8,SPIM1_CLK,SPIS1_CLK,MDIO1_MDIO,I2C_EMAC1_SDA,NAND_ADQ4,USB0_DATA4,SDMMC_DATA6		HPS_IOA_9				C3				
HPS			HPS_IOA_10	GPIO0_IO9,SPIM1_MOSI,SPIS1_MOSI,MDIO1_MDC,I2C_EMAC1_SCL,NAND_ADQ5,USB0_DATA5,SDMMC_DATA7		HPS_IOA_10				B2				
HPS			HPS_IOA_11	GPIO0_IO10,SPIM1_MISO,SPIS1_SS0_N,MDIO0_MDIO,I2C_EMAC0_SDA,NAND_ADQ6,USB0_DATA6		HPS_IOA_11				B6				
HPS			HPS_IOA_12	GPIO0_IO11,SPIM1_SS0_N,SPIS1_MISO,MDIO0_MDC,I2C_EMAC0_SCL,NAND_ADQ7,USB0_DATA7		HPS_IOA_12				D6				
HPS			HPS_IOA_13	GPIO0_IO12,NAND_ALE,USB1_CLK,EMAC0_TX_CLK		HPS_IOA_13				A4				
HPS			HPS_IOA_14	GPIO0_IO13,NAND_RB,USB1_STP,EMAC0_TX_CTL		HPS_IOA_14				B5				
HPS			HPS_IOA_15	GPIO0_IO14,NAND_CE_N,USB1_DIR,EMAC0_RX_CLK		HPS_IOA_15				D2				
HPS			HPS_IOA_16	GPIO0_IO15,USB1_DATA0,EMAC0_RX_CTL		HPS_IOA_16				A5				
HPS			HPS_IOA_17	GPIO0_IO16,NAND_ADQ8,USB1_DATA1,EMAC0_TXD0		HPS_IOA_17				D7				
HPS			HPS_IOA_18	GPIO0_IO17,NAND_ADQ9,USB1_NXT,EMAC0_TXD1		HPS_IOA_18				B7				
HPS			HPS_IOA_19	GPIO0_IO18,NAND_ADQ10,USB1_DATA2,EMAC0_RXD0		HPS_IOA_19				G6				
HPS			HPS_IOA_20	GPIO0_IO19,SPIM1_SS1_N,NAND_ADQ11,USB1_DATA3,EMAC0_RXD1		HPS_IOA_20				A3				
HPS			HPS_IOA_21	GPIO0_IO20,SPIM1_CLK,SPIS0_CLK,UART0_CTS_N,I2C1_SDA,NAND_ADQ12,USB1_DATA4,EMAC0_TXD2		HPS_IOA_21				C6				
HPS			HPS_IOA_22	GPIO0_IO21,SPIM1_MOSI,SPIS0_MOSI,UART0_RTS_N,I2C1_SCL,NAND_ADQ13,USB1_DATA5,EMAC0_TXD3		HPS_IOA_22				G2				
HPS			HPS_IOA_23	GPIO0_IO22,SPIM1_MISO,SPIS0_SS0_N,UART0_TX,I2C0_SDA,NAND_ADQ14,USB1_DATA6,EMAC0_RXD2		HPS_IOA_23				A7				
HPS			HPS_IOA_24	GPIO0_IO23,SPIM1_SS0_N,SPIS0_MISO,UART0_RX,I2C0_SCL,NAND_ADQ15,USB1_DATA7,EMAC0_RXD3		HPS_IOA_24				G8				
HPS			HPS_IOB_1	GPIO1_IO0,SPIM1_CLK,UART0_CTS_N,NAND_ADQ0,EMAC1_TX_CLK		HPS_IOB_1				F5				
HPS			HPS_IOB_2	GPIO1_IO1,SPIM1_MOSI,UART0_RTS_N,NAND_ADQ1,EMAC1_TX_CTL		HPS_IOB_2				G7				
HPS			HPS_IOB_3	GPIO1_IO2,SPIM1_MISO,UART0_TX,I2C0_SDA,NAND_WE_N,EMAC1_RX_CLK		HPS_IOB_3				E4				
HPS			HPS_IOB_4	GPIO1_IO3,SPIM1_SS0_N,UART0_RX,I2C0_SCL,NAND_RE_N,EMAC1_RX_CTL		HPS_IOB_4				F3				
HPS			HPS_IOB_5	GPIO1_IO4,SPIM1_SS1_N,SPIS1_CLK,UART1_CTS_N,NAND_WP_N,EMAC1_TXD0		HPS_IOB_5				G1				
HPS			HPS_IOB_6	GPIO1_IO5,SPIS1_MOSI,UART1_RTS_N,NAND_ADQ2,EMAC1_TXD1		HPS_IOB_6				F9				
HPS			HPS_IOB_7	GPIO1_IO6,SPIS1_SS0_N,UART1_TX,I2C1_SDA,NAND_ADQ3,EMAC1_RXD0		HPS_IOB_7				H6				
HPS			HPS_IOB_8	GPIO1_IO7,SPIS1_MISO,UART1_RX,I2C1_SCL,NAND_CLE,EMAC1_RXD1		HPS_IOB_8				E1				
HPS			HPS_IOB_9	GPIO1_IO8,JTAG_TCK,SPIS0_CLK,MDIO2_MDIO,I2C_EMAC2_SDA,NAND_ADQ4,EMAC1_TXD2		HPS_IOB_9				F8				
HPS			HPS_IOB_10	GPIO1_IO9,JTAG_TMS,SPIS0_MOSI,MDIO2_MDC,I2C_EMAC2_SCL,NAND_ADQ5,EMAC1_TXD3		HPS_IOB_10				E7				
HPS			HPS_IOB_11	GPIO1_IO10,JTAG_TDO,SPIS0_SS0_N,MDIO0_MDIO,I2C_EMAC0_SDA,NAND_ADQ6,EMAC1_RXD2		HPS_IOB_11				F4				
HPS			HPS_IOB_12	GPIO1_IO11,JTAG_TDI,SPIS0_MISO,MDIO0_MDC,I2C_EMAC0_SCL,NAND_ADQ7,EMAC1_RXD3		HPS_IOB_12				H9				
HPS			HPS_IOB_13	GPIO1_IO12,I2C1_SDA,NAND_ALE,SDMMC_DATA0,EMAC2_TX_CLK		HPS_IOB_13				D8				
HPS			HPS_IOB_14	GPIO1_IO13,I2C1_SCL,NAND_RB,SDMMC_CMD,EMAC2_TX_CTL		HPS_IOB_14				F2				
HPS			HPS_IOB_15	GPIO1_IO14,UART1_TX,NAND_CE_N,SDMMC_CCLK,EMAC2_RX_CLK		HPS_IOB_15				J9				
HPS			HPS_IOB_16	GPIO1_IO15,UART1_RX,SDMMC_DATA1,EMAC2_RX_CTL		HPS_IOB_16				E2				
HPS			HPS_IOB_17	GPIO1_IO16,UART1_CTS_N,NAND_ADQ8,SDMMC_DATA2,EMAC2_TXD0		HPS_IOB_17				F7				
HPS			HPS_IOB_18	GPIO1_IO17,SPIM0_SS1_N,UART1_RTS_N,NAND_ADQ9,SDMMC_DATA3,EMAC2_TXD1		HPS_IOB_18				E5				
HPS			HPS_IOB_19	GPIO1_IO18,SPIM0_MISO,MDIO1_MDIO,I2C_EMAC1_SDA,NAND_ADQ10,SDMMC_DATA4,EMAC2_RXD0		HPS_IOB_19				J7				
HPS			HPS_IOB_20	GPIO1_IO19,SPIM0_SS0_N,MDIO1_MDC,I2C_EMAC1_SCL,NAND_ADQ11,SDMMC_DATA5,EMAC2_RXD1		HPS_IOB_20				E6				
HPS			HPS_IOB_21	GPIO1_IO20,SPIM0_CLK,SPIS1_CLK,I2C_EMAC2_SDA,NAND_ADQ12,SDMMC_DATA6,EMAC2_TXD2		HPS_IOB_21				G3				
HPS			HPS_IOB_22	GPIO1_IO21,SPIM0_MOSI,SPIS1_MOSI,I2C_EMAC2_SCL,NAND_ADQ13,SDMMC_DATA7,EMAC2_TXD3		HPS_IOB_22				K9				
HPS			HPS_IOB_23	GPIO1_IO22,SPIM0_MISO,SPIS1_SS0_N,MDIO0_MDIO,I2C_EMAC0_SDA,NAND_ADQ14,EMAC2_RXD2		HPS_IOB_23				E9				
HPS			HPS_IOB_24	GPIO1_IO23,SPIM0_SS0_N,SPIS1_MISO,MDIO0_MDC,I2C_EMAC0_SCL,NAND_ADQ15,EMAC2_RXD3		HPS_IOB_24				K10				
SDM			TDO							AL18				
SDM			TMS							AL19				
SDM			TCK							AL17				
SDM			TDI							AL15				
SDM			OSC_CLK_1							AE17				
SDM			SDM_IO0	PWRMGT_SCL						AE19				
SDM			SDM_IO1	AVSTx8_DATA2,AS_DATA1						AG18				
SDM			SDM_IO5	AS_nCSO0,MSEL0						AF17				
SDM			SDM_IO3	AVSTx8_DATA3,AS_DATA2						AH18				
SDM			nCONFIG							AK19				
SDM			SDM_IO4	AVSTx8_DATA1,AS_DATA0						AJ19				
SDM			SDM_IO2	AVSTx8_DATA0,AS_CLK						AF19				
SDM			SDM_IO7	AS_nCSO2,MSEL1						AG17				
SDM			SDM_IO11	AVSTx8_VALID,PWRMGT_SDA						AK15				
SDM			nSTATUS							AH15				
SDM			SDM_IO16	PWRMGT_SDA						AG15				
SDM			SDM_IO13	AVSTx8_DATA5						AJ16				
SDM			SDM_IO9	AS_nCSO1,MSEL2						AK16				
SDM			SDM_IO6	AVSTx8_DATA4,AS_DATA3						AF18				
SDM			SDM_IO10	AVSTx8_DATA7						AH16				
SDM			SDM_IO8	AVST_READY,AS_nCSO3						AJ17				
SDM			SDM_IO12	PWRMGT_SDA						AG16				
SDM			SDM_IO15	AVSTx8_DATA6						AH19				
SDM			SDM_IO14	AVSTx8_CLK,PWRMGT_SCL						AK17				
SDM			RREF_SDM							AP19				
SDM			VSIGP_0							AM18				
SDM			VSIGN_0							AM17				
SDM			VSIGP_1							AP17				
SDM			VSIGN_1							AP16				
			GND							T4				
			GND							T5				
			GND							AJ18				
			GND							AN16				
			GND							AM16				
			GND							Y8				
			GND							Y32				
			GND							Y31				
			GND							Y3				
			GND							Y25				
			GND							Y23				
			GND							Y18				
			GND							Y13				
			GND							W5				
			GND							W34				
			GND							W33				
			GND							W30				
			GND							W29				
			GND							W26				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
			GND							W25				
			GND							W20				
			GND							W15				
			GND							W10				
			GND							V7				
			GND							V32				
			GND							V31				
			GND							V25				
			GND							V22				
			GND							V2				
			GND							V17				
			GND							V12				
			GND							U9				
			GND							U4				
			GND							U34				
			GND							U33				
			GND							U30				
			GND							U29				
			GND							U26				
			GND							U25				
			GND							U24				
			GND							U19				
			GND							U14				
			GND							T6				
			GND							T32				
			GND							T31				
			GND							T25				
			GND							T21				
			GND							T16				
			GND							T11				
			GND							T1				
			GND							R8				
			GND							R34				
			GND							R33				
			GND							R30				
			GND							R3				
			GND							R29				
			GND							R26				
			GND							R25				
			GND							R23				
			GND							R18				
			GND							R13				
			GND							P5				
			GND							P32				
			GND							P31				
			GND							P25				
			GND							P20				
			GND							P15				
			GND							P10				
			GND							N7				
			GND							N34				
			GND							N33				
			GND							N30				
			GND							N29				
			GND							N26				
			GND							N25				
			GND							N22				
			GND							N2				
			GND							N17				
			GND							N12				
			GND							M9				
			GND							M4				
			GND							M32				
			GND							M31				
			GND							M25				
			GND							M24				
			GND							M19				
			GND							M14				
			GND							L6				
			GND							L34				
			GND							L33				
			GND							L30				
			GND							L29				
			GND							L26				
			GND							L25				
			GND							L21				
			GND							L16				
			GND							L11				
			GND							L1				
			GND							K8				
			GND							K32				
			GND							K31				
			GND							K3				
			GND							K25				
			GND							K23				
			GND							K18				
			GND							K13				
			GND							J5				
			GND							J34				
			GND							J33				
			GND							J30				
			GND							J29				
			GND							J28				
			GND							J27				
			GND							J26				
			GND							J25				
			GND							J20				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
			GND							J15				
			GND							J10				
			GND							H7				
			GND							H32				
			GND							H31				
			GND							H28				
			GND							H27				
			GND							H22				
			GND							H2				
			GND							H17				
			GND							H12				
			GND							G9				
			GND							G4				
			GND							G34				
			GND							G33				
			GND							G30				
			GND							G29				
			GND							G28				
			GND							G24				
			GND							G19				
			GND							G14				
			GND							F6				
			GND							F32				
			GND							F31				
			GND							F28				
			GND							F26				
			GND							F21				
			GND							F16				
			GND							F11				
			GND							F1				
			GND							E8				
			GND							E34				
			GND							E33				
			GND							E30				
			GND							E3				
			GND							E29				
			GND							E28				
			GND							E23				
			GND							E18				
			GND							E13				
			GND							D5				
			GND							D32				
			GND							D31				
			GND							D28				
			GND							D25				
			GND							D20				
			GND							D15				
			GND							D10				
			GND							C7				
			GND							C34				
			GND							C33				
			GND							C30				
			GND							C29				
			GND							C28				
			GND							C27				
			GND							C22				
			GND							C2				
			GND							C17				
			GND							C12				
			GND							B9				
			GND							B4				
			GND							B34				
			GND							B33				
			GND							B32				
			GND							B31				
			GND							B28				
			GND							B24				
			GND							B19				
			GND							B14				
			GND							B1				
			GND							AP5				
			GND							AP33				
			GND							AP32				
			GND							AP31				
			GND							AP30				
			GND							AP25				
			GND							AP20				
			GND							AP2				
			GND							AP15				
			GND							AP10				
			GND							AN7				
			GND							AN34				
			GND							AN33				
			GND							AN30				
			GND							AN29				
			GND							AN28				
			GND							AN27				
			GND							AN22				
			GND							AN2				
			GND							AN17				
			GND							AN12				
			GND							AN1				
			GND							AM9				
			GND							AM4				
			GND							AM32				
			GND							AM31				
			GND							AM28				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
			GND							AM24				
			GND							AM19				
			GND							AM14				
			GND							AL6				
			GND							AL34				
			GND							AL33				
			GND							AL30				
			GND							AL29				
			GND							AL28				
			GND							AL26				
			GND							AL21				
			GND							AL16				
			GND							AL11				
			GND							AL1				
			GND							AK8				
			GND							AK32				
			GND							AK31				
			GND							AK3				
			GND							AK28				
			GND							AK23				
			GND							AK18				
			GND							AK13				
			GND							AJ5				
			GND							AJ34				
			GND							AJ33				
			GND							AJ30				
			GND							AJ29				
			GND							AJ28				
			GND							AJ25				
			GND							AJ20				
			GND							AJ15				
			GND							AJ10				
			GND							AH7				
			GND							AH32				
			GND							AH31				
			GND							AH28				
			GND							AH27				
			GND							AH22				
			GND							AH2				
			GND							AH17				
			GND							AH12				
			GND							AG9				
			GND							AG4				
			GND							AG34				
			GND							AG33				
			GND							AG30				
			GND							AG29				
			GND							AG28				
			GND							AG24				
			GND							AG19				
			GND							AG14				
			GND							AF6				
			GND							AF32				
			GND							AF31				
			GND							AF28				
			GND							AF27				
			GND							AF26				
			GND							AF21				
			GND							AF16				
			GND							AF11				
			GND							AF1				
			GND							AE8				
			GND							AE34				
			GND							AE33				
			GND							AE30				
			GND							AE3				
			GND							AE29				
			GND							AE26				
			GND							AE25				
			GND							AE23				
			GND							AE18				
			GND							AE13				
			GND							AD5				
			GND							AD32				
			GND							AD31				
			GND							AD25				
			GND							AD20				
			GND							AD15				
			GND							AD10				
			GND							AC7				
			GND							AC34				
			GND							AC33				
			GND							AC30				
			GND							AC29				
			GND							AC26				
			GND							AC25				
			GND							AC22				
			GND							AC2				
			GND							AC17				
			GND							AC12				
			GND							AB9				
			GND							AB4				
			GND							AB32				
			GND							AB31				
			GND							AB25				
			GND							AB24				
			GND							AB19				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
			GND							AB14				
			GND							AA6				
			GND							AA34				
			GND							AA33				
			GND							AA30				
			GND							AA29				
			GND							AA26				
			GND							AA25				
			GND							AA21				
			GND							AA16				
			GND							AA11				
			GND							AA1				
			GND							A6				
			GND							A33				
			GND							A30				
			GND							A29				
			GND							A28				
			GND							A26				
			GND							A21				
			GND							A2				
			GND							A16				
			GND							A11				
			GNDSENSE							T14				
			VCC							Y9				
			VCC							Y7				
			VCC							Y22				
			VCC							Y21				
			VCC							Y20				
			VCC							Y19				
			VCC							Y17				
			VCC							Y16				
			VCC							Y15				
			VCC							Y14				
			VCC							Y12				
			VCC							Y10				
			VCC							W9				
			VCC							W8				
			VCC							W7				
			VCC							W22				
			VCC							W21				
			VCC							W19				
			VCC							W18				
			VCC							W17				
			VCC							W16				
			VCC							W14				
			VCC							W13				
			VCC							W12				
			VCC							W11				
			VCC							U7				
			VCC							U22				
			VCC							T9				
			VCC							T8				
			VCC							T7				
			VCC							T22				
			VCC							T20				
			VCC							T19				
			VCC							T18				
			VCC							T17				
			VCC							T13				
			VCC							T12				
			VCC							T10				
			VCC							R9				
			VCC							R7				
			VCC							R22				
			VCC							R21				
			VCC							R20				
			VCC							R19				
			VCC							R17				
			VCC							R16				
			VCC							R15				
			VCC							R14				
			VCC							R12				
			VCC							R11				
			VCC							R10				
			VCC							P9				
			VCC							P8				
			VCC							P7				
			VCC							P22				
			VCC							P21				
			VCC							P19				
			VCC							P17				
			VCC							P16				
			VCC							P14				
			VCC							P13				
			VCC							P12				
			VCC							N9				
			VCC							N8				
			VCC							N21				
			VCC							N19				
			VCC							N15				
			VCC							N14				
			VCC							AB8				
			VCC							AB7				
			VCC							AB22				
			VCC							AB21				
			VCC							AB17				
			VCC							AB15				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
			VCC							AB12				
			VCC							AA9				
			VCC							AA8				
			VCC							AA7				
			VCC							AA22				
			VCC							AA20				
			VCC							AA19				
			VCC							AA17				
			VCC							AA15				
			VCC							AA14				
			VCC							AA13				
			VCC							AA12				
			VCC							AA10				
			VCCPT							V9				
			VCCPT							V8				
			VCCPT							V21				
			VCCPT							V20				
			VCCPT							V19				
			VCCPT							V18				
			VCCPT							V16				
			VCCPT							V13				
			VCCPT							V11				
			VCCPT							V10				
			VCCPT							U8				
			VCCPT							U21				
			VCCPT							U20				
			VCCPT							U18				
			VCCPT							U17				
			VCCPT							U16				
			VCCPT							U15				
			VCCPT							U13				
			VCCPT							U12				
			VCCPT							U11				
			VCCPT							U10				
			DNU							AG27				
			DNU							AN25				
			DNU							AM25				
			DNU							J8				
			DNU							H8				
			DNU							AP18				
			DNU							AN19				
			DNU							AN18				
			DNU							AN20				
			DNU							AP28				
			DNU							AP27				
			TEMPDIODE0n							AN15				
			TEMPDIODE0p							AM15				
			TEMPDIODE1n							AJ27				
			TEMPDIODE1p							AH26				
			VCCBAT							AE15				
			VCCA_PLL							V15				
			VCCA_PLL							V14				
			VCCIO2K							AD19				
			VCCIO2K							AC20				
			VCCIO2K							AC19				
			VCCIO2L							M21				
			VCCIO2L							M20				
			VCCIO2L							L20				
			VCCIO2M							M18				
			VCCIO2M							L19				
			VCCIO2M							L18				
			VCCIO2N							M17				
			VCCIO2N							M16				
			VCCIO2N							L17				
			VCCIO3A							AD12				
			VCCIO3A							AC14				
			VCCIO3A							AC13				
			VCCIO3B							AC9				
			VCCIO3B							AC8				
			VCCIO3B							AC10				
			VCCIO3C							W6				
			VCCIO3C							V6				
			VCCIO3C							V5				
			VCCIO3D							M10				
			VCCIO3D							L9				
			VCCIO3D							L10				
			VCCIO3V							AC24				
			VCCIO3V							AC23				
			VCCIO_HPS							M12				
			VCCIO_HPS							M11				
			VCCIO_SDM							AD16				
2K		VREFB2KN0	VREFB2KN0							AC21				
2L		VREFB2LN0	VREFB2LN0							K20				
2M		VREFB2MN0	VREFB2MN0							K19				
2N		VREFB2NN0	VREFB2NN0							M15				
3A		VREFB3AN0	VREFB3AN0							AC15				
3B		VREFB3BN0	VREFB3BN0							AC11				
3C		VREFB3CN0	VREFB3CN0							Y6				
3D		VREFB3DN0	VREFB3DN0							M8				
			NC							U6				
			NC							R6				
			NC							P6				
			NC							N6				
			NC							AG26				
			NC							AD18				
			NC							AC6				
			NC							AC18				

Bank Number	Index within I/O Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	HPS Function	Dedicated Tx/Rx Channel	Soft CDR Support	GT support	HF35	DQS for X4	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36
			NC							K1				
			NC							K2				
			NC							M2				
			NC							L2				
			NC							U2				
			NC							U1				
			NC							J2				
			NC							J3				
			NC							L4				
			NC							L3				
			NC							T3				
			NC							T2				
			NC							H1				
			NC							J1				
			NC							V1				
			NC							W1				
			VCCH_GXBL1CF							V26				
			VCCH_GXBL1CF							P26				
			VCCH_GXBL1CF							K26				
			VCCH_GXBL1CF							AB26				
			VCCR_GXBL1C							AD28				
			VCCR_GXBL1C							AD27				
			VCCR_GXBL1C							AD26				
			VCCR_GXBL1D							Y28				
			VCCR_GXBL1D							Y27				
			VCCR_GXBL1D							Y26				
			VCCR_GXBL1E							T28				
			VCCR_GXBL1E							T27				
			VCCR_GXBL1E							T26				
			VCCR_GXBL1F							M28				
			VCCR_GXBL1F							M27				
			VCCR_GXBL1F							M26				
			VCCT_GXBL1C							AB28				
			VCCT_GXBL1C							AB27				
			VCCT_GXBL1D							V28				
			VCCT_GXBL1D							V27				
			VCCT_GXBL1E							P28				
			VCCT_GXBL1E							P27				
			VCCT_GXBL1F							K28				
			VCCT_GXBL1F							K27				
			RREF_BL							AP29				
			VCCADC							AF15				
			VCCERAM							Y24				
			VCCERAM							W24				
			VCCERAM							W23				
			VCCERAM							V24				
			VCCERAM							V23				
			VCCERAM							U23				
			VCCERAM							T24				
			VCCERAM							T23				
			VCCERAM							R24				
			VCCERAM							P24				
			VCCERAM							P23				
			VCCERAM							N24				
			VCCERAM							N23				
			VCCERAM							N20				
			VCCERAM							N16				
			VCCERAM							N13				
			VCCERAM							N10				
			VCCERAM							AB23				
			VCCERAM							AB20				
			VCCERAM							AB16				
			VCCERAM							AB13				
			VCCERAM							AB10				
			VCCERAM							AA24				
			VCCERAM							AA23				
			VCCFUSEWR_SDM							AE16				
			VCCLSENSE							T15				
			VCCL_HPS							M13				
			VCCL_HPS							L14				
			VCCL_HPS							L13				
			VCCL_HPS							L12				
			VCCL_HPS							K14				
			VCCP							Y11				
			VCCP							P18				
			VCCP							P11				
			VCCP							N18				
			VCCP							N11				
			VCCP							AB18				
			VCCP							AB11				
			VCCP							AA18				
			VCCPLLDIG_HPS							J11				
			VCCPLLDIG_SDM							AD17				
			VCCPLL_HPS							K11				
			VCCPLL_SDM							AC16				

January 2020	2020.01.06	Initial release.
October 2020	2020.10.27	Removed SD/MMC configuration mode support from Intel Stratix 10 devices.
December 2020	2020.12.10	Added 3.3V I/O in Bank 3C to the IO resource count file.

(1) For more information about pin definition and pin connection guidelines, refer to the Intel® Stratix® 10 Device Family Pin Connection Guidelines