

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
1A	VREFB1N0	IO	ADC1IN1		DIFFIO RX L1n	DIFFOUT L1n	Low Speed	6
1A	VREFB1N0	IO	ADC1IN2		DIFFIO RX L1p	DIFFOUT L1p	Low Speed	7
1A	VREFB1N0	IO	ADC1IN3		DIFFIO RX L3n	DIFFOUT L3n	Low Speed	8
1A	VREFB1N0	IO	ADC1IN4		DIFFIO RX L3p	DIFFOUT L3p	Low Speed	10
1A	VREFB1N0	IO	ADC1IN5		DIFFIO RX L5n	DIFFOUT L5n	Low Speed	11
1A	VREFB1N0	IO	ADC1IN6		DIFFIO RX L5p	DIFFOUT L5p	Low Speed	12
1A	VREFB1N0	IO	ADC1IN7		DIFFIO RX L7n	DIFFOUT L7n	Low Speed	13
1A	VREFB1N0	IO	ADC1IN8		DIFFIO RX L7p	DIFFOUT L7p	Low Speed	14
1B	VREFB1N0	IO		JTAGEN				15
1B	VREFB1N0	IO		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	16
1B	VREFB1N0	IO	VREFB1N0					17
1B	VREFB1N0	IO		TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	18
1B	VREFB1N0	IO		TDI	DIFFIO RX L12n	DIFFOUT L12n	Low Speed	19
1B	VREFB1N0	IO		TD0	DIFFIO RX L12p	DIFFOUT L12p	Low Speed	20
1B	VREFB1N0	IO			DIFFIO RX L14n	DIFFOUT L14n	Low Speed	21
1B	VREFB1N0	IO			DIFFIO RX L14p	DIFFOUT L14p	Low Speed	22
1B	VREFB1N0	IO			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	24
1B	VREFB1N0	IO			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	25
	2 VREFB2N0	IO	CLK0n		DIFFIO RX L20n	DIFFOUT L20n	High Speed	26
	2 VREFB2N0	IO	CLK0p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	27
	2 VREFB2N0	IO	CLK1n		DIFFIO RX L22n	DIFFOUT L22n	High Speed	28
	2 VREFB2N0	IO	CLK1p		DIFFIO RX L22p	DIFFOUT L22p	High Speed	29
	2 VREFB2N0	IO	VREFB2N0					30
	2 VREFB2N0	IO	PLL L CLKOUTn		DIFFIO RX L31n	DIFFOUT L31n	High Speed	32
	2 VREFB2N0	IO	PLL L CLKOUTp		DIFFIO RX L31p	DIFFOUT L31p	High Speed	33
	3 VREFB3N0	IO			DIFFIO TX RX B1n	DIFFOUT B1n	High Speed	38
	3 VREFB3N0	IO			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	39
	3 VREFB3N0	IO			DIFFIO TX RX B3n	DIFFOUT B3n	High Speed	41
	3 VREFB3N0	IO			DIFFIO TX RX B3p	DIFFOUT B3p	High Speed	43
	3 VREFB3N0	IO			DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	44
	3 VREFB3N0	IO			DIFFIO TX RX B5p	DIFFOUT B5p	High Speed	45
	3 VREFB3N0	IO			DIFFIO TX RX B13n	DIFFOUT B13n	High Speed	46
	3 VREFB3N0	IO			DIFFIO TX RX B13p	DIFFOUT B13p	High Speed	47
	3 VREFB3N0	IO			DIFFIO TX RX B15n	DIFFOUT B15n	High Speed	50
	3 VREFB3N0	IO	VREFB3N0					48
	3 VREFB3N0	IO			DIFFIO TX RX B15p	DIFFOUT B15p	High Speed	52
	3 VREFB3N0	IO						54
	3 VREFB3N0	IO	CLK6n		DIFFIO TX RX B18n	DIFFOUT B18n	High Speed	55
	3 VREFB3N0	IO	CLK6p		DIFFIO TX RX B18p	DIFFOUT B18p	High Speed	56
	3 VREFB3N0	IO	CLK7n		DIFFIO TX RX B20n	DIFFOUT B20n	High Speed	57
	3 VREFB3N0	IO	CLK7p		DIFFIO TX RX B20p	DIFFOUT B20p	High Speed	58
	3 VREFB3N0	IO			DIFFIO TX RX B22n	DIFFOUT B22n	High Speed	59
	3 VREFB3N0	IO			DIFFIO TX RX B22p	DIFFOUT B22p	High Speed	60
	4 VREFB4N0	IO	VREFB4N0					61
	4 VREFB4N0	IO						62
	4 VREFB4N0	IO			DIFFIO TX RX B35n	DIFFOUT B35n	High Speed	64
	4 VREFB4N0	IO			DIFFIO TX RX B35p	DIFFOUT B35p	High Speed	65
	4 VREFB4N0	IO						66
	4 VREFB4N0	IO			DIFFIO TX RX B41n	DIFFOUT B41n	High Speed	69
	4 VREFB4N0	IO			DIFFIO TX RX B41p	DIFFOUT B41p	High Speed	70
	5 VREFB5N0	IO	RUP		DIFFIO RX R1p	DIFFOUT R1p	High Speed	75
	5 VREFB5N0	IO			DIFFIO RX R2p	DIFFOUT R2p	High Speed	74
	5 VREFB5N0	IO	RDN		DIFFIO RX R1n	DIFFOUT R1n	High Speed	77
	5 VREFB5N0	IO			DIFFIO RX R2n	DIFFOUT R2n	High Speed	76
	5 VREFB5N0	IO			DIFFIO RX R11p	DIFFOUT R11p	High Speed	79
	5 VREFB5N0	IO						78
	5 VREFB5N0	IO			DIFFIO RX R11n	DIFFOUT R11n	High Speed	81
	5 VREFB5N0	IO	VREFB5N0					80
	5 VREFB5N0	IO			DIFFIO RX R14p	DIFFOUT R14p	High Speed	85
	5 VREFB5N0	IO			DIFFIO RX R15p	DIFFOUT R15p	High Speed	84
	5 VREFB5N0	IO			DIFFIO RX R14n	DIFFOUT R14n	High Speed	87
	5 VREFB5N0	IO			DIFFIO RX R15n	DIFFOUT R15n	High Speed	86
	6 VREFB6N0	IO	CLK2p		DIFFIO RX R18p	DIFFOUT R18p	High Speed	88
	6 VREFB6N0	IO	CLK2n		DIFFIO RX R18n	DIFFOUT R18n	High Speed	89
	6 VREFB6N0	IO	CLK3p		DIFFIO RX R20p	DIFFOUT R20p	High Speed	90
	6 VREFB6N0	IO	CLK3n		DIFFIO RX R20n	DIFFOUT R20n	High Speed	91
	6 VREFB6N0	IO			DIFFIO RX R22p	DIFFOUT R22p	High Speed	92
	6 VREFB6N0	IO			DIFFIO RX R22n	DIFFOUT R22n	High Speed	93
	6 VREFB6N0	IO	DPCLK3		DIFFIO RX R30p	DIFFOUT R30p	High Speed	96
	6 VREFB6N0	IO	VREFB6N0					97
	6 VREFB6N0	IO	DPCLK2		DIFFIO RX R30n	DIFFOUT R30n	High Speed	98
	6 VREFB6N0	IO			DIFFIO RX R31p	DIFFOUT R31p	High Speed	99
	6 VREFB6N0	IO			DIFFIO RX R32p	DIFFOUT R32p	High Speed	100
	6 VREFB6N0	IO			DIFFIO RX R31n	DIFFOUT R31n	High Speed	101
	6 VREFB6N0	IO			DIFFIO RX R32n	DIFFOUT R32n	High Speed	102
	6 VREFB6N0	IO			DIFFIO RX R37p	DIFFOUT R37p	High Speed	105
	6 VREFB6N0	IO			DIFFIO RX R37n	DIFFOUT R37n	High Speed	106
	7 VREFB7N0	IO			DIFFIO RX T1p	DIFFOUT T1p	High Speed	110
	7 VREFB7N0	IO			DIFFIO RX T1n	DIFFOUT T1n	High Speed	111
	7 VREFB7N0	IO	VREFB7N0					112
	7 VREFB7N0	IO						113
	7 VREFB7N0	IO			DIFFIO RX T22p	DIFFOUT T22p	High Speed	114
	7 VREFB7N0	IO			DIFFIO RX T22n	DIFFOUT T22n	High Speed	118
	8 VREFB8N0	IO			DIFFIO RX T28p	DIFFOUT T28p	Low Speed	120
	8 VREFB8N0	IO		DEV CLRn	DIFFIO RX T28n	DIFFOUT T28n	Low Speed	121
	8 VREFB8N0	IO		DEV OE				122
	8 VREFB8N0	IO	VREFB8N0					123
	8 VREFB8N0	IO		CONFIG_SEL				126

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 (2)
8	VREFB8N0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	Low_Speed	124
8	VREFB8N0	Input only		nCONFIG				129
8	VREFB8N0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	Low_Speed	127
8	VREFB8N0	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	Low_Speed	130
8	VREFB8N0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	Low_Speed	131
8	VREFB8N0	IO			DIFFIO_RX_T34p	DIFFOUT_T34p	Low_Speed	132
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T34n	DIFFOUT_T34n	Low_Speed	134
8	VREFB8N0	IO						135
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T36p	DIFFOUT_T36p	Low_Speed	136
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T36n	DIFFOUT_T36n	Low_Speed	138
8	VREFB8N0	IO			DIFFIO_RX_T38p	DIFFOUT_T38p	Low_Speed	140
8	VREFB8N0	IO			DIFFIO_RX_T38n	DIFFOUT_T38n	Low_Speed	141
		GND						95
		GND						83
		GND						68
		GND						63
		GND						53
		GND						42
		GND						142
		GND						137
		GND						133
		GND						125
		GND						116
		GND						104
		REFGND						1
		VCCIO1A						9
		VCCIO1B						23
		VCCIO2						31
		VCCIO3						49
		VCCIO3						40
		VCCIO4						67
		VCCIO5						82
		VCCIO6						94
		VCCIO6						103
		VCCIO7						117
		VCCIO8						139
		VCCIO8						128
		VCCA1						35
		VCCA2						34
		VCCA3						107
		VCCA4						143
		VCCA5						71
		VCCA6						2
		VCC ONE						73
		VCC ONE						72
		VCC ONE						51
		VCC ONE						37
		VCC ONE						36
		VCC ONE						144
		VCC ONE						115
		VCC ONE						109
		VCC ONE						108
		VCC ONE						1
		ADC_VREF						5
		ANAIN1						3

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the [Intel MAX 10 FPGA Device Family Pin Connection Guidelines](#).

(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
1A	VREFB1N0	IO	ADC1IN1		DIFFIO RX L1n	DIFFOUT L1n	Low Speed	D1
1A	VREFB1N0	IO	ADC1IN2		DIFFIO RX L1p	DIFFOUT L1p	Low Speed	C2
1A	VREFB1N0	IO	ADC1IN3		DIFFIO RX L3n	DIFFOUT L3n	Low Speed	E3
1A	VREFB1N0	IO	ADC1IN4		DIFFIO RX L3p	DIFFOUT L3p	Low Speed	E4
1A	VREFB1N0	IO	ADC1IN5		DIFFIO RX L5n	DIFFOUT L5n	Low Speed	C1
1A	VREFB1N0	IO	ADC1IN6		DIFFIO RX L5p	DIFFOUT L5p	Low Speed	B1
1A	VREFB1N0	IO	ADC1IN7		DIFFIO RX L7n	DIFFOUT L7n	Low Speed	F1
1A	VREFB1N0	IO	ADC1IN8		DIFFIO RX L7p	DIFFOUT L7p	Low Speed	E1
1B	VREFB1N0	IO		JTAGEN				E5
1B	VREFB1N0	IO		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	G1
1B	VREFB1N0	IO	VREFB1N0					H1
1B	VREFB1N0	IO		TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	G2
1B	VREFB1N0	IO		TDI	DIFFIO RX L12n	DIFFOUT L12n	Low Speed	F5
1B	VREFB1N0	IO		TDO	DIFFIO RX L12p	DIFFOUT L12p	Low Speed	F6
1B	VREFB1N0	IO			DIFFIO RX L14n	DIFFOUT L14n	Low Speed	F4
1B	VREFB1N0	IO			DIFFIO RX L14p	DIFFOUT L14p	Low Speed	G4
1B	VREFB1N0	IO			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	H2
1B	VREFB1N0	IO			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	H3
2	VREFB2N0	IO	CLK0n		DIFFIO RX L20n	DIFFOUT L20n	High Speed	G5
2	VREFB2N0	IO			DIFFIO RX L21n	DIFFOUT L21n	High Speed	J1
2	VREFB2N0	IO	CLK0p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	H6
2	VREFB2N0	IO			DIFFIO RX L21p	DIFFOUT L21p	High Speed	J2
2	VREFB2N0	IO	CLK1n		DIFFIO RX L22n	DIFFOUT L22n	High Speed	H5
2	VREFB2N0	IO			DIFFIO RX L23n	DIFFOUT L23n	High Speed	M1
2	VREFB2N0	IO	CLK1p		DIFFIO RX L22p	DIFFOUT L22p	High Speed	H4
2	VREFB2N0	IO			DIFFIO RX L23p	DIFFOUT L23p	High Speed	M2
2	VREFB2N0	IO	DPCLK0		DIFFIO RX L24n	DIFFOUT L24n	High Speed	N2
2	VREFB2N0	IO	VREFB2N0					N3
2	VREFB2N0	IO	DPCLK1		DIFFIO RX L24p	DIFFOUT L24p	High Speed	N3
2	VREFB2N0	IO						L2
2	VREFB2N0	IO	PLL L CLKOUTn		DIFFIO RX L31n	DIFFOUT L31n	High Speed	M3
2	VREFB2N0	IO			DIFFIO RX L32n	DIFFOUT L32n	High Speed	K1
2	VREFB2N0	IO	PLL L CLKOUTp		DIFFIO RX L31p	DIFFOUT L31p	High Speed	L3
2	VREFB2N0	IO			DIFFIO RX L32p	DIFFOUT L32p	High Speed	K2
3	VREFB3N0	IO			DIFFIO TX RX B1n	DIFFOUT B1n	High Speed	L5
3	VREFB3N0	IO			DIFFIO RX B2n	DIFFOUT B2n	High Speed	M4
3	VREFB3N0	IO			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	L4
3	VREFB3N0	IO			DIFFIO RX B2p	DIFFOUT B2p	High Speed	M5
3	VREFB3N0	IO			DIFFIO TX RX B3n	DIFFOUT B3n	High Speed	K5
3	VREFB3N0	IO			DIFFIO RX B4n	DIFFOUT B4n	High Speed	N4
3	VREFB3N0	IO			DIFFIO TX RX B3p	DIFFOUT B3p	High Speed	J5
3	VREFB3N0	IO			DIFFIO RX B4p	DIFFOUT B4p	High Speed	N5
3	VREFB3N0	IO			DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	N6
3	VREFB3N0	IO			DIFFIO RX B6n	DIFFOUT B6n	High Speed	N7
3	VREFB3N0	IO			DIFFIO TX RX B5p	DIFFOUT B5p	High Speed	M7
3	VREFB3N0	IO			DIFFIO RX B6p	DIFFOUT B6p	High Speed	N8
3	VREFB3N0	IO			DIFFIO TX RX B13n	DIFFOUT B13n	High Speed	J6
3	VREFB3N0	IO			DIFFIO RX B14n	DIFFOUT B14n	High Speed	M8
3	VREFB3N0	IO			DIFFIO TX RX B13p	DIFFOUT B13p	High Speed	K6
3	VREFB3N0	IO			DIFFIO RX B14p	DIFFOUT B14p	High Speed	M9
3	VREFB3N0	IO			DIFFIO TX RX B15n	DIFFOUT B15n	High Speed	J7
3	VREFB3N0	IO	VREFB3N0					N11
3	VREFB3N0	IO			DIFFIO TX RX B15p	DIFFOUT B15p	High Speed	K7
3	VREFB3N0	IO						N12
3	VREFB3N0	IO			DIFFIO TX RX B16n	DIFFOUT B16n	High Speed	M13
3	VREFB3N0	IO			DIFFIO RX B17n	DIFFOUT B17n	High Speed	N10
3	VREFB3N0	IO			DIFFIO TX RX B16p	DIFFOUT B16p	High Speed	M12
3	VREFB3N0	IO			DIFFIO RX B17p	DIFFOUT B17p	High Speed	N9
3	VREFB3N0	IO	CLK6n		DIFFIO TX RX B18n	DIFFOUT B18n	High Speed	M11
3	VREFB3N0	IO	CLK6p		DIFFIO TX RX B18p	DIFFOUT B18p	High Speed	L11
3	VREFB3N0	IO	CLK7n		DIFFIO TX RX B20n	DIFFOUT B20n	High Speed	J8
3	VREFB3N0	IO	CLK7p		DIFFIO TX RX B20p	DIFFOUT B20p	High Speed	K8
3	VREFB3N0	IO			DIFFIO TX RX B22n	DIFFOUT B22n	High Speed	M10
3	VREFB3N0	IO			DIFFIO TX RX B22p	DIFFOUT B22p	High Speed	L10
5	VREFB5N0	IO	RUP		DIFFIO RX R1p	DIFFOUT R1p	High Speed	K10
5	VREFB5N0	IO			DIFFIO RX R2p	DIFFOUT R2p	High Speed	K11
5	VREFB5N0	IO	RDN		DIFFIO RX R1n	DIFFOUT R1n	High Speed	J10
5	VREFB5N0	IO			DIFFIO RX R2n	DIFFOUT R2n	High Speed	L12
5	VREFB5N0	IO			DIFFIO RX R11p	DIFFOUT R11p	High Speed	K12
5	VREFB5N0	IO						L13
5	VREFB5N0	IO			DIFFIO RX R11n	DIFFOUT R11n	High Speed	J12
5	VREFB5N0	IO	VREFB5N0					K13
5	VREFB5N0	IO			DIFFIO RX R12p	DIFFOUT R12p	High Speed	J9
5	VREFB5N0	IO			DIFFIO RX R13p	DIFFOUT R13p	High Speed	J13
5	VREFB5N0	IO			DIFFIO RX R12n	DIFFOUT R12n	High Speed	H10
5	VREFB5N0	IO			DIFFIO RX R13n	DIFFOUT R13n	High Speed	H13
5	VREFB5N0	IO			DIFFIO RX R14p	DIFFOUT R14p	High Speed	H9
5	VREFB5N0	IO			DIFFIO RX R15p	DIFFOUT R15p	High Speed	G13
5	VREFB5N0	IO			DIFFIO RX R14n	DIFFOUT R14n	High Speed	H8
5	VREFB5N0	IO			DIFFIO RX R15n	DIFFOUT R15n	High Speed	G12
6	VREFB6N0	IO	CLK2p		DIFFIO RX R18p	DIFFOUT R18p	High Speed	G9
6	VREFB6N0	IO	CLK2n		DIFFIO RX R18n	DIFFOUT R18n	High Speed	G10
6	VREFB6N0	IO	CLK3p		DIFFIO RX R20p	DIFFOUT R20p	High Speed	F13
6	VREFB6N0	IO	CLK3n		DIFFIO RX R20n	DIFFOUT R20n	High Speed	E13
6	VREFB6N0	IO			DIFFIO RX R22p	DIFFOUT R22p	High Speed	F12
6	VREFB6N0	IO			DIFFIO RX R22n	DIFFOUT R22n	High Speed	E12
6	VREFB6N0	IO	DPCLK3		DIFFIO RX R30p	DIFFOUT R30p	High Speed	F9
6	VREFB6N0	IO	VREFB6N0					D13
6	VREFB6N0	IO	DPCLK2		DIFFIO RX R30n	DIFFOUT R30n	High Speed	F10
6	VREFB6N0	IO						C13
6	VREFB6N0	IO			DIFFIO RX R31p	DIFFOUT R31p	High Speed	F8

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U169
6	VREFB6N0	IO			DIFFIO RX R32p	DIFFOUT R32p	High Speed	B12
6	VREFB6N0	IO			DIFFIO RX R31n	DIFFOUT R31n	High Speed	E9
6	VREFB6N0	IO			DIFFIO RX R32n	DIFFOUT R32n	High Speed	B11
6	VREFB6N0	IO			DIFFIO RX R33p	DIFFOUT R33p	High Speed	C12
6	VREFB6N0	IO			DIFFIO RX R34p	DIFFOUT R34p	High Speed	B13
6	VREFB6N0	IO			DIFFIO RX R33n	DIFFOUT R33n	High Speed	C11
6	VREFB6N0	IO			DIFFIO RX R34n	DIFFOUT R34n	High Speed	A12
6	VREFB6N0	IO			DIFFIO RX R35p	DIFFOUT R35p	High Speed	E10
6	VREFB6N0	IO			DIFFIO RX R35n	DIFFOUT R35n	High Speed	D9
6	VREFB6N0	IO			DIFFIO RX R37p	DIFFOUT R37p	High Speed	D12
6	VREFB6N0	IO			DIFFIO RX R37n	DIFFOUT R37n	High Speed	D11
8	VREFB8N0	IO	CLK5p		DIFFIO RX T26p	DIFFOUT T26p	Low Speed	C10
8	VREFB8N0	IO			DIFFIO RX T27p	DIFFOUT T27p	Low Speed	A8
8	VREFB8N0	IO	CLK5n		DIFFIO RX T26n	DIFFOUT T26n	Low Speed	C9
8	VREFB8N0	IO			DIFFIO RX T27n	DIFFOUT T27n	Low Speed	A9
8	VREFB8N0	IO			DIFFIO RX T28p	DIFFOUT T28p	Low Speed	B10
8	VREFB8N0	IO			DIFFIO RX T29p	DIFFOUT T29p	Low Speed	A10
8	VREFB8N0	IO		DEV CLRn	DIFFIO RX T28n	DIFFOUT T28n	Low Speed	B9
8	VREFB8N0	IO			DIFFIO RX T29n	DIFFOUT T29n	Low Speed	A11
8	VREFB8N0	IO		DEV OE	DIFFIO RX T30p	DIFFOUT T30p	Low Speed	D8
8	VREFB8N0	IO			DIFFIO RX T30n	DIFFOUT T30n	Low Speed	E8
8	VREFB8N0	IO	VREFB8N0					B7
8	VREFB8N0	IO		CONFIG SEL				D7
8	VREFB8N0	IO			DIFFIO RX T31p	DIFFOUT T31p	Low Speed	A7
8	VREFB8N0	Input only		nCONFIG				E7
8	VREFB8N0	IO			DIFFIO RX T31n	DIFFOUT T31n	Low Speed	A6
8	VREFB8N0	IO			DIFFIO RX T32p	DIFFOUT T32p	Low Speed	B6
8	VREFB8N0	IO			DIFFIO RX T32n	DIFFOUT T32n	Low Speed	B5
8	VREFB8N0	IO			DIFFIO RX T33p	DIFFOUT T33p	Low Speed	A4
8	VREFB8N0	IO			DIFFIO RX T33n	DIFFOUT T33n	Low Speed	B5
8	VREFB8N0	IO			DIFFIO RX T34p	DIFFOUT T34p	Low Speed	A3
8	VREFB8N0	IO			DIFFIO RX T34n	DIFFOUT T34n	Low Speed	E6
8	VREFB8N0	IO			DIFFIO RX T35p	DIFFOUT T35p	Low Speed	B3
8	VREFB8N0	IO		CRC ERROR	DIFFIO RX T34n	DIFFOUT T34n	Low Speed	D6
8	VREFB8N0	IO			DIFFIO RX T35n	DIFFOUT T35n	Low Speed	B4
8	VREFB8N0	IO		nSTATUS	DIFFIO RX T36p	DIFFOUT T36p	Low Speed	C4
8	VREFB8N0	IO						A5
8	VREFB8N0	IO		CONF_DONE	DIFFIO RX T36n	DIFFOUT T36n	Low Speed	C5
8	VREFB8N0	IO			DIFFIO RX T38p	DIFFOUT T38p	Low Speed	A2
8	VREFB8N0	IO			DIFFIO RX T38n	DIFFOUT T38n	Low Speed	B2
		GND						N13
		GND						N1
		GND						M6
		GND						L9
		GND						J4
		GND						H12
		GND						G7
		GND						F3
		GND						E11
		GND						D5
		GND						C3
		GND						B8
		GND						A13
		GND						A1
		REFGND						E2
		VCCIO1A						F2
		VCCIO1B						G3
		VCCIO2						K3
		VCCIO2						J3
		VCCIO3						L8
		VCCIO3						L7
		VCCIO3						L6
		VCCIO5						J11
		VCCIO5						H11
		VCCIO6						G11
		VCCIO6						F11
		VCCIO8						C8
		VCCIO8						C7
		VCCIO8						C6
		VCCA1						K4
		VCCA2						D10
		VCCA3						D4
		VCCA4						K9
		VCC ONE						H7
		VCC ONE						G8
		VCC ONE						G6
		VCC ONE						F7
		ADC VREF						D3
		ANAIN1						D2

Note:

 (1) For more information about pin definition and pin connection guidelines, refer to the [Intel MAX 10 FPGA Device Family Pin Connection Guidelines](#).

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
1A	VREFB1N0	IO	ADC11N1		DIFFIO RX L1n	DIFFOUT L1n	Low Speed	D4
1A	VREFB1N0	IO	ADC11N9		DIFFIO RX L2n	DIFFOUT L2n	Low Speed	C2
1A	VREFB1N0	IO	ADC11N2		DIFFIO RX L1p	DIFFOUT L1p	Low Speed	E4
1A	VREFB1N0	IO	ADC11N16		DIFFIO RX L2p	DIFFOUT L2p	Low Speed	O2
1A	VREFB1N0	IO	ADC11N3		DIFFIO RX L3n	DIFFOUT L3n	Low Speed	G6
1A	VREFB1N0	IO	ADC11N11		DIFFIO RX L4n	DIFFOUT L4n	Low Speed	B1
1A	VREFB1N0	IO	ADC11N4		DIFFIO RX L3p	DIFFOUT L3p	Low Speed	H6
1A	VREFB1N0	IO	ADC11N12		DIFFIO RX L4p	DIFFOUT L4p	Low Speed	C1
1A	VREFB1N0	IO	ADC11N5		DIFFIO RX L5n	DIFFOUT L5n	Low Speed	F5
1A	VREFB1N0	IO	ADC11N13		DIFFIO RX L6n	DIFFOUT L6n	Low Speed	D1
1A	VREFB1N0	IO	ADC11N6		DIFFIO RX L5p	DIFFOUT L5p	Low Speed	E5
1A	VREFB1N0	IO	ADC11N14		DIFFIO RX L6p	DIFFOUT L6p	Low Speed	E1
1A	VREFB1N0	IO	ADC11N7		DIFFIO RX L7n	DIFFOUT L7n	Low Speed	G3
1A	VREFB1N0	IO	ADC11N15		DIFFIO RX L8n	DIFFOUT L8n	Low Speed	F1
1A	VREFB1N0	IO	ADC11N8		DIFFIO RX L7p	DIFFOUT L7p	Low Speed	F2
1A	VREFB1N0	IO	ADC11N10		DIFFIO RX L8p	DIFFOUT L8p	Low Speed	G1
1B	VREFB1N0	IO			DIFFIO RX L9n	DIFFOUT L9n	Low Speed	G7
1B	VREFB1N0	IO			DIFFIO RX L10n	DIFFOUT L10n	Low Speed	H2
1B	VREFB1N0	IO		JTAGEN	DIFFIO RX L9p	DIFFOUT L9p	Low Speed	H7
1B	VREFB1N0	IO			DIFFIO RX L10p	DIFFOUT L10p	Low Speed	H1
1B	VREFB1N0	IO		TMS	DIFFIO RX L11n	DIFFOUT L11n	Low Speed	J7
1B	VREFB1N0	IO	VREFB1N0				Low Speed	J3
1B	VREFB1N0	IO		TCK	DIFFIO RX L11p	DIFFOUT L11p	Low Speed	J8
1B	VREFB1N0	IO					Low Speed	J4
1B	VREFB1N0	IO		TDI	DIFFIO RX L12n	DIFFOUT L12n	Low Speed	H3
1B	VREFB1N0	IO			DIFFIO RX L13n	DIFFOUT L13n	Low Speed	J2
1B	VREFB1N0	IO		TD0	DIFFIO RX L12p	DIFFOUT L12p	Low Speed	H4
1B	VREFB1N0	IO			DIFFIO RX L13p	DIFFOUT L13p	Low Speed	J1
1B	VREFB1N0	IO			DIFFIO RX L14n	DIFFOUT L14n	Low Speed	J6
1B	VREFB1N0	IO			DIFFIO RX L15n	DIFFOUT L15n	Low Speed	K2
1B	VREFB1N0	IO			DIFFIO RX L14p	DIFFOUT L14p	Low Speed	K7
1B	VREFB1N0	IO			DIFFIO RX L15p	DIFFOUT L15p	Low Speed	K1
1B	VREFB1N0	IO			DIFFIO RX L16n	DIFFOUT L16n	Low Speed	K4
1B	VREFB1N0	IO			DIFFIO RX L17n	DIFFOUT L17n	Low Speed	L1
1B	VREFB1N0	IO			DIFFIO RX L16p	DIFFOUT L16p	Low Speed	K3
1B	VREFB1N0	IO			DIFFIO RX L17p	DIFFOUT L17p	Low Speed	L2
2	VREFB2N0	IO	CLK0n		DIFFIO RX L20n	DIFFOUT L20n	High Speed	L3
2	VREFB2N0	IO			DIFFIO RX L21n	DIFFOUT L21n	High Speed	M1
2	VREFB2N0	IO	CLK0p		DIFFIO RX L20p	DIFFOUT L20p	High Speed	M3
2	VREFB2N0	IO			DIFFIO RX L21p	DIFFOUT L21p	High Speed	M2
2	VREFB2N0	IO	CLK1n		DIFFIO RX L22n	DIFFOUT L22n	High Speed	K8
2	VREFB2N0	IO			DIFFIO RX L23n	DIFFOUT L23n	High Speed	N1
2	VREFB2N0	IO	CLK1p		DIFFIO RX L22p	DIFFOUT L22p	High Speed	L8
2	VREFB2N0	IO			DIFFIO RX L23p	DIFFOUT L23p	High Speed	P1
2	VREFB2N0	IO	DPCLK0		DIFFIO RX L24n	DIFFOUT L24n	High Speed	M4
2	VREFB2N0	IO	VREFB2N0				High Speed	R1
2	VREFB2N0	IO	DPCLK1		DIFFIO RX L24p	DIFFOUT L24p	High Speed	N3
2	VREFB2N0	IO					High Speed	R2
2	VREFB2N0	IO			DIFFIO RX L25n	DIFFOUT L25n	High Speed	R3
2	VREFB2N0	IO			DIFFIO RX L26n	DIFFOUT L26n	High Speed	P2
2	VREFB2N0	IO			DIFFIO RX L25p	DIFFOUT L25p	High Speed	T3
2	VREFB2N0	IO			DIFFIO RX L26p	DIFFOUT L26p	High Speed	P3
2	VREFB2N0	IO			DIFFIO RX L27n	DIFFOUT L27n	High Speed	L7
2	VREFB2N0	IO			DIFFIO RX L28n	DIFFOUT L28n	High Speed	T1
2	VREFB2N0	IO			DIFFIO RX L27p	DIFFOUT L27p	High Speed	M7
2	VREFB2N0	IO			DIFFIO RX L28p	DIFFOUT L28p	High Speed	T2
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO RX L31n	DIFFOUT L31n	High Speed	N4
2	VREFB2N0	IO			DIFFIO RX L32n	DIFFOUT L32n	High Speed	U1
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO RX L31p	DIFFOUT L31p	High Speed	P4
2	VREFB2N0	IO			DIFFIO RX L32p	DIFFOUT L32p	High Speed	U2
3	VREFB3N0	IO			DIFFIO TX RX B1n	DIFFOUT B1n	High Speed	R4
3	VREFB3N0	IO			DIFFIO TX RX B2n	DIFFOUT B2n	High Speed	U3
3	VREFB3N0	IO			DIFFIO TX RX B1p	DIFFOUT B1p	High Speed	T4
3	VREFB3N0	IO			DIFFIO TX RX B2p	DIFFOUT B2p	High Speed	V2
3	VREFB3N0	IO			DIFFIO TX RX B3n	DIFFOUT B3n	High Speed	P6
3	VREFB3N0	IO			DIFFIO TX RX B4n	DIFFOUT B4n	High Speed	V3
3	VREFB3N0	IO			DIFFIO TX RX B3p	DIFFOUT B3p	High Speed	P5
3	VREFB3N0	IO			DIFFIO TX RX B4p	DIFFOUT B4p	High Speed	V4
3	VREFB3N0	IO			DIFFIO TX RX B5n	DIFFOUT B5n	High Speed	R5
3	VREFB3N0	IO			DIFFIO TX RX B6n	DIFFOUT B6n	High Speed	U5
3	VREFB3N0	IO			DIFFIO TX RX B5p	DIFFOUT B5p	High Speed	R6
3	VREFB3N0	IO			DIFFIO TX RX B6p	DIFFOUT B6p	High Speed	V5
3	VREFB3N0	IO			DIFFIO TX RX B13n	DIFFOUT B13n	High Speed	T5
3	VREFB3N0	IO			DIFFIO TX RX B14n	DIFFOUT B14n	High Speed	T7
3	VREFB3N0	IO			DIFFIO TX RX B13p	DIFFOUT B13p	High Speed	T6
3	VREFB3N0	IO			DIFFIO TX RX B14p	DIFFOUT B14p	High Speed	T8
3	VREFB3N0	IO			DIFFIO TX RX B15n	DIFFOUT B15n	High Speed	N7
3	VREFB3N0	IO	VREFB3N0				High Speed	U6
3	VREFB3N0	IO			DIFFIO TX RX B15p	DIFFOUT B15p	High Speed	N8
3	VREFB3N0	IO					High Speed	V6
3	VREFB3N0	IO			DIFFIO TX RX B16n	DIFFOUT B16n	High Speed	R8
3	VREFB3N0	IO			DIFFIO TX RX B17n	DIFFOUT B17n	High Speed	U7
3	VREFB3N0	IO			DIFFIO TX RX B16p	DIFFOUT B16p	High Speed	R9
3	VREFB3N0	IO			DIFFIO TX RX B17p	DIFFOUT B17p	High Speed	V7
3	VREFB3N0	IO	CLK6n		DIFFIO TX RX B18n	DIFFOUT B18n	High Speed	V9
3	VREFB3N0	IO			DIFFIO TX RX B19n	DIFFOUT B19n	High Speed	U8
3	VREFB3N0	IO	CLK6p		DIFFIO TX RX B18p	DIFFOUT B18p	High Speed	U8
3	VREFB3N0	IO			DIFFIO TX RX B19p	DIFFOUT B19p	High Speed	U8
3	VREFB3N0	IO	CLK7n		DIFFIO TX RX B20n	DIFFOUT B20n	High Speed	M8

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
3	VREFB3N0	IO			DIFFIO RX B21n	DIFFOUT B21n	High Speed	V10
3	VREFB3N0	IO			DIFFIO TX RX B20p	DIFFOUT B20p	High Speed	M9
3	VREFB3N0	IO	CLK7p		DIFFIO RX B21p	DIFFOUT B21p	High Speed	V11
3	VREFB3N0	IO			DIFFIO TX RX B22n	DIFFOUT B22n	High Speed	T9
3	VREFB3N0	IO			DIFFIO RX B23n	DIFFOUT B23n	High Speed	V12
3	VREFB3N0	IO			DIFFIO TX RX B22p	DIFFOUT B22p	High Speed	T10
3	VREFB3N0	IO			DIFFIO RX B23p	DIFFOUT B23p	High Speed	U11
4	VREFB4N0	IO			DIFFIO TX RX B30n	DIFFOUT B30n	High Speed	P10
4	VREFB4N0	IO			DIFFIO RX B31n	DIFFOUT B31n	High Speed	U12
4	VREFB4N0	IO			DIFFIO TX RX B30p	DIFFOUT B30p	High Speed	N11
4	VREFB4N0	IO			DIFFIO RX B31p	DIFFOUT B31p	High Speed	U13
4	VREFB4N0	IO			DIFFIO TX RX B32n	DIFFOUT B32n	High Speed	M10
4	VREFB4N0	IO	VREFB4N0				High Speed	T11
4	VREFB4N0	IO			DIFFIO TX RX B32p	DIFFOUT B32p	High Speed	L10
4	VREFB4N0	IO					High Speed	T12
4	VREFB4N0	IO			DIFFIO TX RX B33n	DIFFOUT B33n	High Speed	R10
4	VREFB4N0	IO			DIFFIO RX B34n	DIFFOUT B34n	High Speed	V13
4	VREFB4N0	IO			DIFFIO TX RX B33p	DIFFOUT B33p	High Speed	R11
4	VREFB4N0	IO			DIFFIO RX B34p	DIFFOUT B34p	High Speed	V14
4	VREFB4N0	IO			DIFFIO TX RX B35n	DIFFOUT B35n	High Speed	R12
4	VREFB4N0	IO			DIFFIO RX B36n	DIFFOUT B36n	High Speed	T13
4	VREFB4N0	IO			DIFFIO TX RX B35p	DIFFOUT B35p	High Speed	R13
4	VREFB4N0	IO			DIFFIO RX B36p	DIFFOUT B36p	High Speed	T14
4	VREFB4N0	IO			DIFFIO TX RX B37n	DIFFOUT B37n	High Speed	R14
4	VREFB4N0	IO			DIFFIO RX B38n	DIFFOUT B38n	High Speed	V15
4	VREFB4N0	IO			DIFFIO TX RX B37p	DIFFOUT B37p	High Speed	T15
4	VREFB4N0	IO			DIFFIO RX B38p	DIFFOUT B38p	High Speed	U15
4	VREFB4N0	IO			DIFFIO TX RX B41n	DIFFOUT B41n	High Speed	U16
4	VREFB4N0	IO			DIFFIO RX B42n	DIFFOUT B42n	High Speed	V16
4	VREFB4N0	IO			DIFFIO TX RX B41p	DIFFOUT B41p	High Speed	U17
4	VREFB4N0	IO			DIFFIO RX B42p	DIFFOUT B42p	High Speed	V17
5	VREFB5N0	IO	RUP		DIFFIO RX R1p	DIFFOUT R1p	High Speed	N14
5	VREFB5N0	IO			DIFFIO RX R2p	DIFFOUT R2p	High Speed	T16
5	VREFB5N0	IO	RDN		DIFFIO RX R1n	DIFFOUT R1n	High Speed	P14
5	VREFB5N0	IO			DIFFIO RX R2n	DIFFOUT R2n	High Speed	R16
5	VREFB5N0	IO			DIFFIO RX R7p	DIFFOUT R7p	High Speed	M12
5	VREFB5N0	IO			DIFFIO RX R8p	DIFFOUT R8p	High Speed	U13
5	VREFB5N0	IO			DIFFIO RX R7n	DIFFOUT R7n	High Speed	M11
5	VREFB5N0	IO			DIFFIO RX R8n	DIFFOUT R8n	High Speed	T18
5	VREFB5N0	IO			DIFFIO RX R9p	DIFFOUT R9p	High Speed	N15
5	VREFB5N0	IO			DIFFIO RX R10p	DIFFOUT R10p	High Speed	N16
5	VREFB5N0	IO			DIFFIO RX R9n	DIFFOUT R9n	High Speed	M15
5	VREFB5N0	IO			DIFFIO RX R10n	DIFFOUT R10n	High Speed	M16
5	VREFB5N0	IO			DIFFIO RX R11p	DIFFOUT R11p	High Speed	R15
5	VREFB5N0	IO					High Speed	P16
5	VREFB5N0	IO			DIFFIO RX R11n	DIFFOUT R11n	High Speed	P15
5	VREFB5N0	IO	VREFB5N0				High Speed	P17
5	VREFB5N0	IO			DIFFIO RX R12p	DIFFOUT R12p	High Speed	L12
5	VREFB5N0	IO			DIFFIO RX R13p	DIFFOUT R13p	High Speed	T17
5	VREFB5N0	IO			DIFFIO RX R12n	DIFFOUT R12n	High Speed	L11
5	VREFB5N0	IO			DIFFIO RX R13n	DIFFOUT R13n	High Speed	R17
5	VREFB5N0	IO			DIFFIO RX R14p	DIFFOUT R14p	High Speed	L15
5	VREFB5N0	IO			DIFFIO RX R15p	DIFFOUT R15p	High Speed	L16
5	VREFB5N0	IO			DIFFIO RX R14n	DIFFOUT R14n	High Speed	K15
5	VREFB5N0	IO			DIFFIO RX R15n	DIFFOUT R15n	High Speed	K16
5	VREFB5N0	IO			DIFFIO RX R16p	DIFFOUT R16p	High Speed	R18
5	VREFB5N0	IO			DIFFIO RX R17p	DIFFOUT R17p	High Speed	N18
5	VREFB5N0	IO			DIFFIO RX R16n	DIFFOUT R16n	High Speed	P18
5	VREFB5N0	IO			DIFFIO RX R17n	DIFFOUT R17n	High Speed	M18
6	VREFB6N0	IO	CLK2p		DIFFIO RX R18p	DIFFOUT R18p	High Speed	K12
6	VREFB6N0	IO			DIFFIO RX R19p	DIFFOUT R19p	High Speed	M17
6	VREFB6N0	IO	CLK2n		DIFFIO RX R18n	DIFFOUT R18n	High Speed	K11
6	VREFB6N0	IO			DIFFIO RX R19n	DIFFOUT R19n	High Speed	L18
6	VREFB6N0	IO	CLK3p		DIFFIO RX R20p	DIFFOUT R20p	High Speed	L17
6	VREFB6N0	IO			DIFFIO RX R21p	DIFFOUT R21p	High Speed	K18
6	VREFB6N0	IO	CLK3n		DIFFIO RX R20n	DIFFOUT R20n	High Speed	K17
6	VREFB6N0	IO			DIFFIO RX R21n	DIFFOUT R21n	High Speed	J18
6	VREFB6N0	IO			DIFFIO RX R22p	DIFFOUT R22p	High Speed	H18
6	VREFB6N0	IO			DIFFIO RX R23p	DIFFOUT R23p	High Speed	H17
6	VREFB6N0	IO			DIFFIO RX R22n	DIFFOUT R22n	High Speed	G18
6	VREFB6N0	IO			DIFFIO RX R23n	DIFFOUT R23n	High Speed	G17
6	VREFB6N0	IO			DIFFIO RX R24p	DIFFOUT R24p	High Speed	J11
6	VREFB6N0	IO			DIFFIO RX R24n	DIFFOUT R24n	High Speed	J12
6	VREFB6N0	IO			DIFFIO RX R26p	DIFFOUT R26p	High Speed	J15
6	VREFB6N0	IO			DIFFIO RX R27p	DIFFOUT R27p	High Speed	H16
6	VREFB6N0	IO			DIFFIO RX R26n	DIFFOUT R26n	High Speed	H15
6	VREFB6N0	IO			DIFFIO RX R27n	DIFFOUT R27n	High Speed	H16
6	VREFB6N0	IO	DPCLK3		DIFFIO RX R30p	DIFFOUT R30p	High Speed	H11
6	VREFB6N0	IO	VREFB6N0				High Speed	F18
6	VREFB6N0	IO	DPCLK2		DIFFIO RX R30n	DIFFOUT R30n	High Speed	H12
6	VREFB6N0	IO					High Speed	E18
6	VREFB6N0	IO			DIFFIO RX R31p	DIFFOUT R31p	High Speed	F15
6	VREFB6N0	IO			DIFFIO RX R32p	DIFFOUT R32p	High Speed	G16
6	VREFB6N0	IO			DIFFIO RX R31n	DIFFOUT R31n	High Speed	G15
6	VREFB6N0	IO			DIFFIO RX R32n	DIFFOUT R32n	High Speed	F16
6	VREFB6N0	IO			DIFFIO RX R33p	DIFFOUT R33p	High Speed	E16
6	VREFB6N0	IO			DIFFIO RX R34p	DIFFOUT R34p	High Speed	D18
6	VREFB6N0	IO			DIFFIO RX R33n	DIFFOUT R33n	High Speed	D15
6	VREFB6N0	IO			DIFFIO RX R34n	DIFFOUT R34n	High Speed	E17

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
6	VREFB6N0	IO			DIFFIO RX R35p	DIFFOUT R35p	High Speed	G11
6	VREFB6N0	IO			DIFFIO RX R36p	DIFFOUT R36p	High Speed	C18
6	VREFB6N0	IO			DIFFIO RX R35n	DIFFOUT R35n	High Speed	G12
6	VREFB6N0	IO			DIFFIO RX R36n	DIFFOUT R36n	High Speed	B18
6	VREFB6N0	IO			DIFFIO RX R37p	DIFFOUT R37p	High Speed	E15
6	VREFB6N0	IO			DIFFIO RX R38p	DIFFOUT R38p	High Speed	D17
6	VREFB6N0	IO			DIFFIO RX R37n	DIFFOUT R37n	High Speed	D15
6	VREFB6N0	IO			DIFFIO RX R38n	DIFFOUT R38n	High Speed	C17
7	VREFB7N0	IO			DIFFIO RX T1p	DIFFOUT T1p	High Speed	E14
7	VREFB7N0	IO			DIFFIO RX T2p	DIFFOUT T2p	High Speed	B17
7	VREFB7N0	IO			DIFFIO RX T1n	DIFFOUT T1n	High Speed	D14
7	VREFB7N0	IO			DIFFIO RX T2n	DIFFOUT T2n	High Speed	B16
7	VREFB7N0	IO			DIFFIO RX T9p	DIFFOUT T9p	High Speed	D12
7	VREFB7N0	IO			DIFFIO RX T9n	DIFFOUT T9n	High Speed	A17
7	VREFB7N0	IO	VREFB7N0		DIFFIO RX T9n	DIFFOUT T9n	High Speed	D13
7	VREFB7N0	IO			DIFFIO RX T10p	DIFFOUT T10p	High Speed	A16
7	VREFB7N0	IO			DIFFIO RX T11p	DIFFOUT T11p	High Speed	C16
7	VREFB7N0	IO			DIFFIO RX T10n	DIFFOUT T10n	High Speed	A15
7	VREFB7N0	IO			DIFFIO RX T11n	DIFFOUT T11n	High Speed	C15
7	VREFB7N0	IO			DIFFIO RX T12p	DIFFOUT T12p	High Speed	A14
7	VREFB7N0	IO			DIFFIO RX T13p	DIFFOUT T13p	High Speed	C14
7	VREFB7N0	IO			DIFFIO RX T12n	DIFFOUT T12n	High Speed	B14
7	VREFB7N0	IO			DIFFIO RX T13n	DIFFOUT T13n	High Speed	C13
7	VREFB7N0	IO			DIFFIO RX T20p	DIFFOUT T20p	High Speed	B13
7	VREFB7N0	IO			DIFFIO RX T21p	DIFFOUT T21p	High Speed	F11
7	VREFB7N0	IO			DIFFIO RX T20n	DIFFOUT T20n	High Speed	C12
7	VREFB7N0	IO			DIFFIO RX T21n	DIFFOUT T21n	High Speed	F12
7	VREFB7N0	IO			DIFFIO RX T22p	DIFFOUT T22p	High Speed	B12
7	VREFB7N0	IO			DIFFIO RX T23p	DIFFOUT T23p	High Speed	C11
7	VREFB7N0	IO			DIFFIO RX T22n	DIFFOUT T22n	High Speed	A13
7	VREFB7N0	IO			DIFFIO RX T23n	DIFFOUT T23n	High Speed	B11
8	VREFB8N0	IO	CLK4p		DIFFIO RX T24p	DIFFOUT T24p	Low Speed	A12
8	VREFB8N0	IO			DIFFIO RX T25p	DIFFOUT T25p	Low Speed	D10
8	VREFB8N0	IO	CLK4n		DIFFIO RX T24n	DIFFOUT T24n	Low Speed	A11
8	VREFB8N0	IO			DIFFIO RX T25n	DIFFOUT T25n	Low Speed	D9
8	VREFB8N0	IO	CLK5p		DIFFIO RX T26p	DIFFOUT T26p	Low Speed	A10
8	VREFB8N0	IO			DIFFIO RX T27p	DIFFOUT T27p	Low Speed	F10
8	VREFB8N0	IO	CLK5n		DIFFIO RX T26n	DIFFOUT T26n	Low Speed	A9
8	VREFB8N0	IO			DIFFIO RX T27n	DIFFOUT T27n	Low Speed	G10
8	VREFB8N0	IO			DIFFIO RX T28p	DIFFOUT T28p	Low Speed	A8
8	VREFB8N0	IO			DIFFIO RX T29p	DIFFOUT T29p	Low Speed	B9
8	VREFB8N0	IO		DEV_CLRn	DIFFIO RX T28n	DIFFOUT T28n	Low Speed	C10
8	VREFB8N0	IO			DIFFIO RX T29n	DIFFOUT T29n	Low Speed	B8
8	VREFB8N0	IO		DEV_OE	DIFFIO RX T30p	DIFFOUT T30p	Low Speed	C9
8	VREFB8N0	IO			DIFFIO RX T30n	DIFFOUT T30n	Low Speed	D8
8	VREFB8N0	IO	VREFB8N0		DIFFIO RX T30n	DIFFOUT T30n	Low Speed	A7
8	VREFB8N0	IO					Low Speed	D7
8	VREFB8N0	IO		CONFIG_SEL			Low Speed	B7
8	VREFB8N0	IO			DIFFIO RX T31p	DIFFOUT T31p	Low Speed	G9
8	VREFB8N0	IO			DIFFIO RX T31n	DIFFOUT T31n	Low Speed	A6
8	VREFB8N0	IO	input only	nCONFIG			Low Speed	H9
8	VREFB8N0	IO			DIFFIO RX T32p	DIFFOUT T32p	Low Speed	A5
8	VREFB8N0	IO			DIFFIO RX T33p	DIFFOUT T33p	Low Speed	C6
8	VREFB8N0	IO			DIFFIO RX T32n	DIFFOUT T32n	Low Speed	C8
8	VREFB8N0	IO			DIFFIO RX T33n	DIFFOUT T33n	Low Speed	B5
8	VREFB8N0	IO			DIFFIO RX T34p	DIFFOUT T34p	Low Speed	C7
8	VREFB8N0	IO			DIFFIO RX T35p	DIFFOUT T35p	Low Speed	C5
8	VREFB8N0	IO		CRC_ERROR	DIFFIO RX T34n	DIFFOUT T34n	Low Speed	A4
8	VREFB8N0	IO			DIFFIO RX T35n	DIFFOUT T35n	Low Speed	C4
8	VREFB8N0	IO		nSTATUS	DIFFIO RX T36p	DIFFOUT T36p	Low Speed	B4
8	VREFB8N0	IO			DIFFIO RX T37p	DIFFOUT T37p	Low Speed	G8
8	VREFB8N0	IO		CONF_DONE	DIFFIO RX T36n	DIFFOUT T36n	Low Speed	A3
8	VREFB8N0	IO			DIFFIO RX T37n	DIFFOUT T37n	Low Speed	H8
8	VREFB8N0	IO			DIFFIO RX T38p	DIFFOUT T38p	Low Speed	B3
8	VREFB8N0	IO			DIFFIO RX T39p	DIFFOUT T39p	Low Speed	D6
8	VREFB8N0	IO			DIFFIO RX T38n	DIFFOUT T38n	Low Speed	A2
8	VREFB8N0	IO			DIFFIO RX T39n	DIFFOUT T39n	Low Speed	D5
	GND						Low Speed	B2
	GND							V18
	GND							V1
	GND							U4
	GND							U14
	GND							U10
	GND							R7
	GND							N5
	GND							N2
	GND							N17
	GND							N12
	GND							N10
	GND							M14
	GND							L4
	GND							K9
	GND							K6
	GND							K13
	GND							J17
	GND							J10
	GND							H14
	GND							G4
	GND							G2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
		GND						F8
		GND						F17
		GND						E6
		GND						E13
		GND						E10
		GND						D3
		GND						B6
		GND						B15
		GND						B10
		GND						A18
		GND						A1
		REFGND						E3
		VCCIO1A						H5
		VCCIO1A						G5
		VCCIO1B						K5
		VCCIO1B						J5
		VCCIO2						M5
		VCCIO2						L6
		VCCIO2						L5
		VCCIO3						P9
		VCCIO3						P8
		VCCIO3						P7
		VCCIO3						N9
		VCCIO4						P12
		VCCIO4						P11
		VCCIO5						M13
		VCCIO5						L14
		VCCIO5						L13
		VCCIO5						K14
		VCCIO6						J14
		VCCIO6						J13
		VCCIO6						H13
		VCCIO6						G14
		VCCIO6						G13
		VCCIO7						E12
		VCCIO7						E11
		VCCIO7						D11
		VCCIO8						P9
		VCCIO8						E9
		VCCIO8						E8
		VCCIO8						E7
		VCCA1						M6
		VCCA2						F14
		VCCA3						F6
		VCCA3						F4
		VCCA4						P13
		VCC ONE						L9
		VCC ONE						K10
		VCC ONE						J9
		VCC ONE						H10
		VCC ONE						N6
		VCC ONE						F13
		VCC ONE						C3
		VCC ONE						F7
		VCC ONE						N13
		ADC VREF						F3
		ANAIN1						E2

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the [Intel MAX 10 FPGA Device Family Pin Connection Guidelines](#).

Date	Version	Changes Made
February 2015	2015.02.26	Initial release.
May 2015	2015.05.08	Added note (2) to Pin List E144.
December 2016	2016.12.23	Removed I/O performance for single-ended pins.
February 2017	2017.02.21	Rebranded as Intel.
December 2017	2017.12.15	Added Pin List U324.