Pin Information for the MAX®10 10M08DF Device
Version 2017.02.21
Note *(1)*

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	V81
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	C2
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	C1
1B	VREFB1N0	IO		JTAGEN				D2
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	D3
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	D4
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	E1
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	E2
1B	VREFB1N0	IO						E3
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	F1
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	F2
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	G2
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	G1
2	VREFB2N0	IO			DIFFIO_RX_L27n	DIFFOUT_L27n	High_Speed	F3
2	VREFB2N0	IO			DIFFIO_RX_L27p	DIFFOUT_L27p	High_Speed	G3
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	H3
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	J2
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	G4
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	G5
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	J3
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	H4
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	J4
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	J5
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	H6
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	J6
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	G6
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	H7
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	J7
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	J8
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	G7
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	F7
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	G8
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	G9
5	VREFB5N0	IO			DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	F8
5	VREFB5N0	IO			DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	F9
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	E8
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	E7
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	D8
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	D9
6	VREFB6N0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	High_Speed	C8
6	VREFB6N0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	High_Speed	C9
6	VREFB6N0	IO	PLL_R_CLKOUTp		DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	C7
6	VREFB6N0	IO	PLL_R_CLKOUTn		DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	B7
8	VREFB8N0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	Low_Speed	A7
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T16n	DIFFOUT_T16n	Low_Speed	B6
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T18p	DIFFOUT_T18p	Low_Speed	A6
8	VREFB8N0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	Low_Speed	A5
8	VREFB8N0	IO		CONFIG_SEL				C6
8	VREFB8N0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	Low_Speed	A4
8	VREFB8N0	Input_only		nCONFIG				D6
8	VREFB8N0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	Low_Speed	B5
8	VREFB8N0	IO		CRC_ERROR				C5
8	VREFB8N0	IO						A3
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T24p	DIFFOUT_T24p	Low_Speed	B3
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T24n	DIFFOUT_T24n	Low_Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	Low_Speed	C4
8	VREFB8N0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	Low_Speed	C3
		GND						H9
		GND						H5
		GND						H1
		GND						F6
		GND						F4
		GND						E9
		GND						E5
		GND						D7
		GND						D1
		GND						B4
		GND						A9
		GND						A1
		VCC						H8
		VCC						H2
		VCC						B9
		VCC						B2
		VCCD_PLL2						A8
		VCCIO1_2						E4
		VCCIO3						F5
		VCCIO5_6						E6
		VCCIO8						D5
		VCCA1						J1
		VCCA2						B8
		VCCA3						B1
		VCCA4						J9

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the
MAX 10 FPGA Device Family Pin Connection Guidelines.

Date	Version	Changes Made
September 2014	2014.09.22	Initial release.
December 2014	2014.12.15	-Updated the BOOT_SEL pin name to CONFIG_SEL pin name. -Removed differential pair pins for non-differential function support.
August 2015	2015.08.21	Removed Pin List F256, Pin List U324, and Pin List F484.
December 2016	2016.12.23	Removed I/O performance for single-ended pins.
February 2017	2017.02.21	Rebranded as Intel.