Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
		VCCD_PLL7			H25			
		VCCA_PLL7			H26			
		GNDA_PLL7			F26			
		GNDA_PLL7			G26			
B2		FPLL7CLKp	INPUT		D30			
B2		FPLL7CLKn	INPUT		D29			
		NC (Note 3)			F28			
B2		IO	DIFFIO_TX51p		K25			
B2		IO	DIFFIO_TX51n		K24			
B2		IO	DIFFIO_RX50p		G28			
B2		IO	DIFFIO_RX50n		G27			
B2		IO	DIFFIO_TX50p		H28			
B2		IO	DIFFIO_TX50n		H27			
B2		IO	DIFFIO_RX49p		E30			
B2		IO	DIFFIO_RX49n		E29			
B2		IO	DIFFIO_TX49p		K27			
B2		IO	DIFFIO_TX49n		K26			
B2		IO	DIFFIO_RX48p		D32			
B2		IO	DIFFIO_RX48n		D31			
B2		IO	DIFFIO_TX48p		J27			
B2		IO	DIFFIO_TX48n		J26			
B2		IO	DIFFIO_RX47p		F30			
B2		IO	DIFFIO_RX47n		F29			
		NC (Note 7)			L28			
		NC (Note 7)			L27			
B2		IO	DIFFIO_RX46p		G30			
B2		IO	DIFFIO_RX46n		G29			
B2		IO	DIFFIO_TX46p		L26			
B2		IO	DIFFIO_TX46n		L25			
B2		IO	DIFFIO_RX45p		H30			
B2		IO	DIFFIO_RX45n		H29			
B2		IO	DIFFIO_TX45p		L24			
B2		IO	DIFFIO_TX45n		L23			
B2		IO	DIFFIO_RX44p		J30			
B2		IO	DIFFIO_RX44n		J29			
B2		IO	DIFFIO_TX44p		M25			
B2		IO	DIFFIO_TX44n		M24			
		NC (Note 3)			J28			
B2		IO	DIFFIO_RX43p		E32			
B2		IO	DIFFIO_RX43n		E31			
B2		IO	DIFFIO_TX43p		M23			
B2		IO	DIFFIO_TX43n		M22			
B2		IO	DIFFIO_RX42p		F32			
B2		IO	DIFFIO_RX42n		F31			
B2		IO	DIFFIO_TX42p		M27			
B2		IO	DIFFIO_TX42n		M26			
B2		IO	DIFFIO_RX41p		G32			
B2		IO	DIFFIO_RX41n		G31			
B2		IO	DIFFIO_TX41p		N25			
B2		IO	DIFFIO_TX41n		N24			
B2		IO	DIFFIO_RX40p		H32			
B2		IO	DIFFIO_RX40n		H31			
B2		IO	DIFFIO_TX40p		N23			
B2		IO	DIFFIO_TX40n		N22			
B2		IO	DIFFIO_RX39p		J32			
B2		IO	DIFFIO_RX39n		J31			
B2		IO	DIFFIO_TX39p		P23			
B2		IO	DIFFIO_TX39n		P22			
B2		IO	DIFFIO_RX38p		K30			
B2		IO	DIFFIO_RX38n		K29			
B2		IO	DIFFIO_TX38p		N27			
B2		IO	DIFFIO_TX38n		N26			
B2		IO	DIFFIO_RX37p		K32			
B2		IO	DIFFIO_RX37n		K31			
B2		IO	DIFFIO_TX37p		P29			
B2		IO	DIFFIO_TX37n		P28			
B2		IO	DIFFIO_RX36p		L30			
B2		IO	DIFFIO_RX36n		L29			
B2		IO	DIFFIO_TX36p		P27			
B2		IO	DIFFIO_TX36n		P26			
B2		IO	DIFFIO_RX35p		N29			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B2		IO	DIFFIO_RX35n		N28			
B2		IO	DIFFIO_TX35p		P25			
B2		IO	DIFFIO_TX35n		P24			
B2		IO	DIFFIO_RX34p		M30			
B2		IO	DIFFIO_RX34n		M29			
B2		IO	DIFFIO_TX34p		R27			
B2		IO	DIFFIO_TX34n		R26			
		NC (Note 3)			P30			
B2		IO	DIFFIO_RX33p		L32			
B2		IO	DIFFIO_RX33n		L31			
B2		IO	DIFFIO_TX33p		R23			
B2		IO	DIFFIO_TX33n		R22			
B2		IO	DIFFIO_RX32p		N31			
B2		IO	DIFFIO_RX32n		N30			
B2		IO	DIFFIO_TX32p		R25			
B2		IO	DIFFIO_TX32n		R24			
B2		IO	DIFFIO_RX31p		M32			
B2		IO	DIFFIO_RX31n		M31			
B2		IO	DIFFIO_TX31p		R29			
B2		IO	DIFFIO_TX31n		R28			
B2		IO	DIFFIO_RX30p		P32			
B2		IO	DIFFIO_RX30n		P31			
B2		IO	DIFFIO_TX30p		T28			
B2		IO	DIFFIO_TX30n		T27			
B2		IO	DIFFIO_RX29p		R31			
B2		IO	DIFFIO_RX29n		R30			
B2		IO	DIFFIO_TX29p		T23			
B2		IO	DIFFIO_TX29n		T22			
B2		IO	CLK0n/DIFFIO_RX_C0n		T31			
B2		IO	CLK0p/DIFFIO_RX_C0p		T32			
B2		CLK1n	INPUT		T29			
B2		CLK1p	INPUT		T30			
		VCCD_PLL1			U24			
		VCCA_PLL1			T24			
		GNDA_PLL1			T25			
		GNDA_PLL1			T26			
		GNDA_PLL2			U25			
		GNDA_PLL2			U26			
		VCCA_PLL2			V26			
		VCCD_PLL2			V25			
B1		IO	CLK2p/DIFFIO_RX_C1p		U32			
B1		IO	CLK2n/DIFFIO_RX_C1n		U31			
B1		CLK3p	INPUT		U30			
B1		CLK3n	INPUT		U29			
B1		IO	DIFFIO_RX28p		V31			
B1		IO	DIFFIO_RX28n		V30			
B1		IO	DIFFIO_TX28p		U23			
B1		IO	DIFFIO_TX28n		U22			
B1		IO	DIFFIO_RX27p		W32			
B1		IO	DIFFIO_RX27n		W31			
B1		IO	DIFFIO_TX27p		U28			
B1		IO	DIFFIO_TX27n		U27			
B1		IO	DIFFIO_RX26p		AA32			
B1		IO	DIFFIO_RX26n		AA31			
B1		IO	DIFFIO_TX26p		V29			
B1		IO	DIFFIO_TX26n		V28			
B1		IO	DIFFIO_RX25p		Y31			
B1		IO	DIFFIO_RX25n		Y30			
B1		IO	DIFFIO_TX25p		V24			
B1		IO	DIFFIO_TX25n		V23			
		NC (Note 3)			W30			
B1		IO	DIFFIO_RX24p		AB32			
B1		IO	DIFFIO_RX24n		AB31			
B1		IO	DIFFIO_TX24p		W29			
B1		IO	DIFFIO_TX24n		W28			
B1		IO	DIFFIO_RX23p		AA30			
B1		IO	DIFFIO_RX23n		AA29			
B1		IO	DIFFIO_TX23p		W27			
B1		IO	DIFFIO_TX23n		W26			
B1		IO	DIFFIO_RX22p		Y29			
B1		IO	DIFFIO_RX22n		Y28			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B1		IO	DIFFIO_TX22p		W25			
B1		IO	DIFFIO_TX22n		W24			
B1		IO	DIFFIO_RX21p		AB30			
B1		IO	DIFFIO_RX21n		AB29			
B1		IO	DIFFIO_TX21p		Y27			
B1		IO	DIFFIO_TX21n		Y26			
B1		IO	DIFFIO_RX20p		AC32			
B1		IO	DIFFIO_RX20n		AC31			
B1		IO	DIFFIO_TX20p		AA27			
B1		IO	DIFFIO_TX20n		AA26			
B1		IO	DIFFIO_RX19p		AB28			
B1		IO	DIFFIO_RX19n		AB27			
B1		IO	DIFFIO_TX19p		Y25			
B1		IO	DIFFIO_TX19n		Y24			
B1		IO	DIFFIO_RX18p		AD32			
B1		IO	DIFFIO_RX18n		AD31			
B1		IO	DIFFIO_TX18p		W23			
B1		IO	DIFFIO_TX18n		W22			
B1		IO	DIFFIO_RX17p		AE32			
B1		IO	DIFFIO_RX17n		AE31			
B1		IO	DIFFIO_TX17p		AD27			
B1		IO	DIFFIO_TX17n		AD26			
B1		IO	DIFFIO_RX16p		AF32			
B1		IO	DIFFIO_RX16n		AF31			
B1		IO	DIFFIO_TX16p		AC27			
B1		IO	DIFFIO_TX16n		AC26			
B1		IO	DIFFIO_RX15p		AG32			
B1		IO	DIFFIO_RX15n		AG31			
B1		IO	DIFFIO_TX15p		Y23			
B1		IO	DIFFIO_TX15n		Y22			
		NC (Note 3)			AD28			
B1		IO	DIFFIO_RX14p		AC30			
B1		IO	DIFFIO_RX14n		AC29			
B1		IO	DIFFIO_TX14p		AA25			
B1		IO	DIFFIO_TX14n		AA24			
B1		IO	DIFFIO_RX13p		AD30			
B1		IO	DIFFIO_RX13n		AD29			
B1		IO	DIFFIO_TX13p		AB26			
B1		IO	DIFFIO_TX13n		AB25			
B1		IO	DIFFIO_RX12p		AH32			
B1		IO	DIFFIO_RX12n		AH31			
B1		IO	DIFFIO_TX12p		AA23			
B1		IO	DIFFIO_TX12n		AA22			
B1		IO	DIFFIO_RX11p		AE30			
B1		IO	DIFFIO_RX11n		AE29			
B1		IO	DIFFIO_TX11p		AB24			
B1		IO	DIFFIO_TX11n		AB23			
B1		IO	DIFFIO_RX10p		AJ32			
B1		IO	DIFFIO_RX10n		AJ31			
B1		IO	DIFFIO_TX10p		AC25			
B1		IO	DIFFIO_TX10n		AC24			
B1		IO	DIFFIO_RX9p		AF30			
B1		IO	DIFFIO_RX9n		AF29			
B1		IO	DIFFIO_TX9p		AD25			
B1		IO	DIFFIO_TX9n		AD24			
B1		IO	DIFFIO_RX8p		AG30			
B1		IO	DIFFIO_RX8n		AG29			
B1		IO	DIFFIO_TX8p		AE26			
B1		IO	DIFFIO_TX8n		AE25			
B1		IO	DIFFIO_RX7p		AH30			
B1		IO	DIFFIO_RX7n		AH29			
B1		IO	DIFFIO_TX7p		AE28			
B1		IO	DIFFIO_TX7n		AE27			
		NC (Note 7)			AF28			
		NC (Note 7)			AF27			
		NC (Note 3)			AG28			
B1		FPLL8CLKn	INPUT		AJ29			
B1		FPLL8CLKp	INPUT		AJ30			
		GNDA_PLL8			AG26			
		GNDA_PLL8			AG27			
		VCCA_PLL8			AF26			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
		VCCD_PLL8			AF25			
B8	VREFB8N0	TDI		TDI	AL31			
B8	VREFB8N0	TMS		TMS	AE24			
B8	VREFB8N0	TCK		TCK	AF24			
B8	VREFB8N0	TRST		TRST	AK30			
B8	VREFB8N0	nCONFIG		nCONFIG	AL30			
B8	VREFB8N0	VCCSEL		VCCSEL	AC23			
B8	VREFB8N1	VREFB8N1 (Note 8)	VREFB8N1		AG25			
B8	VREFB8N0	IO		CS	AC22			
B8	VREFB8N0	IO		CLKUSR	AD23			
B8	VREFB8N0	IO		nWS	AE23			
B8	VREFB8N0	IO		nRS	AF23			
B8	VREFB8N0	IO			AB21			
B8	VREFB8N0	IO			AE22			
B8	VREFB8N1	IO			AF22			
B8	VREFB8N0	VREFB8N0	VREFB8N0		AK31			
		NC (Note 7)			AD22			
B8	VREFB8N0	IO	DQ17B		AH28	DQ8B		
B8	VREFB8N0	IO	DQSn17B		AK29	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQ17B		AJ28	DQ8B	DQ3B	
B8	VREFB8N0	IO	DQ17B		AM29	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQ17B		AL29	DQ8B	DQ3B	DQ1B
B8	VREFB8N0	IO	DQS17B		AK28	DQVLD8B		
B8	VREFB8N0	IO			AC21			
B8	VREFB8N3	VREFB8N3 (Note 8)	VREFB8N3		AG21			
B8	VREFB8N1	IO	DQ16B		AK27	DQ8B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQSn16B		AL28	DQSn8B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ16B		AJ27	DQ8B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ16B		AM28	DQ8B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ16B		AM27	DQ8B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQS16B		AL27	DQS8B	DQVLD3B	
B8	VREFB8N2	IO			AF21			
B8	VREFB8N1	IO	DQ15B		AK26	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQSn15B		AL26	DQ7B	DQSn3B	DQ1B
B8	VREFB8N1	IO	DQ15B		AJ26	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ15B		AM25	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQ15B		AM26	DQ7B	DQ3B	DQ1B
B8	VREFB8N1	IO	DQS15B		AL25	DQVLD7B	DQS3B	
B8	VREFB8N0	IO			AD21			
B8	VREFB8N2	IO	DQ14B		AG24	DQ7B	DQ3B	DQ1B
B8	VREFB8N2	IO	DQSn14B		AH25	DQSn7B	DQ3B	DQ1B
B8	VREFB8N2	IO	DQ14B		AH26	DQ7B	DQ3B	DQ1B
B8	VREFB8N2	IO	DQ14B		AH24	DQ7B	DQ3B	DQ1B
B8	VREFB8N2	IO	DQ14B		AK25	DQ7B	DQ3B	DQ1B
B8	VREFB8N2	IO	DQS14B		AJ25	DQS7B		
B8	VREFB8N1	IO			AB20			
B8	VREFB8N1	IO			AE21			
B8	VREFB8N3	IO			AG20			
B8	VREFB8N2	VREFB8N2	VREFB8N2		AJ24			
B8	VREFB8N2	IO			AF20			
B8	VREFB8N2	IO	DQ13B		AM24	DQ6B		
B8	VREFB8N2	IO	DQSn13B		AL24	DQ6B	DQ2B	DQSn1B
B8	VREFB8N2	IO	DQ13B		AK24	DQ6B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ13B		AK23	DQ6B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQ13B		AM23	DQ6B	DQ2B	DQ1B
B8	VREFB8N2	IO	DQS13B		AL23	DQVLD6B		DQS1B
B8	VREFB8N1	IO			AD20			
B8	VREFB8N3	IO	DQ12B		AG23	DQ6B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQSn12B		AH22	DQSn6B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQ12B		AG22	DQ6B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQ12B		AK22	DQ6B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQ12B		AJ23	DQ6B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQS12B		AJ22	DQS6B	DQVLD2B	DQVLD1B
B8	VREFB8N2	IO			AC20			
B8	VREFB8N2	IO			AB19			
B8	VREFB8N2	IO			AE20			
B8	VREFB8N3	IO			AC19			
B8	VREFB8N3	IO	DQ11B		AM22	DQ5B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQSn11B		AL22	DQ5B	DQSn2B	DQ1B
B8	VREFB8N3	IO	DQ11B		AJ21	DQ5B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQ11B		AK21	DQ5B	DQ2B	DQ1B

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B8	VREFB8N3	IO	DQ11B		AM21	DQ5B	DQ2B	DQ1B
B8	VREFB8N3	IO	DQS11B		AL21	DQVLD5B	DQS2B	
B8	VREFB8N3	IO			AD19			
B8	VREFB8N2	IO			AE19			
B8	VREFB8N3	IO			AF19			
B8	VREFB8N3	IO			AB18			
B8	VREFB8N4	IO	DQ10B		AH20	DQ5B	DQ2B	DQ1B
B8	VREFB8N4	IO	DQSn10B		AJ20	DQSn5B	DQ2B	DQ1B
B8	VREFB8N4	IO	DQ10B		AJ19	DQ5B	DQ2B	DQ1B
B8	VREFB8N4	IO	DQ10B		AH19	DQ5B	DQ2B	DQ1B
B8	VREFB8N4	IO	DQ10B		AL20	DQ5B	DQ2B	DQ1B
B8	VREFB8N4	IO	DQS10B		AK20	DQS5B		
B8	VREFB8N4	VREFB8N4	VREFB8N4		AK19			
B8	VREFB8N3	IO			AC18			
		NC (Note 7)			AD18			
		NC (Note 7)			AB17			
B8	VREFB8N4	IO		RUnLU	AG17			
B8	VREFB8N4	IO	DEV_OE	DEV_OE	AH17			
B8	VREFB8N4	IO	DEV_CLRn	DEV_CLRn	AG19			
B8	VREFB8N4	IO		nCS	AG18			
B12	VREFB8N4	IO	PLL12_FBn/OUT2n		AL19			
B12	VREFB8N4	IO	PLL12_FBp/OUT2p		AM19			
		NC (Note 7)			AC17			
B12	VREFB8N4	IO	PLL12_OUT1n		AH18			
B12	VREFB8N4	IO	PLL12_OUT1p		AJ18			
B12	VREFB8N4	IO	PLL12_OUT0n		AK18			
B12	VREFB8N4	IO	PLL12_OUT0p		AL18			
B8	VREFB8N4	IO	CLK5n		AJ17			
B8	VREFB8N4	IO	CLK5p		AK17			
B8	VREFB8N4	IO	CLK4n		AL17			
B8	VREFB8N4	IO	CLK4p		AM17			
B12		VCC_PLL12_OUT			AF16			
		VCCD_PLL12			AE18			
		VCCA_PLL12			AF18			
		GNDA_PLL12			AD17			
		GNDA_PLL12			AE17			
		GNDA_PLL6			AD16			
		GNDA_PLL6			AE16			
		VCCA_PLL6			AE15			
		VCCD_PLL6			AD15			
B10		VCC_PLL6_OUT			AF15			
B7	VREFB7N0	IO	CLK7p		AH16			
B7	VREFB7N0	IO	CLK7n		AG16			
B7	VREFB7N0	IO	CLK6p		AM16			
B7	VREFB7N0	IO	CLK6n		AL16			
B10	VREFB7N0	IO	PLL6_OUT1p		AJ15			
B10	VREFB7N0	IO	PLL6_OUT1n		AH15			
B10	VREFB7N0	IO	PLL6_OUT0p		AK16			
B10	VREFB7N0	IO	PLL6_OUT0n		AJ16			
B10	VREFB7N0	IO	PLL6_FBp/OUT2p		AL15			
B10	VREFB7N0	IO	PLL6_FBn/OUT2n		AK15			
B7	VREFB7N0	IO			AB16			
B7	VREFB7N1	IO			AC16			
B7	VREFB7N0	IO			AC15			
B7	VREFB7N0	IO	DQ9B		AM14	DQ4B		
B7	VREFB7N0	IO	DQSn9B		AL13	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	VREFB7N0	VREFB7N0		AK14			
B7	VREFB7N0	IO	DQ9B		AJ13	DQ4B	DQ1B	
B7	VREFB7N0	IO	DQ9B		AJ14	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQ9B		AL14	DQ4B	DQ1B	DQ0B
B7	VREFB7N0	IO	DQS9B		AK13	DQVLD4B		
B7	VREFB7N1	IO			AD14			
B7	VREFB7N1	IO			AE14			
B7	VREFB7N0	IO	DQ8B		AG15	DQ4B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQSn8B		AH14	DQSn4B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ8B		AF13	DQ4B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ8B		AG13	DQ4B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ8B		AH13	DQ4B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQS8B		AG14	DQS4B	DQVLD1B	
B7	VREFB7N1	IO			AB15			
B7	VREFB7N1	VREFB7N1 (Note 8)	VREFB7N1		AF14			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B7	VREFB7N1	IO	DQ7B		AM12	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQSn7B		AL12	DQ3B	DQSn1B	DQ0B
B7	VREFB7N1	IO	DQ7B		AM11	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ7B		AJ12	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ7B		AK12	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQS7B		AL11	DQVLD3B	DQS1B	
B7	VREFB7N1	IO			AC14			
B7	VREFB7N1	IO	DQ6B		AM10	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQSn6B		AK11	DQSn3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B		AL10	DQ3B	DQ1B	DQ0B
B7	VREFB7N1	IO	DQ6B		AH11	DQ3B	DQ1B	DQ0B
B7	VREFB7N2	IO	DQ6B		AJ11	DQ3B	DQ1B	DQ0B
B7	VREFB7N2	IO	DQS6B		AK10	DQS3B		
B7	VREFB7N2	IO			AD13			
B7	VREFB7N2	IO			AE13			
B7	VREFB7N2	IO	DQ5B		AG12	DQ2B		
B7	VREFB7N2	IO	DQSn5B		AG11	DQ2B	DQ0B	DQSn0B
B7	VREFB7N2	VREFB7N2	VREFB7N2		AJ9			
B7	VREFB7N2	IO	DQ5B		AF10	DQ2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ5B		AG10	DQ2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ5B		AF12	DQ2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQS5B		AF11	DQVLD2B		DQS0B
B7	VREFB7N2	IO			AB14			
B7	VREFB7N2	IO	DQ4B		AM9	DQ2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQSn4B		AL9	DQSn2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ4B		AJ8	DQ2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ4B		AK8	DQ2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQ4B		AJ10	DQ2B	DQ0B	DQ0B
B7	VREFB7N2	IO	DQS4B		AK9	DQS2B	DQVLD0B	DQVLD0B
B7	VREFB7N3	IO			AC13			
B7	VREFB7N2	IO			AE12			
B7	VREFB7N2	IO	DQ3B		AM8	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQSn3B		AL8	DQ1B	DQSn0B	DQ0B
B7	VREFB7N3	IO	DQ3B		AJ7	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQ3B		AK7	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQ3B		AM7	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQS3B		AL7	DQVLD1B	DQS0B	
B7	VREFB7N3	IO			AB13			
B7	VREFB7N2	IO			AD12			
B7	VREFB7N3	IO	DQ2B		AM6	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQSn2B		AL6	DQSn1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQ2B		AJ6	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQ2B		AK6	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQ2B		AM5	DQ1B	DQ0B	DQ0B
B7	VREFB7N3	IO	DQS2B		AL5	DQS1B		
B7	VREFB7N3	IO			AE11			
B7	VREFB7N3	IO	DQ1B		AH9	DQ0B		
B7	VREFB7N3	IO	DQSn1B		AH8	DQ0B		
B7	VREFB7N3	IO	DQ1B		AH7	DQ0B		
B7	VREFB7N4	IO	DQ1B		AH6	DQ0B		
B7	VREFB7N3	IO	DQ1B		AG9	DQ0B		
B7	VREFB7N4	IO	DQS1B		AG8	DQVLD0B		
B7	VREFB7N4	VREFB7N4	VREFB7N4		AK2			
B7	VREFB7N3	IO			AD11			
B7	VREFB7N3	IO			AC12			
B7	VREFB7N4	IO	DQ0B		AM4	DQ0B		
B7	VREFB7N4	IO	DQSn0B		AK5	DQSn0B		
B7	VREFB7N4	IO	DQ0B		AH5	DQ0B		
B7	VREFB7N4	IO	DQ0B		AJ5	DQ0B		
B7	VREFB7N4	IO	DQ0B		AL4	DQ0B		
B7	VREFB7N4	IO	DQS0B		AK4	DQS0B		
B7	VREFB7N4	IO			AC11			
B7	VREFB7N4	IO			AB12			
B7	VREFB7N4	IO			AE10			
B7	VREFB7N4	IO	RDN7		AB11			
B7	VREFB7N4	IO	RUP7		AD10			
B7	VREFB7N3	VREFB7N3 (Note 8)	VREFB7N3		AE9			
B7	VREFB7N4	PORSEL		PORSEL	AL2			
B7	VREFB7N4	nIO_PULLUP		nIO_PULLUP	AK3			
B7	VREFB7N4	PLL_ENA		PLL_ENA	AF8			
		GND			AF9			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B7	VREFB7N4	nCEO		nCEO	AL3			
		NC (Note 4)			AE8			
		NC (Note 5)			AE7			
		NC (Note 6)			AF7			
		NC (Note 6)			AG7			
		NC (Note 9)			AJ3			
		NC (Note 9)			AJ4			
		NC (Note 3)			AG5			
		NC (Note 7)			AF6			
		NC (Note 7)			AF5			
		NC (Note 7)			AD7			
		NC (Note 7)			AD6			
		NC (Note 7)			AH4			
		NC (Note 7)			AH3			
		NC (Note 7)			AD9			
		NC (Note 7)			AD8			
		NC (Note 7)			AG4			
		NC (Note 7)			AG3			
		NC (Note 7)			AC7			
		NC (Note 7)			AC6			
		NC (Note 7)			AJ2			
		NC (Note 7)			AJ1			
		NC (Note 7)			AC9			
		NC (Note 7)			AC8			
		NC (Note 7)			AE6			
		NC (Note 7)			AE5			
B6		IO			AB8			
B6		IO			AB7			
B6		IO			AH2			
B6		IO			AH1			
B6		IO			AB10			
B6		IO			AB9			
B6		IO			AF4			
B6		IO			AF3			
B6		IO			AB6			
B6		IO			AB5			
B6		IO			AG2			
B6		IO			AG1			
B6		IO			AA9			
B6		IO			AA8			
B6		IO			AD4			
B6		IO			AD3			
		NC (Note 3)			AD5			
B6		IO			AA11			
B6		IO			AA10			
B6		IO			AF2			
B6		IO			AF1			
B6		IO			Y11			
B6		IO			Y10			
B6		IO			AE4			
B6		IO			AE3			
B6		IO			AA7			
B6		IO			AA6			
B6		IO			AE2			
B6		IO			AE1			
B6		IO			W11			
B6		IO			W10			
B6		IO			AD2			
B6		IO			AD1			
B6		IO			Y9			
B6		IO			Y8			
B6		IO			AC4			
B6		IO			AC3			
B6		IO			Y7			
B6		IO			Y6			
B6		IO			AC2			
B6		IO			AC1			
B6		IO			W5			
B6		IO			W4			
B6		IO			AB4			
B6		IO			AB3			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B6		IO			W7			
B6		IO			W6			
B6		IO			AB2			
B6		IO			AB1			
B6		IO			W9			
B6		IO			W8			
B6		IO			Y5			
B6		IO			Y4			
B6		IO			V5			
B6		IO			V4			
B6		IO			AA4			
B6		IO			AA3			
		NC (Note 3)			W3			
B6		IO			V7			
B6		IO			V6			
B6		IO			AA2			
B6		IO			AA1			
B6		IO			V10			
B6		IO			V9			
B6		IO			Y3			
B6		IO			Y2			
B6		IO			U11			
B6		IO			U10			
B6		IO			W2			
B6		IO			W1			
B6		IO			U6			
B6		IO			U5			
B6		IO			V3			
B6		IO			V2			
B6		CLK9n	INPUT		U4			
B6		CLK9p	INPUT		U3			
B6		IO	CLK8n		U2			
B6		IO	CLK8p		U1			
		NC (Note 4)			U7			
		NC (Note 5)			U9			
		NC (Note 6)			U8			
		NC (Note 6)			V8			
		NC (Note 6)			R8			
		NC (Note 6)			T8			
		NC (Note 5)			R9			
		NC (Note 4)			T9			
B5		CLK11p	INPUT		T3			
B5		CLK11n	INPUT		T4			
B5		IO	CLK10p		T1			
B5		IO	CLK10n		T2			
B5		IO			T11			
B5		IO			T10			
B5		IO			P2			
B5		IO			P1			
B5		IO			T6			
B5		IO			T5			
B5		IO			R3			
B5		IO			R2			
B5		IO			R11			
B5		IO			R10			
B5		IO			M2			
B5		IO			M1			
B5		IO			R5			
B5		IO			R4			
B5		IO			N3			
B5		IO			N2			
B5		IO			R7			
B5		IO			R6			
B5		IO			L2			
B5		IO			L1			
		NC (Note 3)			P3			
B5		IO			P11			
B5		IO			P10			
B5		IO			M4			
B5		IO			M3			
B5		IO			P5			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B5		IO			P4			
B5		IO			N5			
B5		IO			N4			
B5		IO			P7			
B5		IO			P6			
B5		IO			L4			
B5		IO			L3			
B5		IO			P9			
B5		IO			P8			
B5		IO			K2			
B5		IO			K1			
B5		IO			N9			
B5		IO			N8			
B5		IO			K4			
B5		IO			K3			
B5		IO			N7			
B5		IO			N6			
B5		IO			J2			
B5		IO			J1			
B5		IO			M7			
B5		IO			M6			
B5		IO			H2			
B5		IO			H1			
B5		IO			N11			
B5		IO			N10			
B5		IO			J4			
B5		IO			J3			
B5		IO			M11			
B5		IO			M10			
B5		IO			G2			
B5		IO			G1			
B5		IO			L6			
B5		IO			L5			
B5		IO			G4			
B5		IO			G3			
		NC (Note 3)			J5			
B5		IO			M9			
B5		IO			M8			
B5		IO			F2			
B5		IO			F1			
B5		IO			L10			
B5		IO			L9			
B5		IO			F4			
B5		IO			F3			
B5		IO			L8			
B5		IO			L7			
B5		IO			E2			
B5		IO			E1			
		NC (Note 7)			K9			
		NC (Note 7)			K8			
		NC (Note 7)			E4			
		NC (Note 7)			E3			
		NC (Note 7)			K7			
		NC (Note 7)			K6			
		NC (Note 7)			D2			
		NC (Note 7)			D1			
		NC (Note 7)			J9			
		NC (Note 7)			J8			
		NC (Note 7)			H4			
		NC (Note 7)			H3			
		NC (Note 7)			J7			
		NC (Note 7)			J6			
		NC (Note 7)			G6			
		NC (Note 7)			G5			
		NC (Note 7)			H6			
		NC (Note 7)			H5			
		NC (Note 3)			F5			
		NC (Note 9)			D4			
		NC (Note 9)			D3			
		NC (Note 6)			G7			
		NC (Note 6)			G8			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
		NC (Note 5)			H8			
		NC (Note 4)			H7			
		TEMPDIODEp			G9			
		TEMPDIODEn			B3			
B4	VREFB4N0	TDO		TDO	C3			
		NC (Note 2)		MSEL3	H10			
		NC (Note 2)		MSEL2	J10			
		NC (Note 2)		MSEL1	F6			
		NC (Note 2)		MSEL0	B2			
B4	VREFB4N1	VREFB4N1 (Note 8)	VREFB4N1		H9			
B4	VREFB4N0	IO			J11			
B4	VREFB4N0	IO	RUP4		L12			
B4	VREFB4N0	IO	RDN4		K11			
B4	VREFB4N1	IO			H11			
B4	VREFB4N0	IO			K12			
B4	VREFB4N1	IO			L13			
B4	VREFB4N0	IO	DQS0T		C4	DQS0T		
B4	VREFB4N0	IO	DQ0T		B4	DQ0T		
B4	VREFB4N0	IO	DQ0T		D5	DQ0T		
B4	VREFB4N0	IO	DQ0T		E5	DQ0T		
B4	VREFB4N0	IO	DQSn0T		C5	DQSn0T		
B4	VREFB4N0	IO	DQ0T		A4	DQ0T		
B4	VREFB4N2	IO			L14			
B4	VREFB4N0	VREFB4N0	VREFB4N0		C2			
B4	VREFB4N0	IO	DQS1T		B5	DQVLD0T		
B4	VREFB4N0	IO	DQ1T		A5	DQ0T		
B4	VREFB4N1	IO	DQ1T		D6	DQ0T		
B4	VREFB4N0	IO	DQ1T		C6	DQ0T		
B4	VREFB4N1	IO	DQSn1T		B6	DQ0T		
B4	VREFB4N0	IO	DQ1T		A6	DQ0T		
B4	VREFB4N3	IO			L15			
B4	VREFB4N1	IO			K13			
B4	VREFB4N1	IO	DQS2T		D7	DQS1T		
B4	VREFB4N1	IO	DQ2T		B7	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ2T		E7	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ2T		E6	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQSn2T		C7	DQSn1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ2T		A7	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO			J12			
B4	VREFB4N1	IO	DQS3T		B8	DQVLD1T	DQS0T	
B4	VREFB4N1	IO	DQ3T		C9	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ3T		A8	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ3T		C8	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO	DQSn3T		B9	DQ1T	DQSn0T	DQ0T
B4	VREFB4N1	IO	DQ3T		A9	DQ1T	DQ0T	DQ0T
B4	VREFB4N1	IO			H12			
B4	VREFB4N2	IO			K14			
B4	VREFB4N2	IO	DQS4T		F9	DQS2T	DQVLD0T	DQVLD0T
B4	VREFB4N2	IO	DQ4T		D8	DQ2T	DQ0T	DQ0T
B4	VREFB4N2	IO	DQ4T		E8	DQ2T	DQ0T	DQ0T
B4	VREFB4N2	IO	DQ4T		F8	DQ2T	DQ0T	DQ0T
B4	VREFB4N2	IO	DQSn4T		E9	DQSn2T	DQ0T	DQ0T
B4	VREFB4N2	IO	DQ4T		F10	DQ2T	DQ0T	DQ0T
B4	VREFB4N1	IO			J13			
B4	VREFB4N3	IO			L16			
B4	VREFB4N2	IO	DQS5T		C10	DQVLD2T		DQS0T
B4	VREFB4N2	IO	DQ5T		A10	DQ2T	DQ0T	DQ0T
B4	VREFB4N2	IO	DQ5T		B10	DQ2T	DQ0T	DQ0T
B4	VREFB4N2	IO	DQ5T		D10	DQ2T	DQ0T	DQ0T
B4	VREFB4N2	VREFB4N2	VREFB4N2		D9			
B4	VREFB4N2	IO	DQSn5T		C11	DQ2T	DQ0T	DQSn0T
B4	VREFB4N2	IO	DQ5T		D11	DQ2T		
B4	VREFB4N3	IO			K15			
B4	VREFB4N2	IO	DQS6T		F11	DQS3T		
B4	VREFB4N2	IO	DQ6T		E11	DQ3T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ6T		G10	DQ3T	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ6T		G11	DQ3T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQSn6T		F12	DQSn3T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQ6T		G12	DQ3T	DQ1T	DQ0T
B4	VREFB4N2	IO			H13			
B4	VREFB4N2	IO			J14			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B4	VREFB4N3	IO	DQS7T		C12	DQVLD3T	DQS1T	
B4	VREFB4N3	IO	DQ7T		D12	DQ3T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQ7T		A11	DQ3T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQ7T		B11	DQ3T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQSn7T		B12	DQ3T	DQSn1T	DQ0T
B4	VREFB4N3	IO	DQ7T		A12	DQ3T	DQ1T	DQ0T
B4	VREFB4N3	VREFB4N3 (Note 8)	VREFB4N3		G14			
B4	VREFB4N3	IO	DQS8T		F14	DQS4T	DQVLD1T	
B4	VREFB4N3	IO	DQ8T		E13	DQ4T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQ8T		F13	DQ4T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQ8T		G13	DQ4T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQSn8T		E14	DQSn4T	DQ1T	DQ0T
B4	VREFB4N3	IO	DQ8T		F15	DQ4T	DQ1T	DQ0T
B4	VREFB4N3	IO			H14			
B4	VREFB4N4	IO			L17			
B4	VREFB4N4	IO	DQS9T		C13	DQVLD4T		
B4	VREFB4N4	IO	DQ9T		B14	DQ4T	DQ1T	DQ0T
B4	VREFB4N4	IO	DQ9T		D14	DQ4T	DQ1T	DQ0T
B4	VREFB4N4	IO	DQ9T		D13	DQ4T	DQ1T	
B4	VREFB4N4	VREFB4N4	VREFB4N4		C14			
B4	VREFB4N4	IO	DQSn9T		B13	DQ4T	DQ1T	DQ0T
B4	VREFB4N4	IO	DQ9T		A14	DQ4T		
B4	VREFB4N3	IO			J15			
B4	VREFB4N3	IO			K16			
B4	VREFB4N4	IO			K17			
B9	VREFB4N4	IO	PLL5_FBn/OUT2n		E15			
B9	VREFB4N4	IO	PLL5_FBp/OUT2p		D15			
B9	VREFB4N4	IO	PLL5_OUT0n		C15			
B9	VREFB4N4	IO	PLL5_OUT0p		B15			
B9	VREFB4N4	IO	PLL5_OUT1n		D16			
B9	VREFB4N4	IO	PLL5_OUT1p		C16			
B4	VREFB4N4	IO	CLK12n		B16			
B4	VREFB4N4	IO	CLK12p		A16			
B4	VREFB4N4	IO	CLK13n		F16			
B4	VREFB4N4	IO	CLK13p		E16			
B9		VCC_PLL5_OUT			J16			
		VCCD_PLL5			H15			
		VCCA_PLL5			G15			
		GNDA_PLL5			G16			
		GNDA_PLL5			H16			
		GNDA_PLL11			G18			
		GNDA_PLL11			H18			
		VCCA_PLL11			H17			
		VCCD_PLL11			J18			
B11		VCC_PLL11_OUT			J17			
B3	VREFB3N0	IO	CLK14p		A17			
B3	VREFB3N0	IO	CLK14n		B17			
B3	VREFB3N0	IO	CLK15p		C17			
B3	VREFB3N0	IO	CLK15n		D17			
B11	VREFB3N0	IO	PLL11_OUT0p		B18			
B11	VREFB3N0	IO	PLL11_OUT0n		C18			
B11	VREFB3N0	IO	PLL11_OUT1p		D18			
B11	VREFB3N0	IO	PLL11_OUT1n		E18			
B3	VREFB3N0	IO			K18			
B11	VREFB3N0	IO	PLL11_FBp/OUT2p		A19			
B11	VREFB3N0	IO	PLL11_FBn/OUT2n		B19			
B3	VREFB3N0	IO		PGM2	F18			
B3	VREFB3N0	IO		PGM1	F19			
B3	VREFB3N0	IO		PGM0	E17			
B3	VREFB3N0	IO		ASDO	F17			
B3	VREFB3N0	IO		nCSO	G19			
B3	VREFB3N1	IO		CRC_ERROR	G20			
B3	VREFB3N1	IO		DATA0	H19			
B3	VREFB3N1	IO		DATA1	F20			
B3	VREFB3N0	VREFB3N0	VREFB3N0		C19			
B3	VREFB3N0	IO	DQS10T		D19	DQS5T		
B3	VREFB3N0	IO	DQ10T		B20	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ10T		E19	DQ5T	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ10T		C20	DQ5T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQSn10T		D20	DQSn5T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ10T		E20	DQ5T	DQ2T	DQ1T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B3	VREFB3N2	IO			L19			
B3	VREFB3N1	IO			L18			
B3	VREFB3N2	IO			J19			
B3	VREFB3N2	IO			K19			
B3	VREFB3N1	IO	DQS11T		B21	DQVLD5T	DQS2T	
B3	VREFB3N1	IO	DQ11T		A21	DQ5T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ11T		C21	DQ5T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ11T		A22	DQ5T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQSn11T		B22	DQ5T	DQSn2T	DQ1T
B3	VREFB3N1	IO	DQ11T		C22	DQ5T	DQ2T	DQ1T
B3	VREFB3N3	IO			L20			
B3	VREFB3N2	IO			H20			
B3	VREFB3N3	IO			K20			
B3	VREFB3N1	IO	DQS12T		D22	DQS6T	DQVLD2T	DQVLD1T
B3	VREFB3N1	IO	DQ12T		D23	DQ6T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T		D21	DQ6T	DQ2T	DQ1T
B3	VREFB3N2	IO	DQ12T		F22	DQ6T	DQ2T	DQ1T
B3	VREFB3N2	IO	DQSn12T		E22	DQSn6T	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ12T		F23	DQ6T	DQ2T	DQ1T
		NC (Note 7)			L21			
B3	VREFB3N2	IO			J20			
B3	VREFB3N2	IO	DQS13T		B23	DQVLD6T		DQS1T
B3	VREFB3N2	IO	DQ13T		A23	DQ6T	DQ2T	DQ1T
B3	VREFB3N2	IO	DQ13T		C23	DQ6T	DQ2T	DQ1T
B3	VREFB3N2	IO	DQ13T		C24	DQ6T	DQ2T	DQ1T
B3	VREFB3N2	IO	DQSn13T		B24	DQ6T	DQ2T	DQSn1T
B3	VREFB3N2	IO	DQ13T		A24	DQ6T		
B3	VREFB3N4	IO			K21			
B3	VREFB3N2	VREFB3N2	VREFB3N2		D24			
		NC (Note 7)			H21			
B3	VREFB3N4	IO			J21			
B3	VREFB3N2	IO	DQS14T		B25	DQS7T		
B3	VREFB3N2	IO	DQ14T		A25	DQ7T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ14T		A26	DQ7T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ14T		D26	DQ7T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQSn14T		B26	DQSn7T	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ14T		C26	DQ7T	DQ3T	DQ1T
B3	VREFB3N2	IO			G21			
B3	VREFB3N3	IO	DQS15T		D25	DQVLD7T	DQS3T	
B3	VREFB3N3	IO	DQ15T		E24	DQ7T	DQ3T	DQ1T
B3	VREFB3N3	IO	DQ15T		C25	DQ7T	DQ3T	DQ1T
B3	VREFB3N3	IO	DQ15T		E27	DQ7T	DQ3T	DQ1T
B3	VREFB3N3	IO	DQSn15T		E25	DQ7T	DQSn3T	DQ1T
B3	VREFB3N3	IO	DQ15T		E26	DQ7T	DQ3T	DQ1T
B3	VREFB3N1	VREFB3N1 (Note 8)	VREFB3N1		F21			
B3	VREFB3N3	IO	DQS16T		B27	DQS8T	DQVLD3T	
B3	VREFB3N3	IO	DQ16T		A27	DQ8T	DQ3T	DQ1T
B3	VREFB3N3	IO	DQ16T		A28	DQ8T	DQ3T	DQ1T
B3	VREFB3N3	IO	DQ16T		D27	DQ8T	DQ3T	DQ1T
B3	VREFB3N3	IO	DQSn16T		B28	DQSn8T	DQ3T	DQ1T
B3	VREFB3N3	IO	DQ16T		C27	DQ8T	DQ3T	DQ1T
B3	VREFB3N3	IO			H22			
		NC (Note 7)			J22			
B3	VREFB3N4	IO	DQS17T		C28	DQVLD8T		
B3	VREFB3N4	IO	DQ17T		B29	DQ8T	DQ3T	DQ1T
B3	VREFB3N4	IO	DQ17T		A29	DQ8T	DQ3T	DQ1T
B3	VREFB3N4	IO	DQ17T		D28	DQ8T	DQ3T	
B3	VREFB3N4	IO	DQSn17T		C29	DQ8T	DQ3T	DQ1T
B3	VREFB3N4	IO	DQ17T		E28	DQ8T		
		NC (Note 7)			K22			
B3	VREFB3N4	VREFB3N4	VREFB3N4		C31			
B3	VREFB3N3	VREFB3N3 (Note 8)	VREFB3N3		F25			
B3	VREFB3N3	IO			G22			
B3	VREFB3N4	IO		DATA2	G23			
B3	VREFB3N4	IO		DATA3	H23			
B3	VREFB3N4	IO		DATA4	J23			
B3	VREFB3N4	IO		DATA5	L22			
B3	VREFB3N4	IO		DATA6	F24			
B3	VREFB3N4	IO		DATA7	G24			
B3	VREFB3N4	IO		RDYnBSY	H24			
B3	VREFB3N4	IO	INIT_DONE	INIT_DONE	G25			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
B3	VREFB3N4	nSTATUS		nSTATUS	B30			
B3	VREFB3N4	nCE		nCE	C30			
B3	VREFB3N4	DCLK		DCLK	B31			
B3	VREFB3N4	CONF_DONE		CONF_DONE	J25			
		VCCIO2			C32			
		VCCIO2			M28			
		VCCIO2			R32			
		VCCIO2			T21			
		VCCIO1			AA28			
		VCCIO1			AK32			
		VCCIO1			U21			
		VCCIO1			V32			
		VCCIO8			AA17			
		VCCIO8			AH21			
		VCCIO8			AM18			
		VCCIO8			AM30			
		VCCIO7			AA16			
		VCCIO7			AH12			
		VCCIO7			AM3			
		VCCIO7			AM15			
		VCCIO6			AA5			
		VCCIO6			AK1			
		VCCIO6			U12			
		VCCIO6			V1			
		VCCIO5			C1			
		VCCIO5			M5			
		VCCIO5			R1			
		VCCIO5			T12			
		VCCIO4			A3			
		VCCIO4			A15			
		VCCIO4			E12			
		VCCIO4			M16			
		VCCIO3			A18			
		VCCIO3			A30			
		VCCIO3			E21			
		VCCIO3			M17			
		VCCINT			AA12			
		VCCINT			AC10			
		VCCINT			K10			
		VCCINT			K23			
		VCCINT			M21			
		VCCINT			N13			
		VCCINT			N15			
		VCCINT			N17			
		VCCINT			N19			
		VCCINT			P14			
		VCCINT			P16			
		VCCINT			P18			
		VCCINT			P20			
		VCCINT			R13			
		VCCINT			R15			
		VCCINT			R17			
		VCCINT			R19			
		VCCINT			T14			
		VCCINT			T16			
		VCCINT			T18			
		VCCINT			T20			
		VCCINT			U13			
		VCCINT			U15			
		VCCINT			U17			
		VCCINT			U19			
		VCCINT			V14			
		VCCINT			V16			
		VCCINT			V18			
		VCCINT			V20			
		VCCINT			W13			
		VCCINT			W15			
		VCCINT			W17			
		VCCINT			W19			
		VCCINT			W21			
		VCCINT			Y14			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
		VCCINT			Y16			
		VCCINT			Y18			
		VCCINT			Y20			
		GND			A2			
		GND			A13			
		GND			A20			
		GND			A31			
		GND			AA14			
		GND			AA19			
		GND			AA21			
		GND			AB22			
		GND			AC5			
		GND			AC28			
		GND			AF17			
		GND			AG6			
		GND			AH10			
		GND			AH23			
		GND			AH27			
		GND			AL1			
		GND			AL32			
		GND			AM2			
		GND			AM13			
		GND			AM20			
		GND			AM31			
		GND			B1			
		GND			B32			
		GND			E10			
		GND			E23			
		GND			F7			
		GND			F27			
		GND			G17			
		GND			J24			
		GND			K5			
		GND			K28			
		GND			L11			
		GND			M12			
		GND			M14			
		GND			M19			
		GND			N1			
		GND			N14			
		GND			N16			
		GND			N18			
		GND			N20			
		GND			N32			
		GND			P12			
		GND			P13			
		GND			P15			
		GND			P17			
		GND			P19			
		GND			P21			
		GND			R14			
		GND			R16			
		GND			R18			
		GND			R20			
		GND			T7			
		GND			T13			
		GND			T15			
		GND			T17			
		GND			T19			
		GND			U14			
		GND			U16			
		GND			U18			
		GND			U20			
		GND			V11			
		GND			V13			
		GND			V15			
		GND			V17			
		GND			V19			
		GND			V22			
		GND			V27			
		GND			W12			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F1020	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode	DQ Group for DQS x32/x36 Mode
		GND			W14			
		GND			W16			
		GND			W18			
		GND			W20			
		GND			Y1			
		GND			Y13			
		GND			Y15			
		GND			Y17			
		GND			Y19			
		GND			Y32			
		VCCPD2			N21			
		VCCPD2			R21			
		VCCPD1			V21			
		VCCPD1			Y21			
		VCCPD8			AA18			
		VCCPD8			AA20			
		VCCPD7			AA13			
		VCCPD7			AA15			
		VCCPD6			V12			
		VCCPD6			Y12			
		VCCPD5			N12			
		VCCPD5			R12			
		VCCPD4			M13			
		VCCPD4			M15			
		VCCPD3			M18			
		VCCPD3			M20			

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix II device pin table for details.

(2) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix II device and should be connected on the board to configure the FPGA prototype.

(3) This NC pin is a VREF pin in the Stratix II device and should be connected to the VREF input reference voltage for the FPGA prototype. If the VREF is not used, connect pin to VCC or GND.

(4) This NC pin is a VCCD_PLL pin in the Stratix II device and should be connected to the VCCD_PLL power for the FPGA prototype.

(5) This NC pin is a VCCA_PLL pin in the Stratix II device and should be connected to the VCCA_PLL power for the FPGA prototype.

(6) This NC pin is a GNDA_PLL pin in the Stratix II device and should be connected to the GNDA_PLL ground for the FPGA prototype.

(7) This NC pin is an IO pin in the Stratix II device and can be left unconnected.

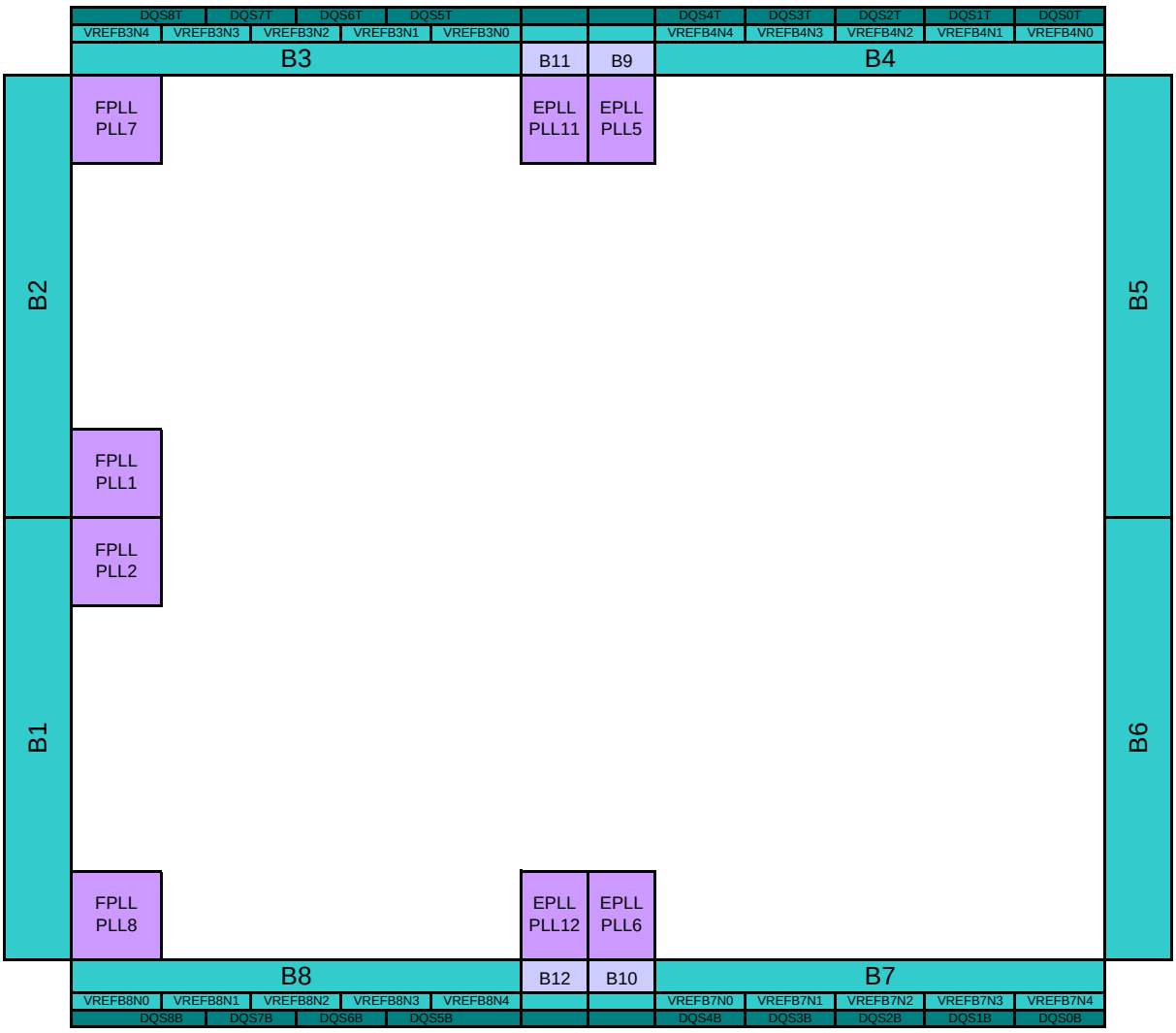
(8) This VREF pin is an IO pin in the Stratix II device and should be connected to the VREF input reference voltage for the FPGA prototype. If the VREF is not used, connect pin to VCC or GND.

(9) This NC pin is an FPLLxCLKp/n input pin in the Stratix II device and should be connected to GND for the FPGA prototype.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HyperTransport™ technology, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards including TDO and nCEO. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCPD[1..8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers all the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, and nCE. The VCCPD pins must be connected to 3.3 V and must ramp-up from 0 V to 3.3 V within 100 ms to ensure successful configuration.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[3,4,7,8]N[0..4]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All the VREF pins within a bank are shorted together. If VREF pins are not used, designers should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p & PLL5_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 9.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p & PLL6_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 10.
VCC_PLL11_OUT	Power	External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p & PLL11_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 11.
VCC_PLL12_OUT	Power	External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p & PLL12_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 12.
VCCA_PLL[1,2,5..8,11,12]	Power	Analog power for PLLs[1,2,5..8,11,12]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
VCCD_PLL[1,2,5..8,11,12]	Power	Digital power for PLLs[1,2,5..8,11,12]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1,2,5..8,11,12]	Ground	Analog ground for PLLs[1,2,5..8,11,12]. All analog GND pins should be connected to the board analog GND plane.
NC	No Connect	Do not drive signals into these pins. Exceptions are the configuration pins and the pins noted in this pin list. These pins should be properly connected on the board when prototyping with the Stratix II FPGA device. Make sure to check the pin out information for the Stratix II FPGA prototype compiled design when laying out the board to ensure compatibility between the HardCopy II device and the Stratix II FPGA prototype device.
RUP4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.
RDN4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
RUP7	I/O, Input	Reference pin for banks 7 & 8. The external precision resistor Rup must be connected to the designated RUP pin within bank 7. If not required, this pin is a regular I/O pin.
RDN7	I/O, Input	Reference pin for banks 7 & 8. The external precision resistor Rdn must be connected to the designated RDN pin within bank 7. If not required, this pin is a regular I/O pin.
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during power up. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input) and nCE. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD or ground. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
DCLK	Input	Dedicated configuration clock pin on Stratix II devices, but kept in HardCopy II for compatibility reasons. It's not required to clock this pin for HardCopy II.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy II to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Once the power up delays are done and the initialization cycle starts, CONF_DONE is released. It is not available as a user I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
nCEO	Output	Output that drives low when device initialization is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy II drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, the device enters an error state when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms. This is in addition to the Instant On delay mode chosen (i.e. instant or additional 50 ms).
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. The JTAG circuitry can be disabled by connecting TRST to GND.
Clock and PLL Pins		
CLK[1,3,9,11]p	Clock, Input	Dedicated clock input pins 1, 3, 9, & 11 that can also be used for data inputs.
CLK[1,3,9,11]n	Clock, Input	Dedicated negative terminal clock input pins for differential clock input that can also be used for data inputs.
CLK[0,2]p/DIFFIO_RX_C[0,1]p	I/O, Clock, RX channel	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[0,2]n/DIFFIO_RX_C[0,1]n	I/O, Clock, RX channel	These pins can be used as I/O pins, the negative terminal clock input pins for differential clock input, or the negative terminal data pins of differential receiver channels.
CLK[4-8,10,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-8,10,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative terminal clock input pins for differential clock input.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FPLL[7,8]CLKp	Clock, Input	Dedicated clock inputs for fast PLLs (PLLs 7 through 8) that can also be used for data inputs.
FPLL[7,8]CLKn	Clock, Input	Dedicated negative terminal associated with FPLL[7..8]CLKp pins that can also be used for data inputs.
PLL5_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5).
PLL5_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL6_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6).
PLL6_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[5..6]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[5..6].
PLL[5..6]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[5..6]_FBp or negative terminal clock output pins for differential clock output.
PLL11_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 11. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL11).
PLL11_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL11. If the clock outputs are single ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL12_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 12. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL12).
PLL12_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL12. If the clock outputs are single ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[11..12]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[11..12].
PLL[11..12]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[11..12]_FBp or negative terminal clock output pins for differential clock output.
Optional/Dual-Purpose Configuration Pins		
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
Dual-Purpose Differential & External Memory Interface Pins		

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DIFFIO_RX[7..50]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[7..46,48..51]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[0..1][T,B] (x32/x36) DQS[0..3][T,B] (x16/x18) DQS[0..8][T,B] (x8/x9) DQS[0..17][T,B] (x4)	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[0..1][T,B] (x32/x36) DQSn[0..3][T,B] (x16/x18) DQSn[0..8][T,B] (x8/x9) DQSn[0..17][T,B] (x4)	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.
DQ[0..1][T,B] (x32/x36) DQ[0..3][T,B] (x16/x18) DQ[0..8][T,B] (x8/x9) DQ[0..17][T,B] (x4)	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DQVLD[0..1][T,B] (x32/x36) DQVLD[0..3][T,B] (x16/x18) DQVLD[0..8][T,B] (x8/x9)	I/O, DQVLD	Optional data valid signal for use in external memory interfacing.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
3. The DQ/DQS groups depicted above are in x8/x9 mode. DQ/DQS support differs across the package offerings.

Version Number	Date	Changes Made
Preliminary	12/29/2004	
1.0	2/3/2005	Initial revision
1.1	2/22/2005	Corrected 8 VREF Pin Names
1.2	3/27/2007	Pintable updated to match latest Engineering pintable released 12/13/05. VREF pins and groups are updated.
		Added configuration function column for FPGA prototyping in the pin list.
		Added "DQ Group for DQS x4 Mode" description to the "Optional Function(s)" header in the pin list.
		Added footnotes in the pin list to describe the HardCopy II pins that have functions which differ from the Stratix II.
		Updated PLL numbers for VCCA_PLL, VCCD_PLL, and GNDA_PLL in the pin definition.
		Added more NC pin definition details for the configuration and noted pins.
		Updated CLK[ ]p/n DIFFIO_RX_C[ ]p/n numbers in the pin definition.
		Updated DIFFIO_RX/TX channel numbers in the pin definition.
		Updated DQS, DQSn, DQ, and DQLVD description in the pin definition.