Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		NC (Note 3)			D25		
		NC (Note 3)			D26		
		NC (Note 3)			H24		
B2		IO	DIFFIO_RX56p		C27		
B2		IO	DIFFIO_RX56n		B27		
B2		IO	DIFFIO_TX56p		H22		
B2		IO	DIFFIO_TX56n		H21		
B2		IO	DIFFIO_RX55p		E26		
B2		IO	DIFFIO_RX55n		E25		
B2		IO	DIFFIO_TX55p		F24		
B2		IO	DIFFIO_TX55n		G23		
B2		IO	DIFFIO_RX54p		F26		
B2		IO	DIFFIO_RX54n		F25		
B2		IO	DIFFIO_TX54p		J24		
B2		IO	DIFFIO_TX54n		J23		
B2		IO	DIFFIO_RX53p		G26		
B2		IO	DIFFIO_RX53n		G25		
B2		IO	DIFFIO_TX53p		K24		
B2		IO	DIFFIO_TX53n		K23		
B2		IO	DIFFIO_RX52p		H26		
B2		IO	DIFFIO_RX52n		H25		
B2		IO	DIFFIO_TX52p		J22		
B2		IO	DIFFIO_TX52n		J21		
		NC (Note 3)			K25		
B2		IO	DIFFIO_RX51p		J26		
B2		IO	DIFFIO_RX51n		J25		
B2		IO	DIFFIO_TX51p		K22		
B2		IO	DIFFIO_TX51n		K21		
B2		IO	DIFFIO_RX50p		L26		
B2		IO	DIFFIO_RX50n		L25		
B2		IO	DIFFIO_TX50p		L24		
B2		IO	DIFFIO_TX50n		L23		
B2		IO	DIFFIO_RX49p		D28		
B2		IO	DIFFIO_RX49n		D27		
B2		IO	DIFFIO_TX49p		L22		
B2		IO	DIFFIO_TX49n		L21		
B2		IO	DIFFIO_RX48p		E28		
B2		IO	DIFFIO_RX48n		E27		
B2		IO	DIFFIO_TX48p		L20		
B2		IO	DIFFIO_TX48n		K20		
B2		IO	DIFFIO_RX47p		K27		
B2		IO	DIFFIO_RX47n		K26		
B2		IO	DIFFIO_TX47p		M20		
B2		IO	DIFFIO_TX47n		M19		
B2		IO	DIFFIO_RX46p		F28		
B2		IO	DIFFIO_RX46n		F27		
B2		IO	DIFFIO_TX46p		M24		
B2		IO	DIFFIO_TX46n		M23		
B2		IO	DIFFIO_RX45p		G28		
B2		IO	DIFFIO_RX45n		G27		
B2		IO	DIFFIO_TX45p		N22		
B2		IO	DIFFIO_TX45n		M22		
B2		IO	DIFFIO_RX44p		H28		
B2		IO	DIFFIO_RX44n		H27		
B2		IO	DIFFIO_TX44p		P26		
B2		IO	DIFFIO_TX44n		N25		
		NC (Note 3)			M26		
B2		IO	DIFFIO_RX43p		J28		
B2		IO	DIFFIO_RX43n		K28		
B2		IO	DIFFIO_TX43p		P25		
B2		IO	DIFFIO_TX43n		P24		
B2		IO	DIFFIO_RX42p		L28		
B2		IO	DIFFIO_RX42n		L27		
B2		IO	DIFFIO_TX42p		N24		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B2		IO	DIFFIO_TX42n		N23		
B2		IO	DIFFIO_RX41p		M28		
B2		IO	DIFFIO_RX41n		M27		
B2		IO	DIFFIO_TX41p		P23		
B2		IO	DIFFIO_TX41n		P22		
B2		IO	CLK0n/DIFFIO_RX_C0n		P27		
B2		IO	CLK0p/DIFFIO_RX_C0p		P28		
B2		CLK1n	INPUT		N27		
B2		CLK1p	INPUT		N28		
		VCCD_PLL1			P21		
		VCCA_PLL1			P20		
		GNDA_PLL1			N19		
		GNDA_PLL1			P19		
		GNDA_PLL2			R22		
		GNDA_PLL2			R21		
		VCCA_PLL2			R20		
		VCCD_PLL2			R19		
B1		IO	CLK2p/DIFFIO_RX_C1p		R28		
B1		IO	CLK2n/DIFFIO_RX_C1n		R27		
B1		CLK3p	INPUT		T28		
B1		CLK3n	INPUT		T27		
B1		IO	DIFFIO_RX40p		U28		
B1		IO	DIFFIO_RX40n		U27		
B1		IO	DIFFIO_TX40p		R24		
B1		IO	DIFFIO_TX40n		R23		
B1		IO	DIFFIO_RX39p		V28		
B1		IO	DIFFIO_RX39n		V27		
B1		IO	DIFFIO_TX39p		T20		
B1		IO	DIFFIO_TX39n		T19		
B1		IO	DIFFIO_RX38p		W28		
B1		IO	DIFFIO_RX38n		Y28		
B1		IO	DIFFIO_TX38p		R26		
B1		IO	DIFFIO_TX38n		R25		
		NC (Note 3)			U26		
B1		IO	DIFFIO_RX37p		AA28		
B1		IO	DIFFIO_RX37n		AA27		
B1		IO	DIFFIO_TX37p		T25		
B1		IO	DIFFIO_TX37n		T24		
B1		IO	DIFFIO_RX36p		AB28		
B1		IO	DIFFIO_RX36n		AB27		
B1		IO	DIFFIO_TX36p		U20		
B1		IO	DIFFIO_TX36n		V19		
B1		IO	DIFFIO_RX35p		AC28		
B1		IO	DIFFIO_RX35n		AC27		
B1		IO	DIFFIO_TX35p		T23		
B1		IO	DIFFIO_TX35n		U22		
B1		IO	DIFFIO_RX34p		W27		
B1		IO	DIFFIO_RX34n		W26		
B1		IO	DIFFIO_TX34p		V20		
B1		IO	DIFFIO_TX34n		W20		
B1		IO	DIFFIO_RX33p		V26		
B1		IO	DIFFIO_RX33n		V25		
B1		IO	DIFFIO_TX33p		U24		
B1		IO	DIFFIO_TX33n		U23		
B1		IO	DIFFIO_RX32p		AD28		
B1		IO	DIFFIO_RX32n		AD27		
B1		IO	DIFFIO_TX32p		V22		
B1		IO	DIFFIO_TX32n		V21		
B1		IO	DIFFIO_RX31p		AE28		
B1		IO	DIFFIO_RX31n		AE27		
B1		IO	DIFFIO_TX31p		V23		
B1		IO	DIFFIO_TX31n		V24		
B1		IO	DIFFIO_RX30p		Y26		
B1		IO	DIFFIO_RX30n		Y25		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B1		IO	DIFFIO_TX30p		W22		
B1		IO	DIFFIO_TX30n		W21		
		NC (Note 3)			W25		
B1		IO	DIFFIO_RX29p		AA26		
B1		IO	DIFFIO_RX29n		AA25		
B1		IO	DIFFIO_TX29p		Y22		
B1		IO	DIFFIO_TX29n		Y21		
B1		IO	DIFFIO_RX28p		AB26		
B1		IO	DIFFIO_RX28n		AB25		
B1		IO	DIFFIO_TX28p		AB23		
B1		IO	DIFFIO_TX28n		AA22		
		NC (Note 7)			AC26		
		NC (Note 7)			AC25		
		NC (Note 7)			Y24		
		NC (Note 7)			Y23		
		NC (Note 7)			AD26		
		NC (Note 7)			AD25		
		NC (Note 7)			W24		
		NC (Note 7)			W23		
		NC (Note 7)			AG27		
		NC (Note 7)			AF27		
		NC (Note 7)			AC24		
		NC (Note 7)			AC23		
		NC (Note 3)			AA24		
		NC (Note 3)			AE26		
		NC (Note 3)			AE25		
B8		TDI		TDI	AD24		
B8		TMS		TMS	AD23		
B8		TCK		TCK	AF26		
B8		TRST		TRST	AG26		
B8		nCONFIG		nCONFIG	AB22		
B8		VCCSEL		VCCSEL	AC22		
B8		IO		CS	AB21		
B8		IO		CLKUSR	AB20		
B8		IO		nWS	AD22		
B8		IO		nRS	AD21		
		NC (Note 3)			AE24		
B8		IO			AG25		
B8		IO			AG24		
B8		IO			AF25		
B8		IO			AF24		
B8		IO			AH25		
B8		IO			AH24		
B8		IO			AE23		
		NC (Note 7)			Y20		
B8		IO			AA20		
B8		IO			Y19		
B8		IO			AC20		
		NC (Note 3)			AE21		
B8		IO			AF22		
B8		IO			AG22		
B8		IO			AE22		
B8		IO			AH23		
B8		IO			AG23		
B8		IO			AH22		
B8		IO			AA19		
B8		IO			AE20		
		NC (Note 7)			W18		
B8		IO			AB19		
B8		IO			AC19		
		NC (Note 3)			AE19		
B8		IO			AD19		
B8		IO			Y18		
B8		IO			AF21		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B8		IO			AG20		
B8		IO			AF20		
B8		IO			AH21		
B8		IO			AG21		
B8		IO			AH20		
B8		IO			AA18		
B8		IO			AC18		
B8		IO			AD18		
		NC (Note 7)			AB18		
B8		IO			AE18		
		NC (Note 3)			AE17		
B8		IO			AG19		
B8		IO			AG18		
B8		IO			AF19		
B8		IO			AF18		
B8		IO			AH19		
B8		IO			AH18		
B8		IO			Y17		
B8		IO			AD17		
B8		IO			AB17		
B8		IO			AC17		
B8		IO			Y16		
		NC (Note 3)			AD15		
		NC (Note 7)			W16		
B8		IO			W15		
B8		IO		RUnLU	AB16		
B8		IO	DEV_OE	DEV_OE	AC16		
B8		IO	DEV_CLRn	DEV_CLRn	AB15		
B8		IO		nCS	AC15		
B8		IO			AE16		
B8		IO			AD16		
B8		IO			AF17		
B8		IO			AH17		
B8		IO	CLK5n		AE15		
B8		IO	CLK5p		AF15		
B8		IO	CLK4n		AG16		
B8		IO	CLK4p		AH16		
		GNDA_PLL6			Y15		
		VCCA_PLL6			AA15		
		VCCD_PLL6			AA14		
		GNDA_PLL6			Y14		
B10		VCC_PLL6_OUT			W14		
B7		IO	CLK7p		AF14		
B7		IO	CLK7n		AE14		
B7		IO	CLK6p		AH15		
B7		IO	CLK6n		AG15		
B10		IO	PLL6_OUT1p		AH13		
B10		IO	PLL6_OUT1n		AG13		
B10		IO	PLL6_OUT0p		AH14		
B10		IO	PLL6_OUT0n		AG14		
B10		IO	PLL6_FBp/OUT2p		AH12		
B10		IO	PLL6_FBn/OUT2n		AG12		
		NC (Note 3)			AD14		
B7		IO			AH11		
B7		IO			AG11		
B7		IO			AD11		
B7		IO			AE11		
B7		IO			AF12		
		NC (Note 7)			AF11		
B7		IO			AD13		
B7		IO			AC13		
B7		IO			AB14		
B7		IO			AE13		
		NC (Note 3)			AD12		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B7		IO			AH9		
B7		IO			AH10		
B7		IO			AE10		
B7		IO			AG9		
B7		IO			AF10		
B7		IO			AG10		
B7		IO			AB13		
B7		IO			AC11		
B7		IO			AB12		
B7		IO			AC12		
		NC (Note 3)			AD10		
		NC (Note 7)			AF9		
B7		IO			AG8		
B7		IO			AE8		
B7		IO			AE9		
B7		IO			AH8		
B7		IO			AF8		
		NC (Note 7)			AB11		
B7		IO			Y13		
B7		IO			Y12		
B7		IO			AC10		
		NC (Note 3)			AD7		
B7		IO			AH6		
B7		IO			AH7		
B7		IO			AE7		
B7		IO			AF7		
B7		IO			AG6		
B7		IO			AG7		
B7		IO			AA11		
B7		IO			AB10		
		NC (Note 7)			W12		
B7		IO			Y11		
B7		IO			AD8		
B7		IO			AC9		
B7		IO			AA10		
B7		IO			AH4		
B7		IO			AH5		
		NC (Note 3)			AE5		
B7		IO			AF4		
B7		IO			AF5		
B7		IO			AG4		
B7		IO			AG5		
B7		IO			AB8		
B7		IO			AC7		
		NC (Note 7)			Y10		
B7		IO			AB9		
		NC (Note 7)			W9		
B7		IO			W10		
B7		IO			Y9		
B7		PORSEL		PORSEL	AD6		
B7		nIO_PULLUP		nIO_PULLUP	AD5		
B7		PLL_ENA		PLL_ENA	AE6		
		GND			AG3		
B7		nCEO		nCEO	AF3		
		NC (Note 3)			AE4		
		NC (Note 3)			AE3		
		NC (Note 3)			AA5		
B6		IO			AB7		
B6		IO			AB6		
B6		IO			AF2		
		NC (Note 7)			AG2		
B6		IO			AC6		
B6		IO			AC5		
B6		IO			AD4		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B6		IO			AD3		
B6		IO			Y6		
B6		IO			Y5		
		NC (Note 7)			AC4		
B6		IO			AC3		
		NC (Note 7)			AA8		
B6		IO			AA7		
B6		IO			AB4		
		NC (Note 7)			AB3		
		NC (Note 7)			Y8		
B6		IO			Y7		
B6		IO			AA4		
B6		IO			AA3		
		NC (Note 3)			W4		
		NC (Note 7)			W8		
B6		IO			W7		
B6		IO			Y4		
		NC (Note 7)			Y3		
B6		IO			W6		
B6		IO			W5		
B6		IO			AE2		
B6		IO			AE1		
B6		IO			V8		
B6		IO			V7		
B6		IO			AD2		
B6		IO			AD1		
		NC (Note 7)			V6		
B6		IO			V5		
B6		IO			V4		
B6		IO			V3		
B6		IO			U7		
B6		IO			U6		
B6		IO			W3		
B6		IO			W2		
B6		IO			V9		
		NC (Note 7)			U9		
B6		IO			AC2		
B6		IO			AC1		
B6		IO			T6		
B6		IO			U5		
B6		IO			AB2		
B6		IO			AB1		
B6		IO			T5		
B6		IO			T4		
B6		IO			AA2		
B6		IO			AA1		
		NC (Note 3)			U3		
		NC (Note 7)			R4		
B6		IO			R3		
B6		IO			Y1		
B6		IO			W1		
B6		IO			T7		
B6		IO			R7		
B6		IO			V2		
B6		IO			V1		
		NC (Note 7)			R6		
		NC (Note 7)			R5		
B6		IO			U2		
B6		IO			U1		
B6		CLK9n	INPUT		T2		
B6		CLK9p	INPUT		T1		
B6		IO	CLK8n		R2		
B6		IO	CLK8p		R1		
		NC (Note 4)			R8		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		NC (Note 5)			R9		
		NC (Note 6)			T9		
		NC (Note 6)			T10		
		NC (Note 6)			P10		
		NC (Note 6)			R10		
		NC (Note 5)			P9		
		NC (Note 4)			N10		
B5		CLK11p	INPUT		N1		
B5		CLK11n	INPUT		N2		
B5		IO	CLK10p		P1		
B5		IO	CLK10n		P2		
B5		IO			P6		
B5		IO			P5		
B5		IO			M2		
B5		IO			M1		
B5		IO			P8		
B5		IO			P7		
B5		IO			L2		
B5		IO			L1		
B5		IO			P4		
B5		IO			P3		
B5		IO			K1		
B5		IO			J1		
		NC (Note 3)			M3		
B5		IO			N5		
B5		IO			N4		
B5		IO			H2		
B5		IO			H1		
B5		IO			M7		
B5		IO			N6		
B5		IO			G2		
B5		IO			G1		
B5		IO			N9		
B5		IO			M9		
B5		IO			F2		
B5		IO			F1		
B5		IO			M6		
B5		IO			M5		
B5		IO			K3		
B5		IO			K2		
B5		IO			L10		
B5		IO			L9		
B5		IO			E2		
B5		IO			E1		
B5		IO			L8		
B5		IO			L7		
B5		IO			D2		
B5		IO			D1		
B5		IO			L6		
B5		IO			L5		
B5		IO			L4		
B5		IO			L3		
B5		IO			K8		
B5		IO			K7		
B5		IO			J4		
B5		IO			J3		
		NC (Note 3)			K4		
B5		IO			J8		
B5		IO			J7		
B5		IO			H4		
B5		IO			H3		
B5		IO			K6		
B5		IO			K5		
B5		IO			G4		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B5		IO			G3		
B5		IO			J6		
B5		IO			J5		
B5		IO			F4		
B5		IO			F3		
B5		IO			G6		
B5		IO			F5		
B5		IO			E4		
B5		IO			E3		
B5		IO			H8		
B5		IO			H7		
B5		IO			C2		
B5		IO			B2		
		NC (Note 3)			H5		
		NC (Note 3)			D3		
		NC (Note 3)			D4		
		TEMPDIODEp			D5		
		TEMPDIODEn			E5		
B4	VREFB4N0	TDO		TDO	G7		
		NC (Note 2)		MSEL3	B3		
		NC (Note 2)		MSEL2	F7		
		NC (Note 2)		MSEL1	E6		
		NC (Note 2)		MSEL0	F6		
B4	VREFB4N0	IO			E7		
B4	VREFB4N0	IO			K11		
B4	VREFB4N0	IO			G8		
B4	VREFB4N0	IO			J10		
B4	VREFB4N0	IO			G9		
B4	VREFB4N0	IO	RUP4		K9		
B4	VREFB4N0	IO	RDN4		J9		
B4	VREFB4N0	IO	DQS1T		B5		
B4	VREFB4N0	IO	DQ1T		B4		
B4	VREFB4N0	IO	DQ1T		C5		
B4	VREFB4N0	IO	DQ1T		C4		
B4	VREFB4N0	VREFB4N0	VREFB4N0		C3		
B4	VREFB4N0	IO	DQSn1T		A5		
B4	VREFB4N0	IO	DQ1T		A4		
		NC (Note 7)			H10		
B4	VREFB4N1	IO			G10		
B4	VREFB4N0	IO			E8		
B4	VREFB4N1	IO			F9		
B4	VREFB4N1	IO			H11		
B4	VREFB4N1	IO			J11		
		NC (Note 7)			K13		
B4	VREFB4N1	IO			J12		
B4	VREFB4N0	IO	DQS3T		B7	DQS0T	
B4	VREFB4N0	IO	DQ3T		B6	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ3T		C7	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ3T		D7	DQ0T	DQ0T
B4	VREFB4N1	IO	DQSn3T		A7	DQSn0T	DQ0T
B4	VREFB4N1	IO	DQ3T		A6	DQ0T	DQ0T
		NC (Note 3)			D6		
B4	VREFB4N1	IO			G11		
B4	VREFB4N2	IO			J13		
B4	VREFB4N1	IO			F10		
B4	VREFB4N2	IO			E10		
B4	VREFB4N1	IO	DQS5T		C8	DQVLD0T	DQS0T
B4	VREFB4N1	IO	DQ5T		C9	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T		D9	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T		D8	DQ0T	DQ0T
B4	VREFB4N1	IO	DQSn5T		B8	DQ0T	DQSn0T
B4	VREFB4N1	IO	DQ5T		A8	DQ0T	DQ0T
B4	VREFB4N1	VREFB4N1	VREFB4N1		E9		
		NC (Note 7)			G12		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B4	VREFB4N1	IO			F11		
B4	VREFB4N1	IO	DQS7T		B10	DQS1T	DQVLD0T
B4	VREFB4N1	IO	DQ7T		C10	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		B9	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		D10	DQ1T	DQ0T
B4	VREFB4N1	IO	DQSn7T		A10	DQSn1T	DQ0T
B4	VREFB4N2	IO	DQ7T		A9	DQ1T	DQ0T
		NC (Note 3)			E11		
B4	VREFB4N2	IO			E14		
B4	VREFB4N2	IO			F13		
B4	VREFB4N1	IO			F12		
B4	VREFB4N2	IO			E13		
B4	VREFB4N2	IO	DQS9T		C11	DQVLD1T	
B4	VREFB4N2	IO	DQ9T		C12	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		D11	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		E12	DQ1T	DQ0T
B4	VREFB4N2	VREFB4N2	VREFB4N2		D13		
B4	VREFB4N2	IO	DQSn9T		B11	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		A11	DQ1T	
B9	VREFB4N2	IO	PLL5_FBn/OUT2n		B12		
B9	VREFB4N2	IO	PLL5_FBp/OUT2p		A12		
B9	VREFB4N2	IO	PLL5_OUT0n		B14		
B9	VREFB4N2	IO	PLL5_OUT0p		A14		
B9	VREFB4N2	IO	PLL5_OUT1n		B13		
B9	VREFB4N2	IO	PLL5_OUT1p		A13		
B4	VREFB4N2	IO	CLK12n		B15		
B4	VREFB4N2	IO	CLK12p		A15		
B4	VREFB4N2	IO	CLK13n		C14		
B4	VREFB4N2	IO	CLK13p		D14		
B9		VCC_PLL5_OUT			K15		
		VCCD_PLL5			H14		
		VCCA_PLL5			H15		
		GNDA_PLL5			J14		
		GNDA_PLL5			J15		
B3	VREFB3N0	IO	CLK14p		A16		
B3	VREFB3N0	IO	CLK14n		B16		
B3	VREFB3N0	IO	CLK15p		C15		
B3	VREFB3N0	IO	CLK15n		D15		
B3	VREFB3N0	IO			A17		
B3	VREFB3N0	IO			D16		
		NC (Note 7)			C17		
B3	VREFB3N0	IO		PGM2	E15		
B3	VREFB3N0	IO		PGM1	F14		
B3	VREFB3N0	IO		PGM0	F15		
B3	VREFB3N0	IO		ASDO	G15		
B3	VREFB3N0	IO		nCSO	G14		
B3	VREFB3N0	IO		CRC_ERROR	J16		
B3	VREFB3N0	IO		DATA0	E16		
B3	VREFB3N0	IO		DATA1	F16		
B3	VREFB3N0	VREFB3N0	VREFB3N0		D17		
		NC (Note 7)			G17		
B3	VREFB3N1	IO			J17		
B3	VREFB3N0	IO			F17		
B3	VREFB3N0	IO			E17		
B3	VREFB3N0	IO	DQS11T		A18	DQS2T	
B3	VREFB3N0	IO	DQ11T		A19	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		C18	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		C19	DQ2T	DQ1T
B3	VREFB3N1	IO	DQSn11T		B18	DQSn2T	DQ1T
B3	VREFB3N1	IO	DQ11T		B19	DQ2T	DQ1T
B3	VREFB3N1	IO			K17		
		NC (Note 3)			D19		
B3	VREFB3N1	IO			D18		
B3	VREFB3N1	IO			E18		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B3	VREFB3N1	IO			G18		
B3	VREFB3N1	IO			F18		
B3	VREFB3N1	IO			H18		
B3	VREFB3N1	IO	DQS13T		A20	DQVLD2T	DQS1T
B3	VREFB3N1	IO	DQ13T		B21	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		A21	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		C20	DQ2T	DQ1T
B3	VREFB3N1	IO	DQSn13T		B20	DQ2T	DQSn1T
B3	VREFB3N1	IO	DQ13T		C21	DQ2T	DQ1T
B3	VREFB3N1	VREFB3N1	VREFB3N1		D21		
B3	VREFB3N1	IO			E19		
B3	VREFB3N2	IO			J18		
		NC (Note 7)			F19		
B3	VREFB3N1	IO			D20		
B3	VREFB3N1	IO	DQS15T		A22	DQS3T	DQVLD1T
B3	VREFB3N1	IO	DQ15T		B23	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		A23	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		D22	DQ3T	DQ1T
B3	VREFB3N2	IO	DQSn15T		B22	DQSn3T	DQ1T
B3	VREFB3N2	IO	DQ15T		C22	DQ3T	DQ1T
		NC (Note 3)			D23		
B3	VREFB3N1	IO			G19		
B3	VREFB3N1	IO			F20		
B3	VREFB3N2	IO			J19		
B3	VREFB3N1	IO			H19		
B3	VREFB3N2	IO			G20		
B3	VREFB3N2	IO	DQS17T		A24	DQVLD3T	
B3	VREFB3N2	IO	DQ17T		A25	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		C24	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		C25	DQ3T	DQ1T
B3	VREFB3N2	IO	DQSn17T		B24	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		B25	DQ3T	
B3	VREFB3N2	VREFB3N2	VREFB3N2		C26		
B3	VREFB3N2	IO			K19		
B3	VREFB3N2	IO		DATA2	E21		
B3	VREFB3N2	IO		DATA3	J20		
B3	VREFB3N2	IO		DATA4	H20		
B3	VREFB3N2	IO		DATA5	G21		
B3	VREFB3N2	IO		DATA6	E22		
B3	VREFB3N2	IO		DATA7	F23		
B3	VREFB3N2	IO		RDYnBSY	F22		
B3	VREFB3N2	IO	INIT_DONE	INIT_DONE	G22		
B3	VREFB3N2	nSTATUS		nSTATUS	B26		
B3	VREFB3N2	nCE		nCE	D24		
B3	VREFB3N2	DCLK		DCLK	E23		
B3	VREFB3N2	CONF_DONE		CONF_DONE	E24		
		VCCIO2			C28		
		VCCIO2			H23		
		VCCIO2			N26		
		VCCIO1			AA23		
		VCCIO1			AF28		
		VCCIO1			T26		
		VCCIO8			AC21		
		VCCIO8			AF16		
		VCCIO8			AH26		
		VCCIO7			AC8		
		VCCIO7			AF13		
		VCCIO7			AH3		
		VCCIO6			AA6		
		VCCIO6			AF1		
		VCCIO6			T3		
		VCCIO5			C1		
		VCCIO5			H6		
		VCCIO5			N3		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		VCCIO4			A3		
		VCCIO4			C13		
		VCCIO4			F8		
		VCCIO3			A26		
		VCCIO3			C16		
		VCCIO3			F21		
		VCCINT			K10		
		VCCINT			K12		
		VCCINT			K14		
		VCCINT			K16		
		VCCINT			K18		
		VCCINT			L11		
		VCCINT			L13		
		VCCINT			L15		
		VCCINT			L17		
		VCCINT			L19		
		VCCINT			M10		
		VCCINT			M12		
		VCCINT			M14		
		VCCINT			M16		
		VCCINT			M18		
		VCCINT			N11		
		VCCINT			N13		
		VCCINT			N15		
		VCCINT			N17		
		VCCINT			P12		
		VCCINT			P14		
		VCCINT			P16		
		VCCINT			P18		
		VCCINT			R11		
		VCCINT			R13		
		VCCINT			R15		
		VCCINT			R17		
		VCCINT			T12		
		VCCINT			T14		
		VCCINT			T16		
		VCCINT			T18		
		VCCINT			U11		
		VCCINT			U13		
		VCCINT			U15		
		VCCINT			U17		
		VCCINT			U19		
		VCCINT			V10		
		VCCINT			V12		
		VCCINT			V14		
		VCCINT			V16		
		VCCINT			V18		
		VCCINT			W11		
		VCCINT			W13		
		VCCINT			W17		
		VCCINT			W19		
		GND			A2		
		GND			A27		
		GND			AA9		
		GND			AA21		
		GND			AB5		
		GND			AB24		
		GND			AC14		
		GND			AD9		
		GND			AD20		
		GND			AE12		
		GND			AF6		
		GND			AF23		
		GND			AG1		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		GND			AG17		
		GND			AG28		
		GND			AH2		
		GND			AH27		
		GND			B1		
		GND			B17		
		GND			B28		
		GND			C6		
		GND			C23		
		GND			D12		
		GND			E20		
		GND			G5		
		GND			G13		
		GND			G16		
		GND			G24		
		GND			H9		
		GND			J2		
		GND			J27		
		GND			L12		
		GND			L14		
		GND			L16		
		GND			L18		
		GND			M4		
		GND			M11		
		GND			M13		
		GND			M15		
		GND			M17		
		GND			M25		
		GND			N7		
		GND			N12		
		GND			N14		
		GND			N16		
		GND			N18		
		GND			N20		
		GND			P11		
		GND			P13		
		GND			P15		
		GND			P17		
		GND			R12		
		GND			R14		
		GND			R16		
		GND			R18		
		GND			T11		
		GND			T13		
		GND			T15		
		GND			T17		
		GND			T22		
		GND			U4		
		GND			U10		
		GND			U12		
		GND			U14		
		GND			U16		
		GND			U18		
		GND			U25		
		GND			V11		
		GND			V13		
		GND			V15		
		GND			V17		
		GND			Y2		
		GND			Y27		
		VCCPD2			M21		
		VCCPD2			N21		
		VCCPD1			T21		
		VCCPD1			U21		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F780	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		VCCPD8			AA16		
		VCCPD8			AA17		
		VCCPD7			AA12		
		VCCPD7			AA13		
		VCCPD6			T8		
		VCCPD6			U8		
		VCCPD5			M8		
		VCCPD5			N8		
		VCCPD4			H12		
		VCCPD4			H13		
		VCCPD3			H16		
		VCCPD3			H17		

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix II device pin table for details.

(2) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix II device and should be connected on the board to configure the FPGA prototype.

(3) This NC pin is a VREF pin in the Stratix II device and should be connected to the VREF input reference voltage for the FPGA prototype. If the VREF is not used, connect pin to VCC or GND.

(4) This NC pin is a VCCD_PLL pin in the Stratix II device and should be connected to the VCCD_PLL power for the FPGA prototype.

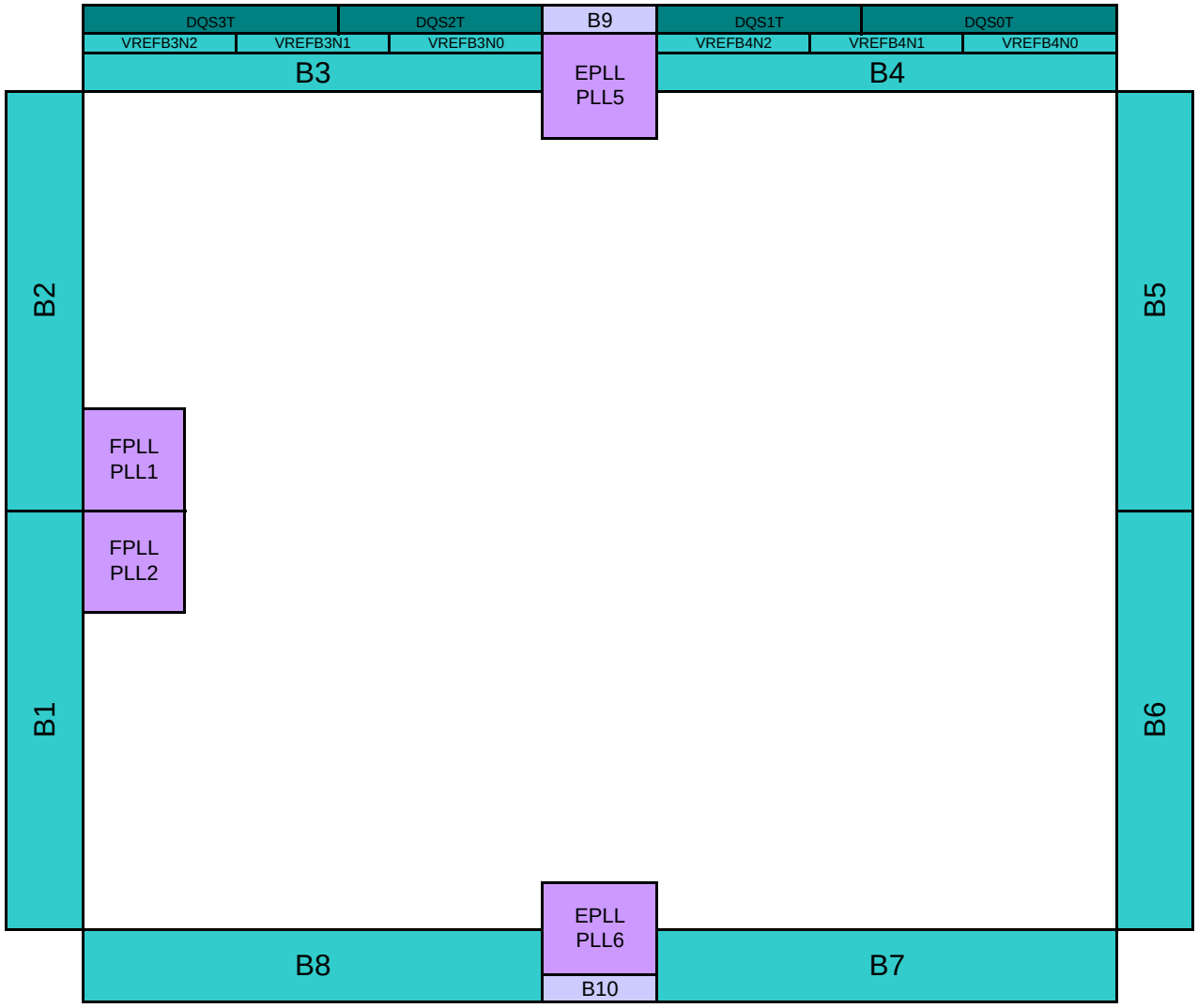
(5) This NC pin is a VCCA_PLL pin in the Stratix II device and should be connected to the VCCA_PLL power for the FPGA prototype.

(6) This NC pin is a GNDA_PLL pin in the Stratix II device and should be connected to the GNDA_PLL ground for the FPGA prototype.

(7) This NC pin is an IO pin in the Stratix II device and can be left unconnected.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HyperTransport™ technology, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards including TDO and nCEO. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCPD[1..8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers all the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, and nCE. The VCCPD pins must be connected to 3.3 V and must ramp-up from 0 V to 3.3 V within 100 ms to ensure successful configuration.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[3..4]N[0..2]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All the VREF pins within a bank are shorted togetherIf VREF pins are not used, designers should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p & PLL5_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 9.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p & PLL6_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 10.
VCCA_PLL[1,2,5,6]	Power	Analog power for PLLs[1,2,5,6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
VCCD_PLL[1,2,5,6]	Power	Digital power for PLLs[1,2,5,6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1,2,5,6]	Ground	Analog ground for PLLs[1,2,5,6]. All analog GND pins should be connected to the board analog GND plane.
NC	No Connect	Do not drive signals into these pins. Exceptions are the configuration pins and the pins noted in this pin list. These pins should be properly connected on the board when prototyping with the Stratix II FPGA device. Make sure to check the pin out information for the Stratix II FPGA prototype compiled design when laying out the board to ensure compatibility between the HardCopy II device and the Stratix II FPGA prototype device.
RUP4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.
RDN4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during power up. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input) and nCE. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD or ground. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
DCLK	Input	Dedicated configuration clock pin on Stratix II devices, but kept in HardCopy II for compatibility reasons. It's not required to clock this pin for HardCopy II.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy II to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Once the power up delays are done and the initialization cycle starts, CONF_DONE is released. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device initialization is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy II drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, the device enters an error state when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms. This is in addition to the Instant On delay mode chosen (i.e. instant or additional 50 ms).
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. The JTAG circuitry can be disabled by connecting TRST to GND.
Clock and PLL Pins		
CLK[1,3,9,11]p	Clock, Input	Dedicated clock input pins 1, 3, 9, & 11 that can also be used for data inputs.
CLK[1,3,9,11]n	Clock, Input	Dedicated negative terminal clock input pins for differential clock input that can also be used for data inputs.
CLK[0,2]p/DIFFIO_RX_C[0,1]p	I/O, Clock, RX channel	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[0,2]n/DIFFIO_RX_C[0,1]n	I/O, Clock, RX channel	These pins can be used as I/O pins, the negative terminal clock input pins for differential clock input, or the negative terminal data pins of differential receiver channels.
CLK[4-8,10,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-8,10,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative terminal clock input pins for differential clock input.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you mus drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
PLL5_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5).
PLL5_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL6_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6).
PLL6_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[5..6]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[5..6].
PLL[5..6]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[5..6]_FBp or negative terminal clock output pins for differential clock output.
Optional/Dual-Purpose Configuration Pins		
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
Dual-Purpose Differential & External Memory Interface Pins		
DIFFIO_RX[28..56]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[28..56]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pin with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[0..1]T (x16/x18) DQS[0..3]T (x8/x9) DQS[1,3,5,7,9,11,13,15,17]T (x4)	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[0..1]T (x16/x18) DQSn[0..3]T (x8/x9) DQSn[1,3,5,7,9,11,13,15,17]T (x4)	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.
DQ[0..1]T (x16/x18) DQ[0..3]T (x8/x9) DQ[1,3,5,7,9,11,13,15,17]T (x4)	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DQVLD[0..1]T (x16/x18) DQVLD[0..3]T (x8/x9)	I/O, DQVLD	Optional data valid signal for use in external memory interfacing.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
3. The DQ/DQS groups depicted above are in x8/x9 mode. DQ/DQS support differs across the package offerings.

Version Number	Date	Changes Made
Preliminary	4/7/2005	
1.0	8/19/2005	Pintable updated to match latest Engineering pintable released 8/10/05. This pintable is compatible with Quartus II Version 5.1
1.1	3/27/2007	Pintable updated to match latest Engineering pintable released 12/13/05.
		Added configuration function column for FPGA prototyping in the pin list.
		Added "DQ Group for DQS x4 Mode" description to the "Optional Function(s)" header in the pin list.
		Added footnotes in the pin list to describe the HardCopy II pins that have functions which differ from the Stratix II.
		Updated PLL numbers for VCCA_PLL, VCCD_PLL, and GNDA_PLL in the pin definition.
		Added more NC pin definition details for the configuration and noted pins.
		Updated CLK[ ]p/n DIFFIO_RX_C[ ]p/n numbers in the pin definition.
		Updated DIFFIO_RX/TX channel numbers in the pin definition.
		Updated DQS, DQSn, DQ, and DQVLD pin numbers in the pin definition.