Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		TDI		TDI			G28			
		TMS		TMS			H28			
		TRST		TRST			J28			
		TCK		TCK			F30			
		TDO		TDO			G29			
1A	VREFB1AN0	IO	PLL_L1_CLKOUT0n		DIFFIO_TX_L1n	DIFFOUT_L1n	G31			
1A	VREFB1AN0	IO	PLL_L1_FB_CLKOUT0p		DIFFIO_TX_L1p	DIFFOUT_L1p	G30			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	E32			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	E31			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J30	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	J29	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	F32	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	F31	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	K28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	K27	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	C34	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	C33	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	N25	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	M24	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	H32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	H31	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M27	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	M26	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	D34	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D33	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K30	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K29	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J32	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J31	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	L29	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	L28	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	E34	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F33	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	M28	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	N27	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	F34	DQSn5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	G33	DQS5L	DQ3L/CQn3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	N26	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	P25	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	K32	DQSn6L	DQSn3L/DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	K31	DQS6L	DQS3L/CQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	L32	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	L31	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	G34	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	H34	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	N24	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	P23	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	J34	DQSn7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	J33	DQS7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	M30	DQ7L		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	M29	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	K34			
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	K33			
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	N30	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	N29	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	N32	DQSn8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	M31	DQS8L	DQ8L/CQn8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	P29	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	P28	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	L34	DQSn9L	DQSn8L/DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	M33	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	R26	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	R25	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	P32	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	N31	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	R24	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	T23	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	M34	DQSn10L	DQ9L	DQSn8L/DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	N33	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	R28	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	R27	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	R32	DQSn11L	DQSn9L/DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	P31	DQS11L	DQS9L/CQ9L	DQ8L
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	R30	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R29	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	N34	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	P34	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	T28	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	T27	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	R34	DQSn12L	DQ10L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	R33	DQS12L	DQ10L/CQn10L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	T25	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	T24	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	T32	DQSn13L	DQSn10L/DQ10L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	R31	DQS13L	DQS10L/CQ10L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	T26	DQ13L	DQ10L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	U25	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	U32	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	U31	DQ13L	DQ10L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	T30			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	T29			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	V32			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	V31			
1C	VREFB1CN0	CLK1n	CLK1n				T34			
1C	VREFB1CN0	CLK1p	CLK1p				T33			
2C	VREFB2CN0	CLK3p	CLK3p				V33			
2C	VREFB2CN0	CLK3n	CLK3n				V34			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	W33			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	W34			
2C	VREFB2CN0	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	W28			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
2C	VREFB2CN0	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	V29			
2C	VREFB2CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AA33	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	Y34	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	W26	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	W27	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	Y31	DQS14L	DQS17L/CQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	Y32	DQSn14L	DQSn17L/DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	V24	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	V25	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AB33	DQS15L	DQ17L/CQn17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AA34	DQSn15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	W30	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	W31	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AA31	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AA32	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	Y28	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	Y29	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	AC34	DQS16L	DQS18L/CQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	AB34	DQSn16L	DQSn18L/DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	Y23	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	W24	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29p	DIFFOUT_L57p	AB31	DQS17L	DQ18L/CQn18L	DQS19L/CQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29n	DIFFOUT_L57n	AB32	DQSn17L	DQ18L	DQSn19L/DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L29p	DIFFOUT_L58p	AA29	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L29n	DIFFOUT_L58n	AA30	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AD33	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L30n	DIFFOUT_L59n	AD34	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	Y25	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L30n	DIFFOUT_L60n	Y26	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AC31	DQS18L	DQS19L/CQ19L	DQ19L/CQn19L
2C	VREFB2CN0	IO			DIFFIO_RX_L31n	DIFFOUT_L61n	AC32	DQSn18L	DQSn19L/DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AA27	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AA28	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	AE33	DQS19L	DQ19L/CQn19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32n	DIFFOUT_L63n	AE34	DQSn19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AB29	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AB30	DQ19L	DQ19L	DQ19L
2A	VREFB2AN0	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AG33			
2A	VREFB2AN0	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	AF34			
2A	VREFB2AN0	IO			DIFFIO_TX_L33p	DIFFOUT_L66p	AA24	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L33n	DIFFOUT_L66n	AA25	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AE31	DQS20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34n	DIFFOUT_L67n	AE32	DQSn20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AC28	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AC29	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AH33	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AG34	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AD30	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AD31	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AF31	DQS21L	DQS24L/CQ24L	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
2A	VREFB2AN0	IO			DIFFIO_RX_L36n	DIFFOUT_L71n	AF32	DQSn21L	DQSn24L/DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AB24	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36n	DIFFOUT_L72n	AB25	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AJ34	DQS22L	DQ24L/CQn24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	AH34	DQSn22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AB26	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AB27	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AG31	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AG32	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AE29	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AE30	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	AK33	DQS23L	DQS25L/CQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	AK34	DQSn23L	DQSn25L/DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	AD28	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	AD29	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AJ31	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AJ32	DQSn24L	DQ25L	DQSn26L/DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AF28	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AF29	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AM34	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AL34	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AE27	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AE28	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AH30	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AH31	DQSn25L	DQSn26L/DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AD26	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	AD27	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AL32	DQS26L	DQ26L/CQn26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AL33	DQSn26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AC25	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AC26	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AK31			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AK32			
2A	VREFB2AN0	IO	PLL_L4_FB_CLKOUT0p		DIFFIO_TX_L44p	DIFFOUT_L88p	AG29			
2A	VREFB2AN0	IO	PLL_L4_CLKOUT0n		DIFFIO_TX_L44n	DIFFOUT_L88n	AG30			
		nCONFIG		nCONFIG			AE25			
		nSTATUS		nSTATUS			AH28			
		CONF_DONE		CONF_DONE			AH29			
		PORSEL		PORSEL			AF26			
		nCE		nCE			AE26			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AH27	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AJ27	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AK28	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AJ28	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AJ29	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AJ26	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AM32	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AM31	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AL29	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AM29	DQ2B	DQ1B	DQ1B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AN30	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AM30	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AH26	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AF24	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH24	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG24	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AH25	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AF23	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AP33	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AN33	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AP32	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AP30	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AP31	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AN31	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AK27	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AL28	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AL27	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AL26	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AK25	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AM26	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AP28	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AN28	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AM28	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AP29	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AP27	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AN27	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AE24			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AE23			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AD22			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AC22			
3B	VREFB3BN0	IO				DIFFOUT_B25n	AH23	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B25p	AJ24	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AJ22	DQSn9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AH22	DQS9B	DQ9B/CQn9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27n	AJ23	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27p	AK22	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AM24	DQSn10B	DQSn9B/DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AL24	DQS10B	DQS9B/CQ9B	DQ9B/CQn9B
3B	VREFB3BN0	IO				DIFFOUT_B29n	AK24	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B29p	AL25	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AM23	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AL23	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AE22	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AE21	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AG21	DQSn11B	DQ10B	DQSn9B/DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AF21	DQS11B	DQ10B/CQn10B	DQS9B/CQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33n	AD21	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33p	AE20	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AP25	DQSn12B	DQSn10B/DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AN25	DQS12B	DQS10B/CQ10B	DQ9B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
3B	VREFB3BN0	IO				DIFFOUT_B35n	AP26	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B35p	AP23	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AP24	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AN24	DQ12B	DQ10B	DQ9B
3C	VREFB3CN0	IO				DIFFOUT_B49n	AL22	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B49p	AM22	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25n	DIFFOUT_B50n	AL21	DQSn17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25p	DIFFOUT_B50p	AK21	DQS17B	DQ17B/CQn17B	
3C	VREFB3CN0	IO				DIFFOUT_B51n	AJ20	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B51p	AJ21	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AP22	DQSn18B	DQSn17B/DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AN22	DQS18B	DQS17B/CQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53n	AM21	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53p	AP20	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AP21	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AN21	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B55n	AL20	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B55p	AM18	DQ19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AM19	DQSn19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AL19	DQS19B		
3C	VREFB3CN0	IO				DIFFOUT_B57n	AK18	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B57p	AL18	DQ19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B58n	AF20			
3C	VREFB3CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B58p	AF19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AE19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AD19			
3C	VREFB3CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B60n	AH19			
3C	VREFB3CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B60p	AG19			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AE18			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	AD18			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AK19			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AJ19			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AP19			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AN19			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AP18			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AN18			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AN16			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AP16			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AN15			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AP15			
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AL17			
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AM17			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	AE16			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AF16			
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AL16			
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AM16			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AD15			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	AD16			
4C	VREFB4CN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AJ16			
4C	VREFB4CN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AK16			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
4C	VREFB4CN0	IO				DIFFOUT_B72p	AL15	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B72n	AM15	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AL14	DQS20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AM14	DQSn20B		
4C	VREFB4CN0	IO				DIFFOUT_B74p	AK13	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B74n	AL13	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AH15	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AJ15	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76p	AG15	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76n	AK15	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AH14	DQS21B	DQS22B/CQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AJ14	DQSn21B	DQSn22B/DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78p	AP14	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78n	AN13	DQ22B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AN12	DQS22B	DQ22B/CQn22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AP12	DQSn22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80p	AM12	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80n	AP13	DQ22B	DQ22B	
4B	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AN10	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AP10	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94p	AP9	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94n	AP11	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B95p	AM9	DQS27B	DQS29B/CQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B95n	AN9	DQSn27B	DQSn29B/DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96p	AE15	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96n	AF15	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B97p	AF13	DQS28B	DQ29B/CQn29B	DQS30B/CQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B97n	AF14	DQSn28B	DQ29B	DQSn30B/DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98p	AE13	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98n	AE14	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50p	DIFFOUT_B99p	AK12	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50n	DIFFOUT_B99n	AL12	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100p	AK10	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100n	AM11	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51p	DIFFOUT_B101p	AL10	DQS29B	DQS30B/CQ30B	DQ30B/CQn30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51n	DIFFOUT_B101n	AL11	DQSn29B	DQSn30B/DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102p	AM8	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102n	AP8	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52p	DIFFOUT_B103p	AN7	DQS30B	DQ30B/CQn30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52n	DIFFOUT_B103n	AP7	DQSn30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104p	AP6	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104n	AM7	DQ30B	DQ30B	DQ30B
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	AC12			
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AD12			
4A	VREFB4AN0	IO				DIFFOUT_B110p	AE12			
4A	VREFB4AN0	IO				DIFFOUT_B110n	AD13			
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AH12	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AJ12	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112p	AG12	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112n	AJ13	DQ33B	DQ36B	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AH11	DQS33B	DQS36B/CQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AJ11	DQSn33B	DQSn36B/DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114p	AJ10	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114n	AL8	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AK9	DQS34B	DQ36B/CQn36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AL9	DQSn34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116p	AL7	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116n	AJ9	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AN4	DQS35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AP4	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118p	AP2	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AP5	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AN3	DQS35B	DQS37B/CQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AP3	DQSn35B	DQSn37B/DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AM6	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AN6	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AL5	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AM5	DQSn36B	DQ37B	DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AL4	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AM4	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AJ7	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AK7	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AJ6	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AK6	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AH8	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AJ8	DQSn37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AE11	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AF11	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AG9	DQS38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AH9	DQSn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AE10	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AF10	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AF8			
		nCEO		nCEO			AJ5			
		DCLK		DCLK			AL3			
		nCSO		nCSO			AE9			
		ASDO		ASDO			AH6			
5A	VREFB5AN0	IO	PLL_R4_CLKOUT0n		DIFFIO_TX_R1n	DIFFOUT_R1n	AH4			
5A	VREFB5AN0	IO	PLL_R4_FB_CLKOUT0p		DIFFIO_TX_R1p	DIFFOUT_R1p	AH5			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AK3			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AK4			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AE7	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AE8	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AM1	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AM2	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AF5	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AF6	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AJ3	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AJ4	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AC8	DQ2R	DQ1R	DQ1R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AC9	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AL1	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AL2	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AE5	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AE6	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AG3	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AG4	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AB10	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AC11	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AK1	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AJ2	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AD6	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AD7	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AJ1	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AH2	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AC7	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AB8	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AF3	DQSn5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AF4	DQS5R	DQ3R/CQn3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AB9	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AA10	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AH1	DQSn6R	DQSn3R/DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AG1	DQS6R	DQS3R/CQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AC5	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AC6	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AF1	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AF2	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AB11	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AA12	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AE3	DQSn7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AE4	DQS7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AD3	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AD4	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AE1			
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AE2			
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AB5	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AB6	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	AB3	DQSn8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AC4	DQS8R	DQ8R/CQn8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AA6	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AA7	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R14n	DIFFOUT_R28n	AD1	DQSn9R	DQSn8R/DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AC2	DQS9R	DQS8R/CQ8R	DQ8R/CQn8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15n	DIFFOUT_R29n	Y9	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	Y10	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R15n	DIFFOUT_R30n	AA3	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AB4	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R31n	Y7	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	Y8	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R32n	AC1	DQSn10R	DQ9R	DQSn8R/DQ8R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
5C	VREFB5CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AB2	DQS10R	DQ9R/CQn9R	DQS8R/CQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	Y11	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	W12	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	Y3	DQSn11R	DQSn9R/DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	AA4	DQS11R	DQS9R/CQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	Y5	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	Y6	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	AB1	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	AA1	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	W7	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	W8	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	W3	DQSn12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	Y4	DQS12R	DQ10R/CQn10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	W10	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	W11	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	Y1	DQSn13R	DQSn10R/DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	Y2	DQS13R	DQS10R/CQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	W5	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	W6	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	V3	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	V4	DQ13R	DQ10R	
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	W9			
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	V10			
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	U3			
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	U4			
5C	VREFB5CN0	CLK8n	CLK8n				W1			
5C	VREFB5CN0	CLK8p	CLK8p				W2			
6C	VREFB6CN0	CLK10p	CLK10p				U2			
6C	VREFB6CN0	CLK10n	CLK10n				U1			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	T2			
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	T1			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	U11			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	U10			
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	P2	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	R1	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	T7	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	U6	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	R4	DQS14R	DQS17R/CQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	R3	DQSn14R	DQSn17R/DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	T9	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	T8	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	N2	DQS15R	DQ17R/CQn17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	P1	DQSn15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	T5	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	T4	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	P4	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	P3	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	R7	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	R6	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	M1	DQS16R	DQS18R/CQ18R	DQ19R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	N1	DQSn16R	DQSn18R/DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	P6	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	P5	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	N4	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	N3	DQSn17R	DQ18R	DQSn19R/DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	R12	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	T11	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	L2	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	L1	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	R10	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	R9	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	M4	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	M3	DQSn18R	DQSn19R/DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	P8	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	P7	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	K2	DQS19R	DQ19R/CQn19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	K1	DQSn19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	N6	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	N5	DQ19R	DQ19R	DQ19R
6A	VREFB6AN0	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	H2			
6A	VREFB6AN0	IO			DIFFIO_RX_R33n	DIFFOUT_R65n	J1			
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	P11	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	P10	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	K4	DQS20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	K3	DQSn20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	M7	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	M6	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	G2	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	H1	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	L5	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	L4	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	J4	DQS21R	DQS24R/CQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	J3	DQSn21R	DQSn24R/DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	L7	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	L6	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	F1	DQS22R	DQ24R/CQn24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	G1	DQSn22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	N9	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	N8	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	H4	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	H3	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	K6	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	K5	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	E2	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	E1	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	N11	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	N10	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	F4	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	F3	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	J7	DQ24R	DQ25R	DQ26R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J6	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	G5	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	G4	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	K8	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	K7	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	C1	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	D1	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	M10	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	M9	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D3	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	D2	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	L9	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	L8	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	E4			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	E3			
6A	VREFB6AN0	IO	PLL_R1_FB_CLKOUT0p		DIFFIO_TX_R44p	DIFFOUT_R88p	H6			
6A	VREFB6AN0	IO	PLL_R1_CLKOUT0n		DIFFIO_TX_R44n	DIFFOUT_R88n	H5			
7A	VREFB7AN0	IO				DIFFOUT_T1n	F8	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	F6	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	E7	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	F7	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	F9	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	G8	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	C3	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	C4	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	C6	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	D6	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	B5	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	C5	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	J11	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	G9	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	G11	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	H11	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	J12	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	G10	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A2	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	B2	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A5	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	A3	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A4	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B4	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	D7	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	E8	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C9	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D9	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	E10	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	D8	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	A7	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	B7	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	A6	DQ6T	DQ3T	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
7A	VREFB7AN0	IO				DIFFOUT_T17p	C7	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A8	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B8	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	M13			
7A	VREFB7AN0	IO				DIFFOUT_T19p	L13			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	K11			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	K12			
7B	VREFB7BN0	IO				DIFFOUT_T25n	G12	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T25p	F11	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	F12	DQSn9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	F13	DQS9T	DQ9T/CQn9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27n	G13	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27p	E11	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	C11	DQSn10T	DQSn9T/DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	D11	DQS10T	DQS9T/CQ9T	DQ9T/CQn9T
7B	VREFB7BN0	IO				DIFFOUT_T29n	D13	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T29p	D10	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C12	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D12	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31n	K14	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31p	K13	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	H14	DQSn11T	DQ10T	DQSn9T/DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	J14	DQS11T	DQ10T/CQn10T	DQS9T/CQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33n	K15	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33p	L14	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	A10	DQSn12T	DQSn10T/DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	B10	DQS12T	DQS10T/CQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35n	A12	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35p	A9	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	A11	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	B11	DQ12T	DQ10T	DQ9T
7C	VREFB7CN0	IO				DIFFOUT_T49n	D14	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T49p	E13	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	E14	DQSn17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	F14	DQS17T	DQ17T/CQn17T	
7C	VREFB7CN0	IO				DIFFOUT_T51n	F15	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T51p	D15	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	A13	DQSn18T	DQSn17T/DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	B13	DQS18T	DQS17T/CQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53n	A15	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53p	C14	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	A14	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	B14	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T55n	C17	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T55p	C15	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	C16	DQSn19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	D16	DQS19T		
7C	VREFB7CN0	IO				DIFFOUT_T57n	D17	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T57p	E17	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T58n	J16			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
7C	VREFB7CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T58p	J15			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	L16			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	K16			
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	G16			
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	H16			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	K17			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	L17			
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	E16			
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	F16			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A16			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B16			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	A17			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	B17			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	B19			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	A19			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	B20			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A20			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	D18			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	C18			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	K19			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	J19			
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	D19			
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	C19			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	L19			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	L20			
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	F19			
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	E19			
8C	VREFB8CN0	IO				DIFFOUT_T72p	C20	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T72n	D20	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	D21	DQS20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	C21	DQSn20T		
8C	VREFB8CN0	IO				DIFFOUT_T74p	D22	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T74n	E22	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	G20	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	F20	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76p	E20	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76n	H20	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	G21	DQS21T	DQS22T/CQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	F21	DQSn21T	DQSn22T/DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78p	A22	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78n	A21	DQ22T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	B23	DQS22T	DQ22T/CQn22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	A23	DQSn22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80p	B22	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80n	C23	DQ22T	DQ22T	
8B	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	B25	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	A25	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94p	A24	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94n	A26	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T95p	C26	DQS27T	DQS29T/CQ29T	DQ30T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8B	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T95n	B26	DQSn27T	DQSn29T/DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96p	K20	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96n	J20	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49p	DIFFOUT_T97p	J22	DQS28T	DQ29T/CQn29T	DQS30T/CQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49n	DIFFOUT_T97n	J21	DQSn28T	DQ29T	DQSn30T/DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98p	K21	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98n	K22	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50p	DIFFOUT_T99p	D25	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50n	DIFFOUT_T99n	D24	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100p	C24	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100n	E25	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51p	DIFFOUT_T101p	E23	DQS29T	DQS30T/CQ30T	DQ30T/CQn30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51n	DIFFOUT_T101n	D23	DQSn29T	DQSn30T/DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102p	A27	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102n	C27	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52p	DIFFOUT_T103p	B28	DQS30T	DQ30T/CQn30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52n	DIFFOUT_T103n	A28	DQSn30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104p	C28	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104n	A29	DQ30T	DQ30T	DQ30T
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	M23			
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	L23			
8A	VREFB8AN0	IO				DIFFOUT_T110p	L22			
8A	VREFB8AN0	IO				DIFFOUT_T110n	K23			
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	G23	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	F23	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112p	F22	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112n	H23	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	G24	DQS33T	DQS36T/CQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	F24	DQSn33T	DQSn36T/DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114p	F25	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114n	D27	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	E26	DQS34T	DQ36T/CQn36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	D26	DQSn34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116p	F26	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116n	D28	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	B31	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	A31	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	A30	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	A33	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	B32	DQS35T	DQS37T/CQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	A32	DQSn35T	DQSn37T/DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	C29	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	B29	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	D30	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	C30	DQSn36T	DQ37T	DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	C31	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	D31	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	F28	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	E28	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	F27	DQ37T	DQ38T	DQ38T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
8A	VREFB8AN0	IO				DIFFOUT_T124n	G27	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	F29	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	E29	DQSn37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	J24	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	K24	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	H26	DQS38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	G26	DQSn38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128p	J25	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	K25	DQ38T	DQ38T	DQ38T
		GND					P21			
		GND					AF9			
		GND					V17			
		GND					B33			
		GND					AN2			
		GND					AN5			
		GND					AN8			
		GND					AN11			
		GND					AN14			
		GND					AN17			
		GND					AN20			
		GND					AN23			
		GND					AN26			
		GND					AN29			
		GND					AN32			
		GND					AM33			
		GND					AK2			
		GND					AK5			
		GND					AK8			
		GND					AK11			
		GND					AK14			
		GND					AK17			
		GND					AK20			
		GND					AK23			
		GND					AK26			
		GND					AK29			
		GND					AJ30			
		GND					AJ33			
		GND					AG2			
		GND					AG5			
		GND					AG8			
		GND					AG11			
		GND					AG14			
		GND					AG17			
		GND					AG20			
		GND					AG23			
		GND					AG26			
		GND					AF27			
		GND					AF30			
		GND					AF33			
		GND					AD2			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					AD5			
		GND					AD8			
		GND					AD11			
		GND					AD14			
		GND					AD17			
		GND					AD20			
		GND					AD23			
		GND					AC14			
		GND					AC16			
		GND					AC18			
		GND					AC20			
		GND					AC24			
		GND					AC27			
		GND					AC30			
		GND					AC33			
		GND					AB13			
		GND					AB15			
		GND					AB17			
		GND					AB19			
		GND					AB21			
		GND					AB23			
		GND					AA2			
		GND					AA5			
		GND					AA8			
		GND					AA11			
		GND					AA14			
		GND					AA16			
		GND					AA18			
		GND					AA20			
		GND					AA22			
		GND					Y13			
		GND					Y15			
		GND					Y17			
		GND					Y19			
		GND					Y21			
		GND					Y24			
		GND					Y27			
		GND					Y30			
		GND					Y33			
		GND					W14			
		GND					W16			
		GND					W18			
		GND					W20			
		GND					W22			
		GND					V2			
		GND					V5			
		GND					V8			
		GND					V11			
		GND					V12			
		GND					V13			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					V15			
		GND					V19			
		GND					V21			
		GND					V23			
		GND					U12			
		GND					U14			
		GND					U16			
		GND					U20			
		GND					U22			
		GND					U23			
		GND					U24			
		GND					U27			
		GND					U30			
		GND					U33			
		GND					T13			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					T21			
		GND					R2			
		GND					R5			
		GND					R8			
		GND					R11			
		GND					R14			
		GND					R16			
		GND					R18			
		GND					R20			
		GND					R22			
		GND					P13			
		GND					P15			
		GND					P17			
		GND					P19			
		GND					P24			
		GND					P27			
		GND					P30			
		GND					P33			
		GND					N12			
		GND					N14			
		GND					N16			
		GND					N18			
		GND					N20			
		GND					N22			
		GND					M2			
		GND					M5			
		GND					M8			
		GND					M11			
		GND					M15			
		GND					M17			
		GND					M19			
		GND					M21			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		GND					L12			
		GND					L15			
		GND					L18			
		GND					L21			
		GND					L24			
		GND					L27			
		GND					L30			
		GND					L33			
		GND					J2			
		GND					J5			
		GND					J8			
		GND					H9			
		GND					H12			
		GND					H15			
		GND					H18			
		GND					H21			
		GND					H24			
		GND					H27			
		GND					H30			
		GND					H33			
		GND					F2			
		GND					F5			
		GND					E6			
		GND					E9			
		GND					E12			
		GND					E15			
		GND					E18			
		GND					E21			
		GND					E24			
		GND					E27			
		GND					E30			
		GND					E33			
		GND					C2			
		GND					B3			
		GND					B6			
		GND					B9			
		GND					B12			
		GND					B15			
		GND					B18			
		GND					B21			
		GND					B24			
		GND					B27			
		GND					B30			
		VCC					U17			
		VCC					AB14			
		VCC					AB22			
		VCC					AA13			
		VCC					AA15			
		VCC					AA17			
		VCC					AA19			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCC					AA21			
		VCC					Y14			
		VCC					Y16			
		VCC					Y18			
		VCC					Y20			
		VCC					W15			
		VCC					W17			
		VCC					W19			
		VCC					W21			
		VCC					V14			
		VCC					V16			
		VCC					V18			
		VCC					V20			
		VCC					U15			
		VCC					U19			
		VCC					U21			
		VCC					T14			
		VCC					T16			
		VCC					T18			
		VCC					T20			
		VCC					R15			
		VCC					R17			
		VCC					R19			
		VCC					R21			
		VCC					P14			
		VCC					P16			
		VCC					P18			
		VCC					P20			
		VCC					P22			
		VCC					N13			
		VCC					N21			
		VCC					N19			
		VCC					AB16			
		VCC					AB18			
		VCC					AB20			
		VCC					Y22			
		VCC					W13			
		VCC					V22			
		VCC					U13			
		VCC					T22			
		VCC					R13			
		VCC					N15			
		VCC					N17			
		DNU					U18			
		VCCPGM					AD24			
		VCCPGM					AD10			
		TEMPDIODEn					D4			
		TEMPDIODEp					E5			
		VCC_CLKIN3C					AG18			
		VCC_CLKIN4C					AE17			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCC_CLKIN7C					H17			
		VCC_CLKIN8C					K18			
		VCCA_PLL_B1					AH18			
		VCCA_PLL_B2					AH17			
		VCCA_PLL_L2					U28			
		VCCA_PLL_L3					V28			
		VCCA_PLL_R2					U7			
		VCCA_PLL_R3					V7			
		VCCA_PLL_T1					G18			
		VCCA_PLL_T2					G17			
		VCCD_PLL_B1					AF18			
		VCCD_PLL_B2					AF17			
		VCCD_PLL_L2					U26			
		VCCD_PLL_L3					V26			
		VCCD_PLL_R2					U9			
		VCCD_PLL_R3					V9			
		VCCD_PLL_T1					J18			
		VCCD_PLL_T2					J17			
		VCCIO1A					B34			
		VCCIO1A					N28			
		VCCIO1A					L26			
		VCCIO1A					H29			
		VCCIO1A					G32			
		VCCIO1C					M32			
		VCCIO1C					V30			
		VCCIO1C					U34			
		VCCIO1C					T31			
		VCCIO2A					AB28			
		VCCIO2A					AN34			
		VCCIO2A					AH32			
		VCCIO2A					AG28			
		VCCIO2A					AD25			
		VCCIO2C					W25			
		VCCIO2C					AD32			
		VCCIO2C					W29			
		VCCIO2C					W32			
		VCCIO3A					AF25			
		VCCIO3A					AM27			
		VCCIO3A					AL30			
		VCCIO3A					AJ25			
		VCCIO3B					AF22			
		VCCIO3B					AM25			
		VCCIO3C					AH21			
		VCCIO3C					AM20			
		VCCIO3C					AJ18			
		VCCIO4A					AF12			
		VCCIO4A					AM3			
		VCCIO4A					AL6			
		VCCIO4A					AH10			
		VCCIO4B					AH13			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCIO4B					AM10			
		VCCIO4C					AG16			
		VCCIO4C					AP17			
		VCCIO4C					AM13			
		VCCIO5A					AD9			
		VCCIO5A					AN1			
		VCCIO5A					AH3			
		VCCIO5A					AG6			
		VCCIO5A					AB7			
		VCCIO5C					W4			
		VCCIO5C					AC3			
		VCCIO5C					V1			
		VCCIO5C					U5			
		VCCIO6A					H7			
		VCCIO6A					N7			
		VCCIO6A					L10			
		VCCIO6A					G3			
		VCCIO6A					B1			
		VCCIO6C					T10			
		VCCIO6C					T3			
		VCCIO6C					T6			
		VCCIO6C					L3			
		VCCIO7A					F10			
		VCCIO7A					J10			
		VCCIO7A					D5			
		VCCIO7A					C8			
		VCCIO7B					C10			
		VCCIO7B					J13			
		VCCIO7C					C13			
		VCCIO7C					G14			
		VCCIO7C					F17			
		VCCIO8A					C32			
		VCCIO8A					J23			
		VCCIO8A					G25			
		VCCIO8A					D29			
		VCCIO8B					C25			
		VCCIO8B					G22			
		VCCIO8C					A18			
		VCCIO8C					H19			
		VCCIO8C					C22			
		VCCPD1A					N23			
		VCCPD1C					R23			
		VCCPD2A					AA23			
		VCCPD2C					W23			
		VCCPD3A					AC23			
		VCCPD3B					AC21			
		VCCPD3C					AC19			
		VCCPD4A					AC13			
		VCCPD4B					AC15			
		VCCPD4C					AC17			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCPD5A					AB12			
		VCCPD5C					Y12			
		VCCPD6A					P12			
		VCCPD6C					T12			
		VCCPD7A					M12			
		VCCPD7B					M14			
		VCCPD7C					M16			
		VCCPD8A					M22			
		VCCPD8B					M20			
		VCCPD8C					M18			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				J26			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				P26			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AA26			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				V27			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AG25			
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AG22			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AH20			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AG10			
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AG13			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AH16			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AF7			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AA9			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				P9			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				U8			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				H10			
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H13			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G15			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				H25			
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				H22			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G19			
		NC					D32			
		NC					AL31			
		NC					AH7			
		NC					G7			
		NC					AK30			
		NC *(5)*					AC10			
		NC *(5)*					M25			
		NC					L11			
		NC					L25			
		NC					K26			
		NC *(4)*					G6			
		NC *(5)*					U29			
		NC *(5)*					AJ17			
		NC *(5)*					V6			
		NC *(5)*					F18			
		NC *(3)*		MSEL2			K9			
		NC *(3)*		MSEL1			J9			
		NC *(3)*		MSEL0			K10			
		VCCAUX					J27			
		VCCAUX					AG27			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix IV Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1152	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode *(2)*
		VCCAUX					AG7			
		VCCAUX					H8			

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix® IV device pin table for details.

(2) The individual index number of the pin in this column may not be the same as its companion Stratix IV device, but the functionality of the pin is fully migratable.

(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix IV device and should be connected on the board to configure the FPGA prototype.

(4) This NC pin is a VCCBAT pin in the Stratix IV device and should be connected for the FPGA prototype.

(5) This NC pin is a VCCPT pin in the Stratix IV device and should be connected for the FPGA prototype.

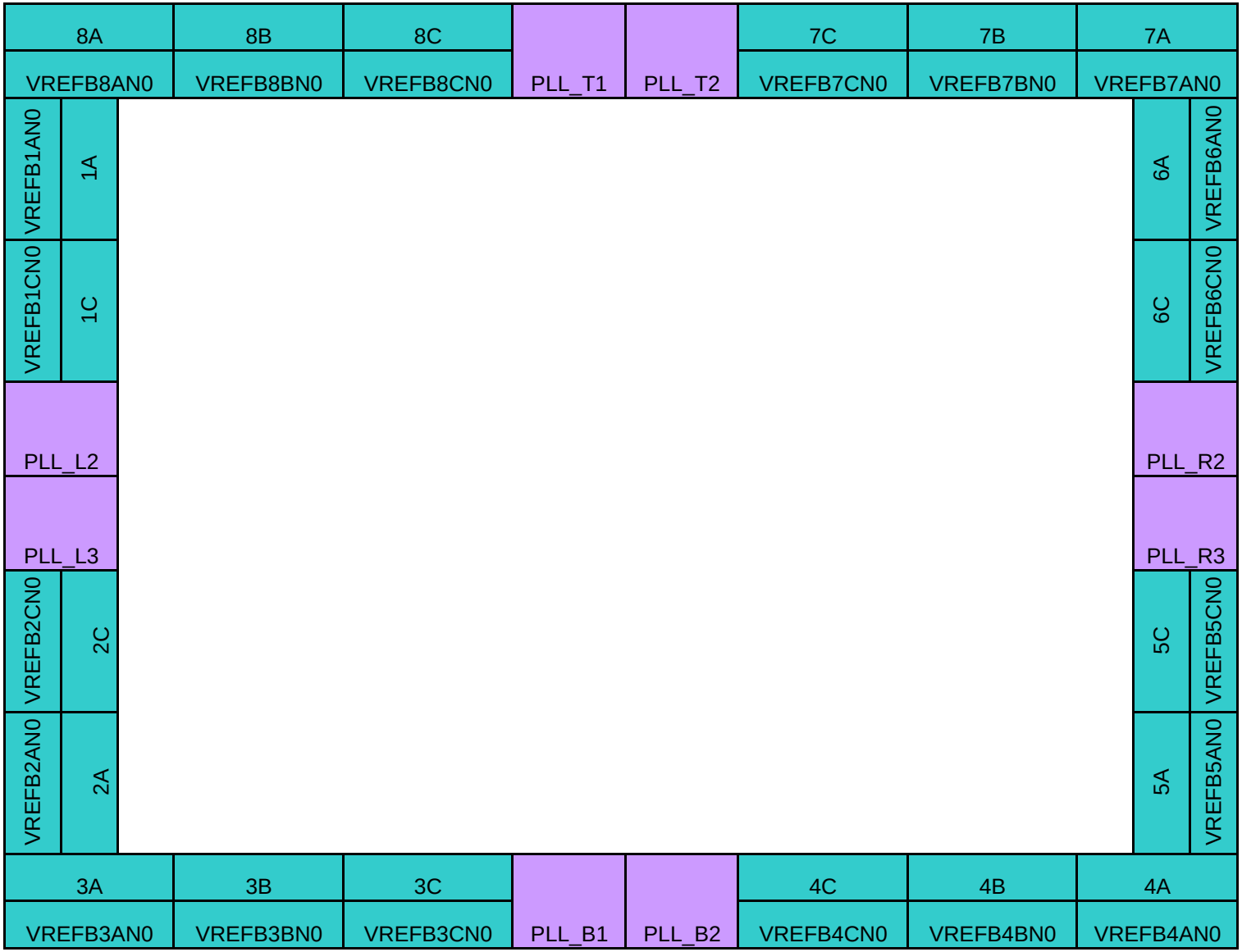
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, ,L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy IV drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
	Optional/Dual-Purpose Configuration Pins	
nCSO	I/O, Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
ASDO	I/O, Output	Dedicated control signal from Stratix IV devices, but kept in HardCopy IV for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix IV devices, but kept in HardCopy IV for compatibility reasons. It's not required to clock this pin for HardCopy IV.
	Differential I/O Pins	
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	External Memory Interface Pins	
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
	Reference Pins	
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
	Supply Pins	
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
VREFB[1:8][A,B,C]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC4E35. Refer to the pin list for the availability of pins in each density.

(2) Refer to HardCopy IV handbook for the power supply recommended operating conditions.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	7/24/2009	Initial release.