Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		TDI		TDI			E17	F24	G28		
		TMS		TMS			D17	H22	H28		
		TRST		TRST			F18	D26	J28		
		TCK		TCK			D18	C26	F30		
		TDO		TDO			A18	G24	G29		
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	B19	F26	G31		
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	C19	F25	G30		
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	A20	C28	E32		
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	A19	D27	E31		
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G17	G26	J30	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G16	G25	J29	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B20	B28	F32	DQSn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C20	C27	F31	DQS1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	D19	H25	K28	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	E19	J24	K27	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	A22	D28	C34	DQSn2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	A21	E28	C33	DQS2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	D20	J23	N25	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	E20	J22	M24	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	B22	F28	H32	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	C22	F27	H31	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	F16	K21	M27	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	F15	K20	M26	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	C21	G28	D34	DQSn3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D21	G27	D33	DQS3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	H16	K26	K30	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	G15	K25	K29	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	D22	J26	J32		
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	E22	J25	J31		
1A	VREFB1AN0	IO						K24	N26		
1A	VREFB1AN0	IO						K23	P25		
1A	VREFB1AN0	IO						H28	K32		
1A	VREFB1AN0	IO						J27	K31		
1A	VREFB1AN0	IO						L23	L32		
1A	VREFB1AN0	IO						L22	L31		
1A	VREFB1AN0	IO						J28	G34		
1A	VREFB1AN0	IO						K27	H34		
1A	VREFB1AN0	IO							N24		
1A	VREFB1AN0	IO							P23		
1A	VREFB1AN0	IO							J34		
1A	VREFB1AN0	IO							J33		
1A	VREFB1AN0	IO							M30		
1A	VREFB1AN0	IO							M29		
1A	VREFB1AN0	IO							K34		
1A	VREFB1AN0	IO							K33		
1A	VREFB1AN0	IO							E34		
1A	VREFB1AN0	IO							F33		
1A	VREFB1AN0	IO							F34		
1A	VREFB1AN0	IO							L28		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
1A	VREFB1AN0	IO							L29		
1A	VREFB1AN0	IO							G33		
1A	VREFB1AN0	IO							N27		
1A	VREFB1AN0	IO							M28		
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	G19	M23	R28		
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	H19	M22	R27		
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	F20	L26	R32	DQSn5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	G20	L25	P31	DQS5L	
1C	VREFB1CN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	H20	M21	R30	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	J19	M20	R29	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	F22	K28	N34	DQ5L	
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	F21	L28	P34	DQ5L	
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	J18	N21	T28	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	J17	N20	T27	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	K20	M26	R34	DQSn6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	K19	M25	R33	DQS6L	DQ5L/CQn5L
1C	VREFB1CN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	H17	N25	T25	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	J16	M24	T24	DQ6L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	J21	M28	T32	DQSn7L	DQSn5L/DQ5L
1C	VREFB1CN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	J20	M27	R31	DQS7L	DQS5L/CQ5L
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	K16	N23	T26	DQ7L	DQ5L
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	L16	P23	U25	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	G22	P25	U32	DQ7L	DQ5L
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	G21	N24	U31	DQ7L	DQ5L
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	L20	P20	T30		
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	L19	P19	T29		
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	J22	N27	V32		
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	K21	N26	V31		
1C	VREFB1CN0	CLK1n	CLK1n				K22	N28	T34		
1C	VREFB1CN0	CLK1p	CLK1p				L22	P28	T33		
1C	VREFB1CN0	IO							N30		
1C	VREFB1CN0	IO							N29		
1C	VREFB1CN0	IO							N32		
1C	VREFB1CN0	IO							M31		
1C	VREFB1CN0	IO							P29		
1C	VREFB1CN0	IO							P28		
1C	VREFB1CN0	IO							L34		
1C	VREFB1CN0	IO							M33		
1C	VREFB1CN0	IO							R26		
1C	VREFB1CN0	IO							R25		
1C	VREFB1CN0	IO							P32		
1C	VREFB1CN0	IO							N31		
1C	VREFB1CN0	IO							R24		
1C	VREFB1CN0	IO							T23		
1C	VREFB1CN0	IO							M34		
1C	VREFB1CN0	IO							N33		
2C	VREFB2CN0	CLK3p	CLK3p				M19	R27	V33		
2C	VREFB2CN0	CLK3n	CLK3n				M20	R28	V34		
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	M21	U28	W33		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	M22	T28	W34		
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	M15	R20	W28		
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	M16	R21	V29		
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	N21	R26	AA33	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	N22	T27	Y34	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	P16	T25	W26	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	P17	R25	W27	DQ8L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	N19	V27	Y31	DQS8L	DQS10L/CQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	N20	V28	Y32	DQSn8L	DQSn10L/DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	N16	T20	V24	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	N17	T21	V25	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	R21	V26	AB33	DQS9L	DQ10L/CQn10L
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	R22	U26	AA34	DQSn9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	P19	T24	W30	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	P20	U25	W31	DQ9L	DQ10L
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	U22	W27	AA31	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	T22	W28	AA32	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	R19	T22	Y28	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	R20	T23	Y29	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	T20	V24	AC34	DQS10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	T21	V25	AB34	DQSn10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	R18	V23	Y23		
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	T19	U23	W24		
2C	VREFB2CN0	IO							AB31		
2C	VREFB2CN0	IO							AB32		
2C	VREFB2CN0	IO							AA29		
2C	VREFB2CN0	IO							AA30		
2C	VREFB2CN0	IO							AD33		
2C	VREFB2CN0	IO							AD34		
2C	VREFB2CN0	IO							Y25		
2C	VREFB2CN0	IO							Y26		
2C	VREFB2CN0	IO							AC31		
2C	VREFB2CN0	IO							AC32		
2C	VREFB2CN0	IO							AA27		
2C	VREFB2CN0	IO							AA28		
2C	VREFB2CN0	IO							AE33		
2C	VREFB2CN0	IO							AE34		
2C	VREFB2CN0	IO							AB29		
2C	VREFB2CN0	IO							AB30		
2A	VREFB2AN0	IO							AG33		
2A	VREFB2AN0	IO							AF34		
2A	VREFB2AN0	IO							AA24		
2A	VREFB2AN0	IO							AA25		
2A	VREFB2AN0	IO							AE31		
2A	VREFB2AN0	IO							AE32		
2A	VREFB2AN0	IO							AC28		
2A	VREFB2AN0	IO							AC29		
2A	VREFB2AN0	IO							AH33		
2A	VREFB2AN0	IO							AG34		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
2A	VREFB2AN0	IO							AD30		
2A	VREFB2AN0	IO							AD31		
2A	VREFB2AN0	IO							AF31		
2A	VREFB2AN0	IO							AF32		
2A	VREFB2AN0	IO							AB24		
2A	VREFB2AN0	IO							AB25		
2A	VREFB2AN0	IO						AA27	AJ34		
2A	VREFB2AN0	IO						Y28	AG32		
2A	VREFB2AN0	IO						W22	AG31		
2A	VREFB2AN0	IO						W23	AB26		
2A	VREFB2AN0	IO						AB27	AB27		
2A	VREFB2AN0	IO						AA28	AE29		
2A	VREFB2AN0	IO						W24	AE30		
2A	VREFB2AN0	IO						W25	AH34		
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	V21	Y25	AK33		
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	V22	Y26	AK34		
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	U15	V20	AD28	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	T15	V21	AD29	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	Y22	AC28	AJ31	DQS12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	W22	AB28	AJ32	DQSn12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	U16	AA25	AF28	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	T17	AA26	AF29	DQ12L	
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	W20	AB25	AM34	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	W21	AB26	AL34	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	U19	AC25	AE27	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	U20	AC26	AE28	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AA21	AD27	AH30	DQS13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AA22	AD28	AH31	DQSn13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	V19	W20	AD26	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	V20	W21	AD27	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AB20	AG28	AL32	DQS14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AB21	AF28	AL33	DQSn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	V16	Y23	AC25	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	W17	AA24	AC26	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AB18	AE27	AK31		
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AB19	AE28	AK32		
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AA19	AA23	AG29		
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	Y19	AB24	AG30		
		nCONFIG		nCONFIG			AB17	W19	AE25		
		nSTATUS		nSTATUS			W18	AD25	AH28		
		CONF_DONE		CONF_DONE			V18	AE26	AH29		
		PORSEL		PORSEL			Y18	AB23	AF26		
		nCE		nCE			Y17	Y20	AE26		
3A	VREFB3AN0	IO						AF26	AE23		
3A	VREFB3AN0	IO						AH27	AP29		
3A	VREFB3AN0	IO						AH25	AM28		
3A	VREFB3AN0	IO						AG25	AL29		
3A	VREFB3AN0	IO						AG27	AM29		
3A	VREFB3AN0	IO						AH26	AN28		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
3A	VREFB3AN0	IO						AE22	AK27		
3A	VREFB3AN0	IO						AD22	AM30		
3A	VREFB3AN0	IO						AB20	AN27		
3A	VREFB3AN0	IO						AB21	AP28		
3A	VREFB3AN0	IO						AD21	AN30		
3A	VREFB3AN0	IO						AC21	AM31		
3A	VREFB3AN0	IO						AD24	AH26		
3A	VREFB3AN0	IO						AE23	AP27		
3A	VREFB3AN0	IO						AF24	AM26		
3A	VREFB3AN0	IO						AE24	AL26		
3A	VREFB3AN0	IO						AF23	AM32		
3A	VREFB3AN0	IO						AG24	AF24		
3A	VREFB3AN0	IO						AH24	AG24		
3A	VREFB3AN0	IO						AH23	AK25		
3A	VREFB3AN0	IO						AH20	AL27		
3A	VREFB3AN0	IO						AH21	AH25		
3A	VREFB3AN0	IO						AH22	AH24		
3A	VREFB3AN0	IO						AG22	AH27		
3A	VREFB3AN0	IO						AC20	AL28		
3A	VREFB3AN0	IO						AG21	AN31		
3A	VREFB3AN0	IO						AF21	AF23		
3A	VREFB3AN0	IO						AE21	AJ28		
3A	VREFB3AN0	IO						AF20	AJ29		
3A	VREFB3AN0	IO						AE20	AP32		
3A	VREFB3AN0	IO						AD19	AP30		
3A	VREFB3AN0	IO						AC19	AP31		
3A	VREFB3AN0	IO						AB19	AN33		
3A	VREFB3AN0	IO						AA19	AP33		
3A	VREFB3AN0	IO						AE19	AK28		
3A	VREFB3AN0	IO						AD18	AJ26		
3A	VREFB3AN0	IO						Y19	AJ27		
3A	VREFB3AN0	IO						AA18	AC22		
3A	VREFB3AN0	IO						Y18	AD22		
3A	VREFB3AN0	IO						Y17	AE24		
3B	VREFB3BN0	IO							AH23		
3B	VREFB3BN0	IO							AJ24		
3B	VREFB3BN0	IO							AJ22		
3B	VREFB3BN0	IO							AH22		
3B	VREFB3BN0	IO							AJ23		
3B	VREFB3BN0	IO							AK22		
3B	VREFB3BN0	IO							AM24		
3B	VREFB3BN0	IO							AL24		
3B	VREFB3BN0	IO							AK24		
3B	VREFB3BN0	IO							AL25		
3B	VREFB3BN0	IO							AM23		
3B	VREFB3BN0	IO							AL23		
3B	VREFB3BN0	IO							AE22		
3B	VREFB3BN0	IO							AE21		
3B	VREFB3BN0	IO							AG21		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
3B	VREFB3BN0	IO							AF21		
3B	VREFB3BN0	IO							AD21		
3B	VREFB3BN0	IO							AE20		
3B	VREFB3BN0	IO							AP25		
3B	VREFB3BN0	IO							AN25		
3B	VREFB3BN0	IO							AP26		
3B	VREFB3BN0	IO							AP23		
3B	VREFB3BN0	IO							AP24		
3B	VREFB3BN0	IO							AN24		
3C	VREFB3CN0	IO				DIFFOUT_B21n	W16	AF19	AL22	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B21p	V15	AG19	AM22	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	Y14	AH19	AL21	DQSn7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	W14	AG18	AK21	DQS7B	DQ7B/CQn7B
3C	VREFB3CN0	IO				DIFFOUT_B23n	Y15	AH17	AJ20	DQ7B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B23p	W15	AH18	AJ21	DQ7B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AB16	AF17	AP22	DQSn8B	DQSn7B/DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AA16	AE18	AN22	DQS8B	DQS7B/CQ7B
3C	VREFB3CN0	IO				DIFFOUT_B25n	Y16	AE16	AM21	DQ8B	DQ7B
3C	VREFB3CN0	IO				DIFFOUT_B25p	AB14	AD16	AP20	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AB15	AF16	AP21	DQ8B	DQ7B
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AA15	AE17	AN21	DQ8B	DQ7B
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	T13	AC17	AE19		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	R13	AB17	AD19		
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	W13	AC16	AH19		
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	V13	AB16	AG19		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	Y12	AA15	AE18		
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	W12	Y15	AD18		
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	U14	AH16	AK19		
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	U13	AG16	AJ19		
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AB12	AH15	AP19		
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AA12	AG15	AN19		
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AB13	AF15	AP18		
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AA13	AE15	AN18		
3C	VREFB3CN0	IO							AL20		
3C	VREFB3CN0	IO							AM18		
3C	VREFB3CN0	IO							AM19		
3C	VREFB3CN0	IO							AL19		
3C	VREFB3CN0	IO							AK18		
3C	VREFB3CN0	IO							AL18		
3C	VREFB3CN0	IO							AF20		
3C	VREFB3CN0	IO							AF19		
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	Y10	AE14	AN16		
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AA10	AF14	AP16		
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AB10	AG13	AN15		
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AB11	AH14	AP15		
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	W11	AG12	AJ16		
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	Y11	AH13	AK16		
4C	VREFB4CN0	IO				DIFFOUT_B36p	T10	Y13	AL15	DQ9B	
4C	VREFB4CN0	IO				DIFFOUT_B36n	R10	Y14	AM15	DQ9B	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	U9	AD13	AL14	DQS9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	V9	AE13	AM14	DQSn9B	
4C	VREFB4CN0	IO				DIFFOUT_B38p	R9	AA13	AK13	DQ9B	
4C	VREFB4CN0	IO				DIFFOUT_B38n	T9	AB13	AL13	DQ9B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AA9	AG10	AH15	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AB9	AH10	AJ15	DQ10B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B40p	W8	AH11	AG15	DQ10B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B40n	AB8	AH12	AK15	DQ10B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	W9	AF10	AH14	DQS10B	DQS11B/CQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	Y9	AF11	AJ14	DQSn10B	DQSn11B/DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42p	Y7	AF12	AP14	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B42n	W7	AC12	AN13	DQ11B	DQ11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AA7	AD12	AN12	DQS11B	DQ11B/CQn11B
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AB7	AE12	AP12	DQSn11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B44p	AB6	AC11	AM12	DQ11B	DQ11B
4C	VREFB4CN0	IO				DIFFOUT_B44n	AA6	AE11	AP13	DQ11B	DQ11B
4C	VREFB4CN0	IO							AL17		
4C	VREFB4CN0	IO							AM17		
4C	VREFB4CN0	IO							AE16		
4C	VREFB4CN0	IO							AF16		
4C	VREFB4CN0	IO							AL16		
4C	VREFB4CN0	IO							AM16		
4C	VREFB4CN0	IO							AD15		
4C	VREFB4CN0	IO							AD16		
4B	VREFB4BN0	IO							AN10		
4B	VREFB4BN0	IO							AP10		
4B	VREFB4BN0	IO							AP9		
4B	VREFB4BN0	IO							AP11		
4B	VREFB4BN0	IO							AM9		
4B	VREFB4BN0	IO							AN9		
4B	VREFB4BN0	IO							AE15		
4B	VREFB4BN0	IO							AF15		
4B	VREFB4BN0	IO							AF13		
4B	VREFB4BN0	IO							AF14		
4B	VREFB4BN0	IO							AE13		
4B	VREFB4BN0	IO							AE14		
4B	VREFB4BN0	IO							AK12		
4B	VREFB4BN0	IO							AL12		
4B	VREFB4BN0	IO							AK10		
4B	VREFB4BN0	IO							AM11		
4B	VREFB4BN0	IO							AL10		
4B	VREFB4BN0	IO							AL11		
4B	VREFB4BN0	IO							AM8		
4B	VREFB4BN0	IO							AP8		
4B	VREFB4BN0	IO							AN7		
4B	VREFB4BN0	IO							AP7		
4B	VREFB4BN0	IO							AP6		
4B	VREFB4BN0	IO							AM7		
4A	VREFB4AN0	IO						AB11	AM4		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
4A	VREFB4AN0	IO						AC10	AL5		
4A	VREFB4AN0	IO						Y10	AC12		
4A	VREFB4AN0	IO						Y11	AE10		
4A	VREFB4AN0	IO						AG9	AE11		
4A	VREFB4AN0	IO						AH8	AM5		
4A	VREFB4AN0	IO						AE10	AD12		
4A	VREFB4AN0	IO						AH9	AG9		
4A	VREFB4AN0	IO						AE9	AF11		
4A	VREFB4AN0	IO						AF9	AN6		
4A	VREFB4AN0	IO						AF8	AF10		
4A	VREFB4AN0	IO						AE8	AH9		
4A	VREFB4AN0	IO						AG7	AM6		
4A	VREFB4AN0	IO						AH7	AG12		
4A	VREFB4AN0	IO						AG6	AJ6		
4A	VREFB4AN0	IO						AH6	AH8		
4A	VREFB4AN0	IO						AG4	AJ7		
4A	VREFB4AN0	IO						AH3	AK6		
4A	VREFB4AN0	IO						AH4	AL8		
4A	VREFB4AN0	IO						AH5	AH11		
4A	VREFB4AN0	IO						AG3	AJ8		
4A	VREFB4AN0	IO						AH2	AK7		
4A	VREFB4AN0	IO						AD9	AJ10		
4A	VREFB4AN0	IO						AC9	AJ11		
4A	VREFB4AN0	IO						AA9	AN3		
4A	VREFB4AN0	IO						AB9	AN4		
4A	VREFB4AN0	IO						Y9	AL7		
4A	VREFB4AN0	IO						AA10	AK9		
4A	VREFB4AN0	IO						AE6	AH12		
4A	VREFB4AN0	IO						AF6	AP3		
4A	VREFB4AN0	IO						AE4	AP4		
4A	VREFB4AN0	IO						AE7	AP2		
4A	VREFB4AN0	IO						AE5	AP5		
4A	VREFB4AN0	IO						AF5	AJ9		
4A	VREFB4AN0	IO						AB8	AL9		
4A	VREFB4AN0	IO						AC8	AJ12		
4A	VREFB4AN0	IO						AC7	AJ13		
4A	VREFB4AN0	IO						AD7	AE12		
4A	VREFB4AN0	IO						AB7	AD13		
4A	VREFB4AN0	IO						AD6	AL4		
		nIO_PULLUP		nIO_PULLUP			AB4	AE3	AF8		
		nCEO		nCEO			U5	AB5	AJ5		
		DCLK		DCLK			Y4	AC5	AL3		
		nCSO		nCSO			Y6	AD4	AE9		
		ASDO		ASDO			Y3	AA6	AH6		
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	W4	AC3	AH4		
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	W5	AC4	AH5		
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AA3	AF1	AK3		
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AA4	AE2	AK4		
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	V6	AB3	AE7	DQ1R	DQ1R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	V7	AB4	AE8	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AB2	AG1	AM1	DQSn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AB3	AF2	AM2	DQS1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	U4	Y6	AF5	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	T4	Y7	AF6	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AB1	AE1	AJ3	DQSn2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AA1	AD1	AJ4	DQS2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	V3	AA4	AC8	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	V4	Y5	AC9	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	W2	AC1	AL1	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	W3	AC2	AL2	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	U7	Y3	AE5	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	U8	Y4	AE6	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	Y1	AB1	AG3	DQSn3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	Y2	AB2	AG4	DQS3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	T7	W8	AB10	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	T8	W9	AC11	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	W1	AA1	AK1		
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	V1	Y2	AJ2		
5A	VREFB5AN0	IO						W5	AB9		
5A	VREFB5AN0	IO						W6	AA10		
5A	VREFB5AN0	IO						Y1	AH1		
5A	VREFB5AN0	IO						W2	AG1		
5A	VREFB5AN0	IO						V6	AC5		
5A	VREFB5AN0	IO						V7	AC6		
5A	VREFB5AN0	IO						W3	AF1		
5A	VREFB5AN0	IO						W4	AF2		
5A	VREFB5AN0	IO							AB11		
5A	VREFB5AN0	IO							AA12		
5A	VREFB5AN0	IO							AE3		
5A	VREFB5AN0	IO							AE4		
5A	VREFB5AN0	IO							AD3		
5A	VREFB5AN0	IO							AD4		
5A	VREFB5AN0	IO							AE1		
5A	VREFB5AN0	IO							AE2		
5A	VREFB5AN0	IO							AC7		
5A	VREFB5AN0	IO							AB8		
5A	VREFB5AN0	IO							AH2		
5A	VREFB5AN0	IO							AF3		
5A	VREFB5AN0	IO							AF4		
5A	VREFB5AN0	IO							AD6		
5A	VREFB5AN0	IO							AD7		
5A	VREFB5AN0	IO							AJ1		
5C	VREFB5CN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	R6	U6	Y11		
5C	VREFB5CN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	P7	U7	W12		
5C	VREFB5CN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	R3	V3	Y3	DQSn5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	R4	V4	AA4	DQS5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	P3	U8	Y5	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	P4	U9	Y6	DQ5R	

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
5C	VREFB5CN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	U3	W1	AB1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	T3	V1	AA1	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	P6	T4	W7	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	N6	U5	W8	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	U1	U3	W3	DQSn6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	U2	U4	Y4	DQS6R	DQ5R/CQn5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	N4	T8	W10	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	N5	T9	W11	DQ6R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	T1	T2	Y1	DQSn7R	DQSn5R/DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	T2	T3	Y2	DQS7R	DQS5R/CQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	M6	T6	W5	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	M7	R6	W6	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	P1	R4	V3	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	P2	T5	V4	DQ7R	DQ5R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	M3	R9	W9		
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	M4	R10	V10		
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R14n	DIFFOUT_R28n	N2	U1	U3		
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R14p	DIFFOUT_R28p	N3	U2	U4		
5C	VREFB5CN0	CLK8n	CLK8n				N1	T1	W1		
5C	VREFB5CN0	CLK8p	CLK8p				M1	R1	W2		
5C	VREFB5CN0	IO							AB5		
5C	VREFB5CN0	IO							AB6		
5C	VREFB5CN0	IO							AB3		
5C	VREFB5CN0	IO							AC4		
5C	VREFB5CN0	IO							AA6		
5C	VREFB5CN0	IO							AA7		
5C	VREFB5CN0	IO							AD1		
5C	VREFB5CN0	IO							AC2		
5C	VREFB5CN0	IO							Y9		
5C	VREFB5CN0	IO							Y10		
5C	VREFB5CN0	IO							AA3		
5C	VREFB5CN0	IO							AB4		
5C	VREFB5CN0	IO							Y7		
5C	VREFB5CN0	IO							Y8		
5C	VREFB5CN0	IO							AC1		
5C	VREFB5CN0	IO							AB2		
6C	VREFB6CN0	CLK10p	CLK10p				L2	P2	U2		
6C	VREFB6CN0	CLK10n	CLK10n				L1	P1	U1		
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R15p	DIFFOUT_R29p	K2	M1	T2		
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R15n	DIFFOUT_R29n	K1	N1	T1		
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R15p	DIFFOUT_R30p	L4	P9	U11		
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R15n	DIFFOUT_R30n	L3	P8	U10		
6C	VREFB6CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R31p	H1	N4	P2	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R31n	J1	P4	R1	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R32p	K8	N7	T7	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R32n	K7	N6	U6	DQ8R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R33p	K4	P3	R4	DQS8R	DQS10R/CQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R33n	K3	N2	R3	DQSn8R	DQSn10R/DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R34p	H7	N5	T9	DQ9R	DQ10R

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
6C	VREFB6CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R34n	J7	M4	T8	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R35p	F1	L2	N2	DQS9R	DQ10R/CQn10R
6C	VREFB6CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R35n	G1	L1	P1	DQSn9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R36p	J4	N9	T5	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R36n	J3	N8	T4	DQ9R	DQ10R
6C	VREFB6CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R37p	H3	L3	P4	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R37n	H2	M3	P3	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R38p	H5	L5	R7	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R38n	H4	L4	R6	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R39p	G4	K2	M1	DQS10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R39n	G3	K1	N1	DQSn10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R40p	H6	L6	P6		
6C	VREFB6CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R40n	J6	M6	P5		
6C	VREFB6CN0	IO							N4		
6C	VREFB6CN0	IO							N3		
6C	VREFB6CN0	IO							R12		
6C	VREFB6CN0	IO							T11		
6C	VREFB6CN0	IO							L2		
6C	VREFB6CN0	IO							L1		
6C	VREFB6CN0	IO							R10		
6C	VREFB6CN0	IO							R9		
6C	VREFB6CN0	IO							M4		
6C	VREFB6CN0	IO							M3		
6C	VREFB6CN0	IO							P8		
6C	VREFB6CN0	IO							P7		
6C	VREFB6CN0	IO							K2		
6C	VREFB6CN0	IO							K1		
6C	VREFB6CN0	IO							N6		
6C	VREFB6CN0	IO							N5		
6A	VREFB6AN0	IO							H2		
6A	VREFB6AN0	IO							J1		
6A	VREFB6AN0	IO							P11		
6A	VREFB6AN0	IO							P10		
6A	VREFB6AN0	IO							K4		
6A	VREFB6AN0	IO							K3		
6A	VREFB6AN0	IO							M7		
6A	VREFB6AN0	IO							M6		
6A	VREFB6AN0	IO							G2		
6A	VREFB6AN0	IO							H1		
6A	VREFB6AN0	IO							L5		
6A	VREFB6AN0	IO							L4		
6A	VREFB6AN0	IO							J4		
6A	VREFB6AN0	IO							J3		
6A	VREFB6AN0	IO							L7		
6A	VREFB6AN0	IO							L6		
6A	VREFB6AN0	IO						H2	H4		
6A	VREFB6AN0	IO						J1	H3		
6A	VREFB6AN0	IO						K7	F1		
6A	VREFB6AN0	IO						K6	G1		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
6A	VREFB6AN0	IO						G2	K5		
6A	VREFB6AN0	IO						H1	K6		
6A	VREFB6AN0	IO						K5	N8		
6A	VREFB6AN0	IO						K4	N9		
6A	VREFB6AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R45p	E2	F1	E2		
6A	VREFB6AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R45n	E1	G1	E1		
6A	VREFB6AN0	IO			DIFFIO_TX_R23p	DIFFOUT_R46p	F8	J4	N11	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R23n	DIFFOUT_R46n	G8	J3	N10	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	D2	E2	F4	DQS12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	D1	E1	F3	DQSn12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	F7	L9	J7	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	G6	L8	J6	DQ12R	
6A	VREFB6AN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	B1	H4	G5	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	C1	H3	G4	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	F4	K9	K8	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	F3	K8	K7	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	A2	D2	C1	DQS13R	DQS14R/CQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	B2	D1	D1	DQSn13R	DQSn14R/DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	E5	J6	M10	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	E4	H5	M9	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	D3	F4	D3	DQS14R	DQ14R/CQn14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	E3	F3	D2	DQSn14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	B4	G4	L9	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	C4	G3	L8	DQ14R	DQ14R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R28p	DIFFOUT_R55p	A4	B1	E4		
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R28n	DIFFOUT_R55n	A3	C1	E3		
6A	VREFB6AN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	B5	H6	H6		
6A	VREFB6AN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	C5	G5	H5		
7A	VREFB7AN0	IO						A2	F8		
7A	VREFB7AN0	IO						C3	F9		
7A	VREFB7AN0	IO						A4	E7		
7A	VREFB7AN0	IO						B4	A2		
7A	VREFB7AN0	IO						A3	B2		
7A	VREFB7AN0	IO						B2	A4		
7A	VREFB7AN0	IO						D7	A5		
7A	VREFB7AN0	IO						E7	A3		
7A	VREFB7AN0	IO						G8	G8		
7A	VREFB7AN0	IO						G9	F7		
7A	VREFB7AN0	IO						E8	J12		
7A	VREFB7AN0	IO						F8	B4		
7A	VREFB7AN0	IO						D6	D7		
7A	VREFB7AN0	IO						E5	F6		
7A	VREFB7AN0	IO						C5	G11		
7A	VREFB7AN0	IO						D5	G10		
7A	VREFB7AN0	IO						B5	C9		
7A	VREFB7AN0	IO						C6	D8		
7A	VREFB7AN0	IO						A5	A8		
7A	VREFB7AN0	IO						A6	H11		
7A	VREFB7AN0	IO						A8	J11		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
7A	VREFB7AN0	IO						A9	C3		
7A	VREFB7AN0	IO						A7	D9		
7A	VREFB7AN0	IO						B7	E10		
7A	VREFB7AN0	IO						B8	A7		
7A	VREFB7AN0	IO						F9	B8		
7A	VREFB7AN0	IO						C8	G9		
7A	VREFB7AN0	IO						D8	C4		
7A	VREFB7AN0	IO						D9	B5		
7A	VREFB7AN0	IO						C9	B7		
7A	VREFB7AN0	IO						E10	C5		
7A	VREFB7AN0	IO						F10	E8		
7A	VREFB7AN0	IO						H10	C7		
7A	VREFB7AN0	IO						G10	C6		
7A	VREFB7AN0	IO						D10	D6		
7A	VREFB7AN0	IO						E11	A6		
7A	VREFB7AN0	IO						H11	M13		
7A	VREFB7AN0	IO						J10	L13		
7A	VREFB7AN0	IO						J11	K11		
7A	VREFB7AN0	IO						J12	K12		
7B	VREFB7BN0	IO							G12		
7B	VREFB7BN0	IO							F11		
7B	VREFB7BN0	IO							F12		
7B	VREFB7BN0	IO							F13		
7B	VREFB7BN0	IO							G13		
7B	VREFB7BN0	IO							E11		
7B	VREFB7BN0	IO							C11		
7B	VREFB7BN0	IO							D11		
7B	VREFB7BN0	IO							D13		
7B	VREFB7BN0	IO							D10		
7B	VREFB7BN0	IO							C12		
7B	VREFB7BN0	IO							D12		
7B	VREFB7BN0	IO							K14		
7B	VREFB7BN0	IO							K13		
7B	VREFB7BN0	IO							H14		
7B	VREFB7BN0	IO							J14		
7B	VREFB7BN0	IO							K15		
7B	VREFB7BN0	IO							L14		
7B	VREFB7BN0	IO							A10		
7B	VREFB7BN0	IO							B10		
7B	VREFB7BN0	IO							A12		
7B	VREFB7BN0	IO							A9		
7B	VREFB7BN0	IO							A11		
7B	VREFB7BN0	IO							B11		
7C	VREFB7CN0	IO				DIFFOUT_T21n	D7	B10	D14	DQ7T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T21p	D9	C10	E13	DQ7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	C10	A10	E14	DQSn7T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	D10	B11	F14	DQS7T	DQ7T/CQn7T
7C	VREFB7CN0	IO				DIFFOUT_T23n	D8	A11	F15	DQ7T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T23p	C9	A12	D15	DQ7T	DQ7T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	A7	C12	A13	DQSn8T	DQSn7T/DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	B7	D11	B13	DQS8T	DQS7T/CQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25n	A9	E13	A15	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T25p	C7	D13	C14	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	A8	C13	A14	DQ8T	DQ7T
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	B8	D12	B14	DQ8T	DQ7T
7C	VREFB7CN0	IO				DIFFOUT_T27n	F10	G12	C17	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T27p	G10	F12	C15	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	F9	F13	C16	DQSn9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	G9	G13	D16	DQS9T	
7C	VREFB7CN0	IO				DIFFOUT_T29n	H10	H14	D17	DQ9T	
7C	VREFB7CN0	IO				DIFFOUT_T29p	G11	J14	E17	DQ9T	
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C11	A13	J16		
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D11	B13	J15		
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A11	A14	A16		
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B11	B14	B16		
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	A10	C14	A17		
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	B10	D14	B17		
7C	VREFB7CN0	IO							L16		
7C	VREFB7CN0	IO							K16		
7C	VREFB7CN0	IO							G16		
7C	VREFB7CN0	IO							H16		
7C	VREFB7CN0	IO							K17		
7C	VREFB7CN0	IO							L17		
7C	VREFB7CN0	IO							E16		
7C	VREFB7CN0	IO							F16		
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	A13	D15	B19		
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	A12	C15	A19		
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	D12	B16	B20		
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	C12	A15	A20		
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	C13	B17	D18		
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	B13	A16	C18		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	H14	J16	K19		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	G14	J15	J19		
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	D14	E16	D19		
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D13	D16	C19		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	E14	G16	L19		
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	F14	H16	L20		
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	A15	B19	G20	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A14	A19	F20	DQ10T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T40p	B14	A17	E20	DQ10T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T40n	D15	A18	H20	DQ10T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C15	C19	G21	DQS10T	DQS11T/CQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C14	C18	F21	DQSn10T	DQSn11T/DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42p	C17	F17	A22	DQ11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T42n	B17	C17	A21	DQ11T	DQ11T
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	A17	E17	B23	DQS11T	DQ11T/CQn11T
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	A16	D17	A23	DQSn11T	DQ11T
8C	VREFB8CN0	IO				DIFFOUT_T44p	D16	D18	B22	DQ11T	DQ11T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
8C	VREFB8CN0	IO				DIFFOUT_T44n	C16	F18	C23	DQ11T	DQ11T
8C	VREFB8CN0	IO							F19		
8C	VREFB8CN0	IO							E19		
8C	VREFB8CN0	IO							C20		
8C	VREFB8CN0	IO							D20		
8C	VREFB8CN0	IO							D21		
8C	VREFB8CN0	IO							C21		
8C	VREFB8CN0	IO							D22		
8C	VREFB8CN0	IO							E22		
8B	VREFB8BN0	IO							B25		
8B	VREFB8BN0	IO							A25		
8B	VREFB8BN0	IO							A24		
8B	VREFB8BN0	IO							A26		
8B	VREFB8BN0	IO							C26		
8B	VREFB8BN0	IO							B26		
8B	VREFB8BN0	IO							K20		
8B	VREFB8BN0	IO							J20		
8B	VREFB8BN0	IO							J22		
8B	VREFB8BN0	IO							J21		
8B	VREFB8BN0	IO							K21		
8B	VREFB8BN0	IO							K22		
8B	VREFB8BN0	IO							D25		
8B	VREFB8BN0	IO							D24		
8B	VREFB8BN0	IO							C24		
8B	VREFB8BN0	IO							E25		
8B	VREFB8BN0	IO							E23		
8B	VREFB8BN0	IO							D23		
8B	VREFB8BN0	IO							A27		
8B	VREFB8BN0	IO							C27		
8B	VREFB8BN0	IO							B28		
8B	VREFB8BN0	IO							A28		
8B	VREFB8BN0	IO							C28		
8B	VREFB8BN0	IO							A29		
8A	VREFB8AN0	IO						G18	F22		
8A	VREFB8AN0	IO						F19	F23		
8A	VREFB8AN0	IO						J18	D26		
8A	VREFB8AN0	IO						J19	F26		
8A	VREFB8AN0	IO						B20	A30		
8A	VREFB8AN0	IO						A21	A33		
8A	VREFB8AN0	IO						A20	A31		
8A	VREFB8AN0	IO						D19	A32		
8A	VREFB8AN0	IO						D20	G23		
8A	VREFB8AN0	IO						C20	E26		
8A	VREFB8AN0	IO						D21	D28		
8A	VREFB8AN0	IO						C21	B31		
8A	VREFB8AN0	IO						B22	B32		
8A	VREFB8AN0	IO						A22	F24		
8A	VREFB8AN0	IO						A23	D27		
8A	VREFB8AN0	IO						B23	E28		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
8A	VREFB8AN0	IO						B25	E29		
8A	VREFB8AN0	IO						A26	H23		
8A	VREFB8AN0	IO						A24	G24		
8A	VREFB8AN0	IO						A25	F25		
8A	VREFB8AN0	IO						B26	F27		
8A	VREFB8AN0	IO						A27	F28		
8A	VREFB8AN0	IO						F20	F29		
8A	VREFB8AN0	IO						E20	G27		
8A	VREFB8AN0	IO						H20	B29		
8A	VREFB8AN0	IO						G20	G26		
8A	VREFB8AN0	IO						H19	J25		
8A	VREFB8AN0	IO						J20	L23		
8A	VREFB8AN0	IO						D23	C29		
8A	VREFB8AN0	IO						C23	J24		
8A	VREFB8AN0	IO						D22	H26		
8A	VREFB8AN0	IO						D25	M23		
8A	VREFB8AN0	IO						D24	C30		
8A	VREFB8AN0	IO						C24	K24		
8A	VREFB8AN0	IO						F21	K25		
8A	VREFB8AN0	IO						G21	C31		
8A	VREFB8AN0	IO						F22	D30		
8A	VREFB8AN0	IO						E22	L22		
8A	VREFB8AN0	IO						E23	K23		
8A	VREFB8AN0	IO						G22	D31		
		GND					L14	M17	V2		
		GND					AB5	AF3	AF9		
		GND					M11	R14	V17		
		GND					E18	K11	E21		
		GND					AB22	B24	N14		
		GND					AA20	AG2	AN5		
		GND					AA17	AG5	AN8		
		GND					AA14	AG8	AN11		
		GND					AA11	AG11	AN14		
		GND					AA8	AG14	AN17		
		GND					AA5	AG17	AN20		
		GND					AA2	AG20	AN23		
		GND					Y21	AG23	AN26		
		GND					V17	AG26	AN29		
		GND					V14	AF27	AN32		
		GND					V11	AD2	AM33		
		GND					V8	AD5	AK2		
		GND					V5	AD8	AK5		
		GND					V2	AD11	AK8		
		GND					U21	AD14	AK11		
		GND					U18	AD17	AK14		
		GND					R14	AD20	AK17		
		GND					R11	AD23	AK20		
		GND					R8	AC24	AK23		
		GND					R5	AC27	AK26		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		GND					R2	AA2	AK29		
		GND					P21	AA5	AJ30		
		GND					P18	AA8	AJ33		
		GND					P15	AA11	AG2		
		GND					P13	AA14	AG5		
		GND					P11	AA17	AG8		
		GND					P9	AA20	AG11		
		GND					N14	Y12	AG14		
		GND					N12	Y16	AG17		
		GND					N10	Y21	AG20		
		GND					M13	Y24	AG23		
		GND					M9	Y27	AG26		
		GND					M8	W12	AF27		
		GND					M5	W14	AF30		
		GND					M2	W16	AF33		
		GND					L21	W18	AD2		
		GND					L18	V2	AD5		
		GND					L15	V5	AD8		
		GND					L10	V8	AD11		
		GND					K13	V11	AD14		
		GND					K11	V13	AD17		
		GND					K9	V15	AD20		
		GND					J14	V17	AD23		
		GND					J12	V19	AC14		
		GND					J10	U10	AC16		
		GND					J8	U12	AC18		
		GND					J5	U14	AC20		
		GND					J2	U16	AC24		
		GND					H21	U18	AC27		
		GND					H18	U21	AC30		
		GND					H15	U24	AC33		
		GND					H12	U27	AB13		
		GND					H9	T11	AB15		
		GND					F5	T13	AB17		
		GND					F2	T15	AB19		
		GND					E21	T17	AB21		
		GND					E15	T19	AB23		
		GND					E12	R2	AA2		
		GND					E9	R5	AA5		
		GND					E6	R8	AA8		
		GND					C2	R12	AA11		
		GND					B21	R16	AA14		
		GND					B18	R18	AA16		
		GND					B15	P11	AA18		
		GND					B12	P13	AA20		
		GND					B9	P17	AA22		
		GND					B6	P21	Y13		
		GND					B3	P24	Y15		
		GND					A1	P27	Y17		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		GND						E15	N16		
		GND						N10	N18		
		GND						N12	N20		
		GND						N14	N22		
		GND						N16	M2		
		GND						N18	M5		
		GND						M2	M8		
		GND						M5	M11		
		GND						M8	M15		
		GND						M11	M17		
		GND						M13	M19		
		GND						M15	M21		
		GND						M19	L12		
		GND						L10	L15		
		GND						L12	L18		
		GND						L14	L21		
		GND						L16	L24		
		GND						L18	L27		
		GND						L21	L30		
		GND						L24	L33		
		GND						L27	J2		
		GND						K13	J5		
		GND						K15	J8		
		GND						K17	H9		
		GND						K19	H12		
		GND						J2	H15		
		GND						J5	H18		
		GND						J8	H21		
		GND						J13	H24		
		GND						J17	H27		
		GND						H9	H30		
		GND						H12	H33		
		GND						H15	F2		
		GND						H18	F5		
		GND						H21	E6		
		GND						H24	E9		
		GND						H27	E12		
		GND						F2	E15		
		GND						F5	E18		
		GND						E6	E24		
		GND						E9	E27		
		GND						E12	E30		
		GND						E18	E33		
		GND						E21	C2		
		GND						E24	B3		
		GND						E27	B6		
		GND						C2	B9		
		GND						B3	B12		
		GND						B6	B15		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		GND						B9	B18		
		GND						B12	B21		
		GND						B15	B24		
		GND						B18	B27		
		GND						B21	B30		
		GND						B27	B33		
		GND							P27		
		GND							P30		
		GND							P33		
		GND							N12		
		GND							AN2		
		GND							P19		
		GND							P21		
		GND							P24		
		GND							P17		
		GND							R16		
		GND							R18		
		GND							R20		
		GND							R22		
		GND							P13		
		GND							P15		
		GND							R11		
		GND							R14		
		GND							R5		
		GND							R8		
		GND							T13		
		GND							T15		
		GND							T17		
		GND							T19		
		GND							T21		
		GND							R2		
		GND							U33		
		GND							U27		
		GND							U30		
		GND							U22		
		GND							U23		
		GND							U24		
		GND							U12		
		GND							U14		
		GND							U16		
		GND							U20		
		GND							V8		
		GND							V11		
		GND							V12		
		GND							V13		
		GND							V15		
		GND							V19		
		GND							V21		
		GND							V23		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		GND							W18		
		GND							W20		
		GND							W22		
		GND							V5		
		GND							Y33		
		GND							W14		
		GND							W16		
		GND							Y19		
		GND							Y21		
		GND							Y24		
		GND							Y27		
		GND							Y30		
		VCCL					L11	R15	U17		
		VCCL					K14	L17	T14		
		VCCL					P12	V14	AB22		
		VCCL					N13	V18	AA13		
		VCCL					N11	U11	AA15		
		VCCL					N9	U13	AA17		
		VCCL					M12	U15	AA19		
		VCCL					M10	U17	AA21		
		VCCL					L13	T12	Y14		
		VCCL					K12	T14	Y16		
		VCCL					K10	T16	Y18		
		VCCL					J13	R13	Y20		
		VCCL					J11	R17	W15		
		VCCL						M16	T16		
		VCCL						P12	T18		
		VCCL						P14	T20		
		VCCL						P16	R15		
		VCCL						P18	R17		
		VCCL						N13	R19		
		VCCL						N15	R21		
		VCCL						N17	P14		
		VCCL						M12	P16		
		VCCL						M14	P18		
		VCCL						L11	P20		
		VCCL							P22		
		VCCL							N13		
		VCCL							N21		
		VCCL							U21		
		VCCL							V20		
		VCCL							U15		
		VCCL							U19		
		VCCL							V16		
		VCCL							V18		
		VCCL							AB14		
		VCCL							W17		
		VCCL							W19		
		VCCL							W21		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		VCCL							V14		
		VCC					J9	T18	AB20		
		VCC					P14	V12	AB16		
		VCC					M14	V16	AB18		
		VCC					L9	R11	Y22		
		VCC						M18	T22		
		VCC						N11	R13		
		VCC						L13	N15		
		VCC						L15	N17		
		VCC							V22		
		VCC							U13		
		VCC							N19		
		VCC							W13		
		VCCPT					F17	G23	J27		
		VCCPT					U17	AC23	AG27		
		VCCPT					U6	AB6	AG7		
		VCCPT					F6	G6	H8		
		DNU					L12	P15	U18		
		VCCPGM					T16	AA21	AD24		
		VCCPGM					T6	Y8	AD10		
		TEMPDIODEn					A6	D4	D4		
		TEMPDIODEp					A5	D3	E5		
		VCC_CLKIN3C					T12	AB14	AG18		
		VCC_CLKIN4C					U10	AC13	AE17		
		VCC_CLKIN7C					E11	F14	H17		
		VCC_CLKIN8C					F13	F16	K18		
		VCCA_PLL_B1					U11	AC14	AH18		
		VCCA_PLL_L2					M18	R22	U28		
		VCCA_PLL_R2					L5	R7	U7		
		VCCA_PLL_T1					F12	F15	G18		
		VCCA_PLL_L3							V28		
		VCCA_PLL_B2							AH17		
		VCCA_PLL_R3							V7		
		VCCA_PLL_T2							G17		
		VCCD_PLL_B1					U12	AB15	AF18		
		VCCD_PLL_L2					M17	P22	U26		
		VCCD_PLL_R2					L6	P7	U9		
		VCCD_PLL_T1					G12	G15	J18		
		VCCD_PLL_L3							V26		
		VCCD_PLL_B2							AF17		
		VCCD_PLL_R3							V9		
		VCCD_PLL_T2							J17		
		VCCIO1A					C18	E26	H29		
		VCCIO1A					F19	H23	L26		
		VCCIO1A						H26	G32		
		VCCIO1A							B34		
		VCCIO1A							N28		
		VCCIO1C					H22	P26	M32		
		VCCIO1C					K17	R23	V30		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		VCCIO1C							U34		
		VCCIO1C							T31		
		VCCIO2A					R16	W26	AH32		
		VCCIO2A					Y20	AD26	AB28		
		VCCIO2A						AA22	AG28		
		VCCIO2A							AD25		
		VCCIO2A							AN34		
		VCCIO2C					P22	T26	W25		
		VCCIO2C					R17	V22	AD32		
		VCCIO2C							W29		
		VCCIO2C							W32		
		VCCIO3A						AC22	AF25		
		VCCIO3A						AF22	AM27		
		VCCIO3A						AF25	AL30		
		VCCIO3A						AC18	AJ25		
		VCCIO3B							AF22		
		VCCIO3B							AM25		
		VCCIO3C					T14	AF18	AM20		
		VCCIO3C					Y13	AC15	AH21		
		VCCIO3C							AJ18		
		VCCIO4A						AC6	AH10		
		VCCIO4A						AF4	AF12		
		VCCIO4A						AF7	AM3		
		VCCIO4A						AD10	AL6		
		VCCIO4B							AH13		
		VCCIO4B							AM10		
		VCCIO4C					W10	AB12	AG16		
		VCCIO4C					Y8	AF13	AP17		
		VCCIO4C							AM13		
		VCCIO5A					R7	AA7	AH3		
		VCCIO5A					Y5	AD3	AD9		
		VCCIO5A						AA3	AG6		
		VCCIO5A							AB7		
		VCCIO5A							AN1		
		VCCIO5C					N7	P6	AC3		
		VCCIO5C					R1	R3	W4		
		VCCIO5C							V1		
		VCCIO5C							U5		
		VCCIO6A					D5	E3	H7		
		VCCIO6A					C3	K3	L10		
		VCCIO6A						H7	G3		
		VCCIO6A							B1		
		VCCIO6A							N7		
		VCCIO6C					G2	L7	T10		
		VCCIO6C					K6	N3	T3		
		VCCIO6C							T6		
		VCCIO6C							L3		
		VCCIO7A						C7	D5		
		VCCIO7A						F7	C8		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
		VCCIO7A						F11	F10		
		VCCIO7A						C4	J10		
		VCCIO7B							C10		
		VCCIO7B							J13		
		VCCIO7C					E8	C11	C13		
		VCCIO7C					C8	G14	G14		
		VCCIO7C							F17		
		VCCIO8A						C25	C32		
		VCCIO8A						F23	D29		
		VCCIO8A						E19	G25		
		VCCIO8A						C22	J23		
		VCCIO8B							C25		
		VCCIO8B							G22		
		VCCIO8C					B16	C16	C22		
		VCCIO8C					G13	G17	H19		
		VCCIO8C							A18		
		VCCPD1A					J15	L19	N23		
		VCCPD1C					K15	N19	R23		
		VCCPD2A					R15	U19	AA23		
		VCCPD2C					N15	R19	W23		
		VCCPD3A						W17	AC23		
		VCCPD3B							AC21		
		VCCPD3C					R12	W15	AC19		
		VCCPD4A						W11	AC13		
		VCCPD4B							AC15		
		VCCPD4C					P10	W13	AC17		
		VCCPD5A					P8	V10	AB12		
		VCCPD5C					N8	T10	Y12		
		VCCPD6A					H8	M10	P12		
		VCCPD6C					L8	P10	T12		
		VCCPD7A						K12	M12		
		VCCPD7B							M14		
		VCCPD7C					H11	K14	M16		
		VCCPD8A						K18	M22		
		VCCPD8B							M20		
		VCCPD8C					H13	K16	M18		
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				G18	K22	J26		
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				K18	N22	P26		
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				T18	Y22	AA26		
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				N18	U22	V27		
3A	VREFB3AN0	VREFB3AN0						AB18	AG25		
3B	VREFB3BN0	VREFB3BN0							AG22		
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				V12	AA16	AH20		
4A	VREFB4AN0	VREFB4AN0						AB10	AG10		
4B	VREFB4BN0	VREFB4BN0							AG13		
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				V10	AA12	AH16		
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				T5	W7	AF7		
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				P5	T7	AA9		
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				G5	J7	P9		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	FF484	F780/H780 for Stratix III only	H1152 for Stratix III only	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				K5	M7	U8		
7A	VREFB7AN0	VREFB7AN0						G11	H10		
7B	VREFB7BN0	VREFB7BN0							H13		
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				E10	H13	G15		
8A	VREFB8AN0	VREFB8AN0						G19	H25		
8B	VREFB8BN0	VREFB8BN0							H22		
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				E13	H17	G19		
		NC						AE25			
		NC						U20	AK30		
		NC						M9	K26		
		NC						L20	L25		
		NC						K10	L11		
		NC						J21	M25		
		NC					E16	E25	D32		
		NC					AA18	AB22	AL31		
		NC					W6	W10	AH7		
		NC					D6	E4	G7		
		NC					W19	V9	AC10		
		NC *(3)*		MSEL2			G7	G7	K9		
		NC *(3)*		MSEL1			C6	J9	J9		
		NC *(3)*		MSEL0			E7	H8	K10		
		NC *(4)*					D4	F6	G6		
		NC *(5)*					L17	R24	U29		
		NC *(5)*					T11	AD15	AJ17		
		NC *(5)*					L7	P5	V6		
		NC *(5)*					F11	E14	F18		

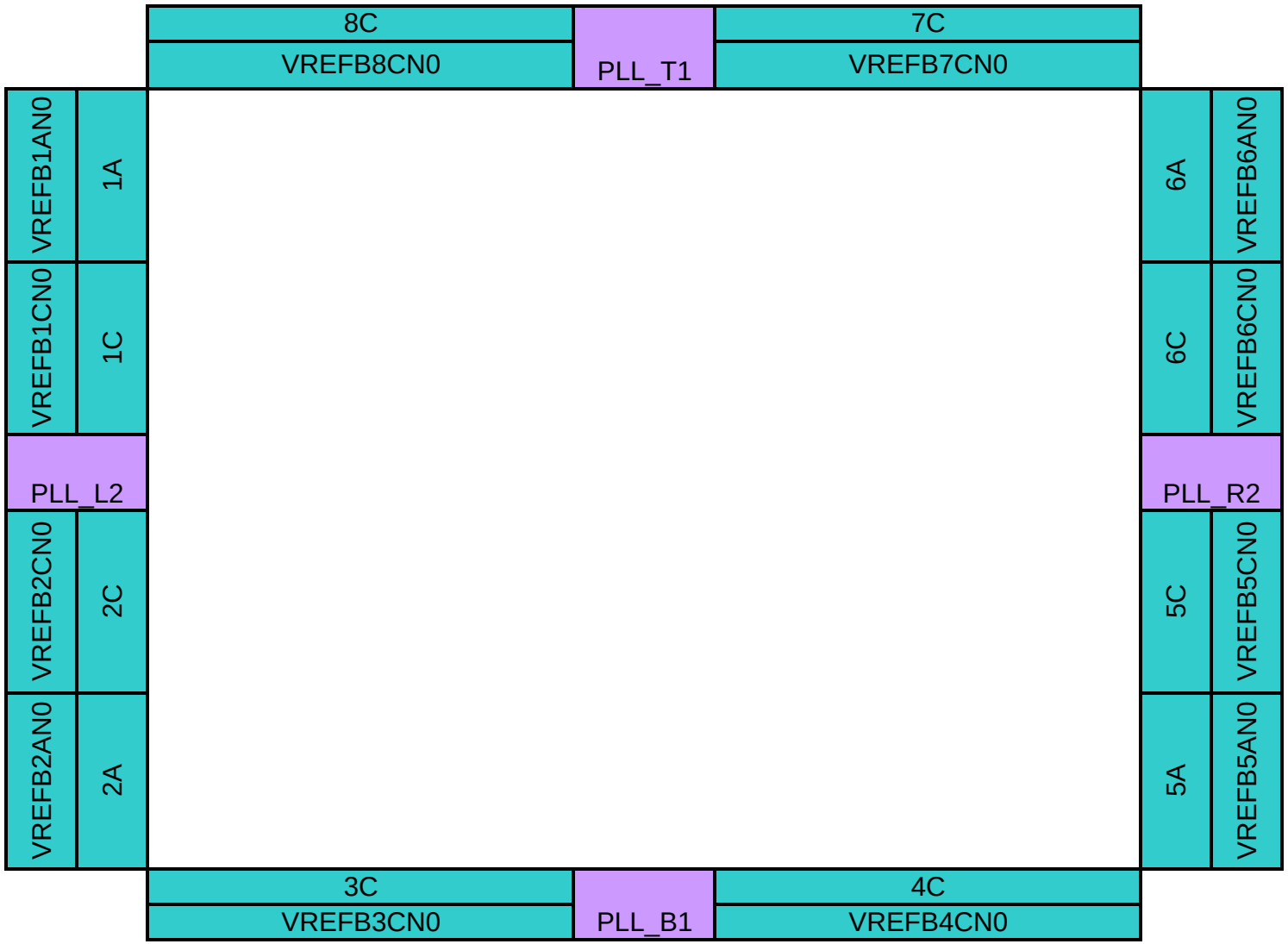
Notes:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix® III device pin table for details.
(2) The individual index number of the pin in this column may not be the same as its companion Stratix III device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix III device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix III device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix III device and should be connected for the FPGA prototype.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VCCL	Power	VCCL supplies power to the core voltage power supply pins.
VCC	Power	VCC supplies power to the periphery circuitry.
RUP[1..8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1..8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
VCCIO[1..8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0-V PCI/PCI-X I/O, and 3.0 V LVTTL I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), 3.0-V PCI/PCI-X and 3.0 V LVTTL I/O standards.
VREF[1..8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, these pins are used as the voltage-referenced pins for the bank.
VCCA_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Analog power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must power up these pins even if the PLL is not used. You are advised to keep this pin isolated from other VCC for better jitter performance.
VCCD_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Digital power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must power up these pins even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCPGM	Power	Power supply for configuration pins. Can be connected to 1.8 V, 2.5 V or 3.0 V depending on the particular design.
VCCPD[1..8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.0 V or 2.5 V. VCCPD for 3.0-V I/O standard is 3.0 V, and VCCPD for 2.5-V/1.8-V/1.2-V I/O standards is 2.5 V.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high (0.9V) turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the HardCopy III device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the HardCopy III device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy III to enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy III drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V,3.0 V) selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin. Connect TCK to GND if the JTAG circuitry is not used.
TMS	Input	Dedicated JTAG input pin. Connect TMS to VCCPD if the JTAG circuitry is not used.
TDI	Input	Dedicated JTAG input pin. Connect TDI to VCCPD if the JTAG circuitry is not used.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,4,5,6,7,9,11..15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[0,2,4,5,6,7,9,11..15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for dfferential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L2,L3,R2,R3]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single-ended I/O or one differential I/O pair. When using both pins as single-ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L2,L3,R2,R3]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual-purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock ouput pins.
PLL_[T1,T2,B1,B2]_CLKOUT0[p,n]	I/O, Clock	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.
	Optional/Dual-Purpose Configuration Pins	
nCSO	Output	Dedicated control signal from Stratix III devices, but kept in HardCopy III for compatibility reasons.
ASDO	Output	Dedicated control signal from Stratix III devices, but kept in HardCopy III for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix III devices, but kept in HardCopy III for compatibility reasons. It's not required to clock this pin for HardCopy III.
	Differential I/O Pins	
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers.Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
	External Memory Interface Pins	
DQS[1..44][T,B], DQS[1..40][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1..44][T,B], DQSn[1..40][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry.
DQ[1..44][T,B],DQ[1..40][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1..44][T,B], CQ[1..40][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1..44][T,B], CQn[1..40][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.

Notes:
(1) These pin definitions are prepared based on the device with the largest density, HC335. Refer to the pin list for the availability of pins in each density.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	10/28/2009	Initial release.