Pin Name (1)	**208-Pin PQFP**	**240-Pin PQFP** (2), (3)	**256-Pin FineLine BGA**	**356-Pin FineLine BGA**	**484-Pin FineLine BGA**
MSEL0 (4)	108	124	P1	D4	U4
MSEL1 (4)	107	123	R1	D3	V4
nSTATUS (4)	52	60	T16	D24	W19
nCONFIG (4)	105	121	N4	D2	T7
DCLK (4)	155	179	B2	AC5	E5
CONF_DONE (4)	2	2	C15	AC24	F18
INIT_DONE (5)	19	26	G16	T24	K19
nCE (4)	154	178	B1	AC2	E4
nCEO (4)	3	3	B16	AC22	E19
nWS (6)	206	238	B14	AE24	E17
nRS (6)	204	236	C14	AE23	F17
nCS (6)	208	240	A16	AD24	D19
CS (6)	207	239	A15	AD23	D18
RDYnBUSY (6)	16	23	G14	U22	K17
CLKUSR (6)	10	11	D15	AA24	G18
DATA7 (6)	166	190	B5	AF4	E8
DATA6 (6)	164	188	D4	AD8	G7
DATA5 (6)	162	186	A4	AE5	D7
DATA4 (6)	161	185	B4	AD6	E7
DATA3 (6)	159	183	C3	AF2	F6
DATA2 (6)	158	182	A2	AD5	D5
DATA1 (6)	157	181	B3	AD4	E6
DATA0 (4), (7)	156	180	A1	AD3	D4
TDI (4)	153	177	C2	AC3	F5
TDO (4)	4	4	C16	AC23	F19
TCK (4)	1	1	B15	AD25	E18
TMS (4)	50	58	P15	D22	U18
TRST (4)	51	59	R16	D23	V19
Dedicated Inputs	78, 80, 182, 184	90, 92, 210, 212	B9, E8, M9, R8	A13, B14, AF14, AE13	E12, H11, R12, V11
Dedicated Clock Pins	79, 183	91, 211	A9, L8	A14, AF13	D12, P11
GCLK1 (9)	79	91	L8	A14	P11
Lock (10)	62	73	P12	C18	U15
DEV_CLRn (5)	180	209	D8	AD13	G11
DEV_OE (5)	186	213	C9	AE14	F12
VCCINT (2.5 V)	6, 23, 35, 43, 76, 106, 109, 117, 137, 145, 181	5, 27, 47, 96, 122, 130, 150, 170	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L12, M11, R2	A1, A26, C26, D5, F1, H22, J1, M26, N1, T26, U5, AA1, AD26, AF1, AF26	C11, C15, H14, J8, J10, J12, J15, L9, L10, L13, M10, M13, M14, N12, P8, P10, P15, R14, V5, W21, Y8, AA12
VCCIO (2.5 or 3.3 V)	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	16, 37, 57, 77, 112, 140, 160, 189, 205, 224	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12	A7, A23, B4, C15, D25, F4, H24, K5, M23, P2, T25, V2, W22, AB1, AC25, AD18, AF3, AF7, AF16	A6, A13, B5, E1, G1, G15, H9, H20, J11, J13, K9, K11, K14, K20, L14, M9, N3, N9, N11, N14, N20, P13, R1, R9, T3, T15, T22, V22, AB13
VCC_CKLK (11)	77	89	L9 (10)	C14	P12

Pin Name (1)	**208-Pin PQFP**	**240-Pin PQFP** (2), (3)	**256-Pin FineLine BGA**	**356-Pin FineLine BGA**	**484-Pin FineLine BGA**
GNDINT (13)	20, 21, 32, 33, 48, 49, 59, 72, 82, 91, 123, 124, 129, 130, 151, 152, 171, 185, 188, 201	10, 22, 32, 42, 52, 69, 85, 104, 125, 135, 145, 155, 165, 176, 197, 216, 232	E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K7, K10, L6, L11, M5, M12	A2, A10, A20, B1, B22, B25, B26, C2, C9, C13, C25, H23, J26, K1, M1, N26, R1, R26, T1, U26, W1, AD2, AD14, AD20, AE1, AE2, AE7, AE25, AE26, AF11, AF19, AF25	A1, A8, A22, B1, B2, B17, B21, B22, C2, C21, E21, G3, G21, H2, H8, H15, J9, J14, J20, K3, K10, K12, K13, L11, L12, M11, M12, M20, N10, N13, P9, P14, R8, R15, R22, T1, V3, W20, Y1, Y2, Y3, Y21, Y22, AA1, AA6, AA22, AB11, AB16
GND_CKLK (11)	81	93	T8	B13	W11
No Connect (N.C.)	-	-	-	-	A2, A3, A4, A5, B3, B4, B10, C17, F2, J2, K2, L2, N1, P20, P22, R3, T20, T21, U1, W22, Y16, AA15, AB3, AB4, AB5, AB7, AB15, AB17, AB18, AB19, AB20
Total User I/O Pins (12)	147	189	191	274	338

Notes:

(1) All pins that are not listed are user I/O pins.
(2) EPF10K50E, EPF10K100E, and EPF10K100B devices are pin-compatible with EPF10K130E devices in the same package if pins 20, 76, and 159 are connected to VCCINT. The MAX+PLUS II software performs this function automatically when future migration is set.
(3) EPF10K50E, EPF10K100E, and EPF10K100B devices are pin-compatible with EPF10K200E devices in the same package if pins 20, 40, 76, 139, 159, 187, and 225 are connected to VCCINT. The MAX+PLUS II software performs this function automatically when future migration is set.
(4) This pin is a dedicated pin; it is not available as a user I/O pin.
(5) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(6) This pin can be used as a user I/O pin after configuration.
(7) This pin is tri-stated in user mode.
(8) The optional JTAG pin TRST is not used in the 144-pin TQFP package.
(9) This pin drives the ClockLock and ClockBoost circuitry.
(10) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(11) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the Clock Lock and Clock Boost circuitry should be isolated from the power and ground to the rest of the device. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(12) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.
(13) The Quartus II software lists some GNDINT pins as GND. The MAX+PLUS II software lists all of these pins (GNDIO, GNDINT, and GND pins) as GND pins. All of these pins can be connected to a single GND plane.