Pin Information for the Cyclone™ EP1C6 Device
Version 1.5

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
B1	VREF0B1	IO	LVDS14p	INIT_DONE	1	1	D4	DM1L		
B1	VREF0B1	IO	LVDS14n	CRC_ERROR	2	2	C3	DQ1L0		
B1	VREF0B1	IO	LVDS13p	CLKUSR	3	3	C2	DQ1L1		
B1	VREF0B1	IO	LVDS13n		4	4	B1			
B1	VREF0B1	IO	VREF0B1		5	5	G5			
B1	VREF0B1	IO			6	6	F4	DQ1L2		
B1	VREF0B1	IO	LVDS12p		7	7	D3	DQ1L3	DQ0L0	DQ0L0
B1	VREF0B1	IO	LVDS12n			8	E4		DQ0L1	DQ0L1
B1	VREF0B1	VCCIO1			8	9				
B1	VREF0B1	GND			9	10				
B1	VREF0B1	IO	DPCLK1		10	11	F5	DQS0L	DQS0L	DQS0L
B1	VREF0B1	IO	LVDS11p			12	E3		DQ0L2	DQ0L2
B1	VREF0B1	IO	LVDS11n			13	D2		DQ0L3	DQ0L3
B1	VREF0B1	IO	LVDS10p			14	E2			
B1	VREF0B1	IO	LVDS10n			15	D1			
B1	VREF0B1	IO	LVDS9p			16	F3			
B1	VREF0B1	IO	LVDS9n			17	G3			
B1	VREF0B1	IO	LVDS8p			18	F2			
B1	VREF0B1	IO	LVDS8n			19	E1			
B1	VREF0B1	IO	LVDS7p			20	G2			
B1	VREF0B1	IO	LVDS7n			21	F1		DM0L	DM0L
B1	VREF0B1	VCCIO1				22				
B1	VREF1B1	IO	VREF1B1		11	23	H5			
B1	VREF1B1	IO		nCSO	12	24	G4			
B1	VREF1B1	DATA0		DATA0	13	25	H2			
B1	VREF1B1	nCONFIG		nCONFIG	14	26	H3			
	VREF1B1	VCCA_PLL1			15	27	H6			
B1	VREF1B1	CLK0	LVDSCLK1p		16	28	G1			
B1	VREF1B1	CLK1	LVDSCLK1n		17	29	H1			
	VREF1B1	GNDA_PLL1			18	30	J6			
	VREF1B1	GNDG_PLL1			19	31	J5			
B1	VREF1B1	nCEO		nCEO	20	32	H4			
B1	VREF1B1	nCE		nCE	21	33	J4			
B1	VREF1B1	MSEL0		MSEL0	22	34	J3			
B1	VREF1B1	MSEL1		MSEL1	23	35	J2			
B1	VREF1B1	DCLK		DCLK	24	36	K4			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
B1	VREF1B1	IO		ASDO	25	37	K3			
B1	VREF1B1	IO	PLL1_OUTp		26	38	J1			
B1	VREF1B1	IO	PLL1_OUTn		27	39	K2			
B1	VREF2B1	GND				40				
B1	VREF2B1	IO				41	L3			
B1	VREF2B1	IO	LVDS6p			42	K1			
B1	VREF2B1	IO	LVDS6n			43	L1			
B1	VREF2B1	IO	LVDS5p			44	L2			
B1	VREF2B1	IO	LVDS5n			45	M1			
B1	VREF2B1	IO	LVDS4p			46	N1			
B1	VREF2B1	IO	LVDS4n			47	M2			
B1	VREF2B1	IO	LVDS3p			48	N2		DQ0L4	DQ0L4
B1	VREF2B1	IO	LVDS3n			49	M3		DQ0L5	DQ0L5
B1	VREF2B1	IO	DPCLK0		28	50	L5	DQS1L	DQS1L	DQS1L
B1	VREF2B1	VCCIO1			29	51				
B1	VREF2B1	GND			30	52				
B1	VREF2B1	IO	LVDS2p			53	M4		DQ0L6	DQ0L6
B1	VREF2B1	IO	LVDS2n			54	N3		DQ0L7	DQ0L7
B1	VREF2B1	IO	VREF2B1		31	55	K5			
B1	VREF2B1	IO			32	56	L4	DQ1L4		
B1	VREF2B1	IO	LVDS1p		33	57	R1	DQ1L5		
B1	VREF2B1	IO	LVDS1n		34	58	P2	DQ1L6		
B1	VREF2B1	IO	LVDS0p		35	59	P3	DQ1L7		
B1	VREF2B1	IO	LVDS0n		36	60	N4			
B4	VREF2B4	IO	LVDS71p		37	61	R2			
B4	VREF2B4	IO	LVDS71n		38	62	T2			
B4	VREF2B4	IO	LVDS70p			63	R3			
B4	VREF2B4	IO	LVDS70n			64	P4			
B4	VREF2B4	IO	LVDS69p		39	65	R4	DQ1B7		
B4	VREF2B4	IO	LVDS69n		40	66	T4	DQ1B6		
B4	VREF2B4	IO	LVDS68p		41	67	R5	DQ1B5	DQ1B7	DQ1B7
B4	VREF2B4	IO	LVDS68n		42	68	P5	DQ1B4	DQ1B6	DQ1B6
B4	VREF2B4	GND			43	69				
B4	VREF2B4	VCCIO4			44	70				
	VREF2B4	GND			45	71				
	VREF2B4	VCCINT			46	72				

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
B4	VREF2B4	IO	DPCLK7		47	73	M5	DQS1B	DQS1B	DQS1B
B4	VREF2B4	IO	VREF2B4		48	74	M6			
B4	VREF2B4	IO	LVDS67p		49	75	N5			
B4	VREF2B4	IO	LVDS67n			76	N6		DQ1B5	DQ1B5
B4	VREF2B4	IO	LVDS66p			77	P6		DQ1B4	DQ1B4
B4	VREF2B4	IO	LVDS66n			78	R6			
B4	VREF2B4	IO				79	M7			
B4	VREF2B4	IO	LVDS65p			80	T6			
B4	VREF2B4	IO	LVDS65n			81	R7			
B4	VREF2B4	IO	LVDS64p			82	P7			
B4	VREF2B4	IO	LVDS64n			83	N7			
B4	VREF2B4	IO	LVDS63p		50	84	R8			
B4	VREF2B4	IO	LVDS63n		51	85	T8			
B4	VREF1B4	IO	LVDS62p		52	86	N8			
B4	VREF1B4	IO	LVDS62n		53	87	P8			
B4	VREF1B4	IO				88	M8			
	VREF1B4	GND			54	89				
	VREF1B4	VCCINT			55	90				
B4	VREF1B4	GND				91				
B4	VREF1B4	VCCIO4				92				
B4	VREF1B4	IO	VREF1B4		56	93	M10			
B4	VREF1B4	IO	LVDS61p		57	94	R9	DM1B	DM1B	DM1B
B4	VREF1B4	IO	LVDS61n		58	95	T9			
B4	VREF1B4	IO	LVDS60p			96	P9			
B4	VREF1B4	IO	LVDS60n			97	N9			
B4	VREF1B4	IO	LVDS59p			98	R10			
B4	VREF1B4	IO	LVDS59n		59	99	T11			
B4	VREF1B4	IO	LVDS58p			100	N10			
B4	VREF1B4	IO	LVDS58n			101	P10			
B4	VREF0B4	IO	LVDS57p			102	R11			
B4	VREF0B4	IO	LVDS57n			103	P11			
B4	VREF0B4	IO	LVDS56p			104	N11			
B4	VREF0B4	IO	LVDS56n			105	N12			
B4	VREF0B4	IO			60	106	M9			
B4	VREF0B4	IO	VREF0B4		61	107	M11			
B4	VREF0B4	IO	DPCLK6		62	108	M12	DQS0B	DQS0B	DQS0B

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
	VREF0B4	GND			63	109				
	VREF0B4	VCCINT			64	110				
B4	VREF0B4	GND			65	111				
B4	VREF0B4	VCCIO4			66	112				
B4	VREF0B4	IO	LVDS55p		67	113	P12	DQ1B3	DQ1B3	DQ1B3
B4	VREF0B4	IO	LVDS55n		68	114	R12	DQ1B2	DQ1B2	DQ1B2
B4	VREF0B4	IO	LVDS54p		69	115	T13	DQ1B1	DQ1B1	DQ1B1
B4	VREF0B4	IO	LVDS54n		70	116	R13	DQ1B0	DQ1B0	DQ1B0
B4	VREF0B4	IO	LVDS53p			117	R14			
B4	VREF0B4	IO	LVDS53n			118	P13			
B4	VREF0B4	IO	LVDS52p		71	119	T15			
B4	VREF0B4	IO	LVDS52n		72	120	R15			
B3	VREF2B3	IO	LVDS51n		73	121	N13			
B3	VREF2B3	IO	LVDS51p		74	122	P14			
B3	VREF2B3	IO	LVDS50n		75	123	P15			
B3	VREF2B3	IO	LVDS50p		76	124	R16			
B3	VREF2B3	IO	LVDS49n		77	125	N15	DQ1R7	DQ1R7	DQ1R7
B3	VREF2B3	IO	LVDS49p		78	126	N16	DQ1R6		
B3	VREF2B3	IO	VREF2B3		79	127	K12			
B3	VREF2B3	IO				128	K14		DQ1R6	DQ1R6
B3	VREF2B3	GND			80	129				
B3	VREF2B3	VCCIO3			81	130				
B3	VREF2B3	IO	DPCLK5		82	131	L12	DQS1R	DQS1R	DQS1R
B3	VREF2B3	IO	LVDS48n		83	132	N14	DQ1R5	DQ1R5	DQ1R5
B3	VREF2B3	IO	LVDS48p		84	133	M13	DQ1R4	DQ1R4	DQ1R4
B3	VREF2B3	IO	LVDS47n		85	134	M14	DM1R		
B3	VREF2B3	IO	LVDS47p			135	L13			
B3	VREF2B3	IO	LVDS46n			136	M15			
B3	VREF2B3	IO	LVDS46p			137	M16			
B3	VREF2B3	IO	LVDS45n			138	L14			
B3	VREF2B3	IO	LVDS45p			139	L15			
B3	VREF2B3	IO	LVDS44n			140	L16			
B3	VREF2B3	IO	LVDS44p			141	K16			
B3	VREF2B3	GND				142				
B3	VREF1B3	IO	PLL2_OUTn			143	K15			
B3	VREF1B3	IO	PLL2_OUTp			144	J16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
B3	VREF1B3	CONF_DONE		CONF_DONE	86	145	K13			
B3	VREF1B3	nSTATUS		nSTATUS	87	146	J13			
B3	VREF1B3	TCK		TCK	88	147	J14			
B3	VREF1B3	TMS		TMS	89	148	J15			
B3	VREF1B3	TDO		TDO	90	149	H15			
	VREF1B3	GNDG_PLL2			91	150	J12			
	VREF1B3	GNDA_PLL2				151	J11			
B3	VREF1B3	CLK3	LVDSCLK2n		92	152	H16			
B3	VREF1B3	CLK2	LVDSCLK2p		93	153	G16			
	VREF1B3	VCCA_PLL2			94	154	H11			
B3	VREF1B3	TDI		TDI	95	155	H14			
B3	VREF1B3	IO	VREF1B3		96	156	H12			
B3	VREF0B3	VCCIO3				157				
B3	VREF0B3	IO	LVDS43n			158	G14		DM1R	DM1R
B3	VREF0B3	IO	LVDS43p			159	G13			
B3	VREF0B3	IO	LVDS42n			160	G15			
B3	VREF0B3	IO	LVDS42p			161	F16			
B3	VREF0B3	IO	LVDS41n			162	F14			
B3	VREF0B3	IO	LVDS41p			163	F13			
B3	VREF0B3	IO	LVDS40n			164	F15			
B3	VREF0B3	IO	LVDS40p			165	E16			
B3	VREF0B3	IO	LVDS39n			166	E15			
B3	VREF0B3	IO	LVDS39p		97	167	D16	DQ1R3		
B3	VREF0B3	IO	LVDS38n		98	168	D15	DQ1R2		
B3	VREF0B3	IO	LVDS38p		99	169	E14	DQ1R1	DQ1R3	DQ1R3
B3	VREF0B3	IO	DPCLK4		100	170	F12	DQS0R	DQS0R	DQS0R
B3	VREF0B3	GND			101	171				
B3	VREF0B3	VCCIO3			102	172				
B3	VREF0B3	IO	LVDS37n			173	E13		DQ1R2	DQ1R2
B3	VREF0B3	IO	LVDS37p			174	D14		DQ1R1	DQ1R1
B3	VREF0B3	IO			103	175	H13	DQ1R0	DQ1R0	DQ1R0
B3	VREF0B3	IO	VREF0B3		104	176	G12			
B3	VREF0B3	IO	LVDS36n		105	177	B16			
B3	VREF0B3	IO	LVDS36p		106	178	C15			
B3	VREF0B3	IO	LVDS35n		107	179	C14			
B3	VREF0B3	IO	LVDS35p		108	180	D13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
B2	VREF0B2	IO	LVDS34n		109	181	B15			
B2	VREF0B2	IO	LVDS34p		110	182	A15			
B2	VREF0B2	IO	LVDS33n			183	B14			
B2	VREF0B2	IO	LVDS33p			184	C13			
B2	VREF0B2	IO	LVDS32n		111	185	B13	DQ0T0	DQ0T0	DQ0T0
B2	VREF0B2	IO	LVDS32p		112	186	A13	DQ0T1	DQ0T1	DQ0T1
B2	VREF0B2	IO	LVDS31n		113	187	B12	DQ0T2	DQ0T2	DQ0T2
B2	VREF0B2	IO	LVDS31p		114	188	C12	DQ0T3	DQ0T3	DQ0T3
B2	VREF0B2	VCCIO2			115	189				
B2	VREF0B2	GND			116	190				
	VREF0B2	VCCINT			117	191				
	VREF0B2	GND			118	192				
B2	VREF0B2	IO	DPCLK3		119	193	E12	DQS0T	DQS0T	DQS0T
B2	VREF0B2	IO	VREF0B2		120	194	E11			
B2	VREF0B2	IO			121	195	E9			
B2	VREF0B2	IO	LVDS30n			196	D12			
B2	VREF0B2	IO	LVDS30p			197	D11			
B2	VREF0B2	IO	LVDS29n			198	C11			
B2	VREF0B2	IO	LVDS29p			199	B11			
B2	VREF1B2	IO	LVDS28n			200	A11			
B2	VREF1B2	IO	LVDS28p			201	B10			
B2	VREF1B2	IO	LVDS27n		122	202	C10			
B2	VREF1B2	IO	LVDS27p			203	D10			
B2	VREF1B2	IO	LVDS26n			204	A9			
B2	VREF1B2	IO	LVDS26p			205	B9			
B2	VREF1B2	IO	LVDS25n		123	206	D9	DM0T	DM0T	DM0T
B2	VREF1B2	IO	LVDS25p		124	207	C9			
B2	VREF1B2	IO	VREF1B2		125	208	E10			
B2	VREF1B2	VCCIO2				209				
B2	VREF1B2	GND				210				
	VREF1B2	VCCINT			126	211				
	VREF1B2	GND			127	212				
B2	VREF1B2	IO				213	E8			
B2	VREF1B2	IO	LVDS24n		128	214	C8			
B2	VREF1B2	IO	LVDS24p		129	215	D8			
B2	VREF2B2	IO	LVDS23n		130	216	A8			

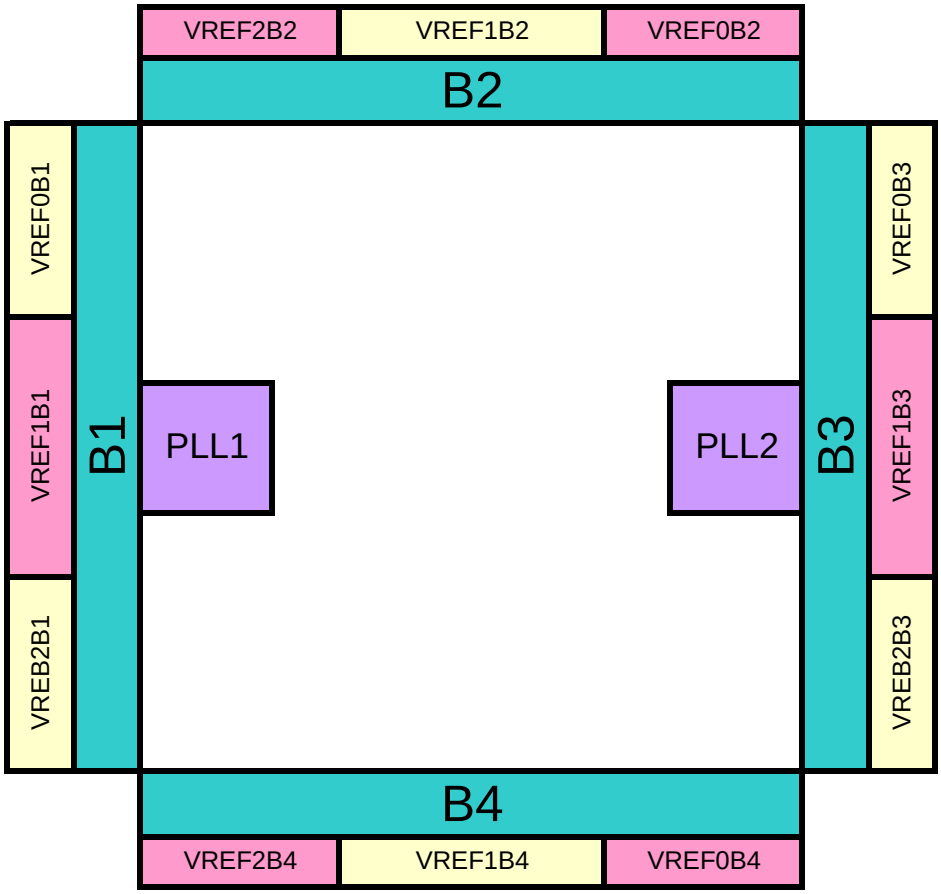
Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
B2	VREF2B2	IO	LVDS23p		131	217	B8			
B2	VREF2B2	IO	LVDS22n			218	D7			
B2	VREF2B2	IO	LVDS22p			219	C7			
B2	VREF2B2	IO	LVDS21n			220	B7			
B2	VREF2B2	IO	LVDS21p			221	A6			
B2	VREF2B2	IO				222	E7			
B2	VREF2B2	IO	LVDS20n			223	B6			
B2	VREF2B2	IO	LVDS20p			224	C6			
B2	VREF2B2	IO	LVDS19n			225	D6			
B2	VREF2B2	IO	LVDS19p		132	226	D5			
B2	VREF2B2	IO	VREF2B2		133	227	E6			
B2	VREF2B2	IO	DPCLK2		134	228	E5	DQS1T	DQS1T	DQS1T
	VREF2B2	VCCINT			135	229				
	VREF2B2	GND			136	230				
B2	VREF2B2	VCCIO2			137	231				
B2	VREF2B2	GND			138	232				
B2	VREF2B2	IO	LVDS18n		139	233	C5	DQ0T4	DQ0T4	DQ0T4
B2	VREF2B2	IO	LVDS18p		140	234	B5	DQ0T5	DQ0T5	DQ0T5
B2	VREF2B2	IO	LVDS17n		141	235	A4	DQ0T6	DQ0T6	DQ0T6
B2	VREF2B2	IO	LVDS17p		142	236	B4	DQ0T7	DQ0T7	DQ0T7
B2	VREF2B2	IO	LVDS16n			237	C4			
B2	VREF2B2	IO	LVDS16p			238	B3			
B2	VREF2B2	IO	LVDS15n	DEV_OE	143	239	A2			
B2	VREF2B2	IO	LVDS15p	DEV_CLRn	144	240	B2			
		VCCINT					A7			
		VCCINT					A10			
		VCCINT					G8			
		VCCINT					G10			
		VCCINT					H7			
		VCCINT					H9			
		VCCINT					J8			
		VCCINT					J10			
		VCCINT					K7			
		VCCINT					K9			
		VCCINT					T7			
		VCCINT					T10			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
		VCCIO1					C1			
		VCCIO1					G6			
		VCCIO1					P1			
		VCCIO4					T3			
		VCCIO4					L7			
		VCCIO4					L10			
		VCCIO4					T14			
		VCCIO3					P16			
		VCCIO3					K11			
		VCCIO3					C16			
		VCCIO2					A14			
		VCCIO2					F10			
		VCCIO2					F7			
		VCCIO2					A3			
		GND					A1			
		GND					A16			
		GND					A5			
		GND					A12			
		GND					F6			
		GND					F8			
		GND					F9			
		GND					F11			
		GND					G7			
		GND					G9			
		GND					G11			
		GND					H8			
		GND					H10			
		GND					J7			
		GND					J9			
		GND					K6			
		GND					K8			
		GND					K10			
		GND					L6			
		GND					L8			
		GND					L9			
		GND					L11			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	T144	Q240	F256	DQS for x8 in the T144	DQS for x8 in the Q240	DQS for x8 in the F256
		GND					T1			
		GND					T5			
		GND					T12			
		GND					T16			

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL[1..2]	Power	Analog power for PLLs[1..2]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..2]	Ground	Analog ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
GNDG_PLL[1..2]	Ground	Guard ring ground for PLLs[1..2]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	No connect pins should not be connected on the board. They should be left floating.
		Configuration and JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.
		Clock and PLL Pins
CLK0	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK0 is LVDSCLK1p, which is used for differential input to PLL1.
CLK1	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK1 is LVDSCLK1n, which is used for differential input to PLL1.
CLK2	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK2 is LVDSCLK2p, which is used for differential input to PLL2.
CLK3	Input, LVDS Input	Dedicated global clock input. The dual-function of CLK3 is LVDSCLK2n, which is used for differential input to PLL2.
DPCLK[7..0]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
PLL1_OUTp	I/O, Output	External clock output from PLL 1. This pin can be used with differential or single ended I/O standards. If clock output from PLL1 is not used, this pin is available as a user I/O pin.
PLL1_OUTn	I/O, Output	Negative terminal for external clock output from PLL1. If the clock output is single ended, this pin is available as a user I/O pin.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL2_OUTp	I/O, Output	External clock output from PLL 2. This pin can be used with differential or single ended I/O standards. If clock output from PLL2 is not used, this pin is available as a user I/O pin. The EP1C6T144 does not support this output pin.
PLL2_OUTn	I/O, Output	Negative terminal for external clock output from PLL2. If the clock output is single ended, this pin is available as a user I/O pin. The EP1C6T144 does not support this output pin.
Dual-Purpose LVDS & External Memory Interface Pins		
LVDS[0..71]p	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 71. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins. Both the positive pin and negative pin needs to be bonded out in order to use the LVDS channel.
LVDS[0..71]n	I/O, LVDS RX or TX	Dual-purpose LVDS I/O channels 0 to 71. These channels can be used for receiving or transmitting LVDS compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for LVDS interfacing, these pins are available as user I/O pins. Both the positive pin and negative pin needs to be bonded out in order to use the LVDS channel.
LVDSCLK1p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK0 input pin.
LVDSCLK1n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL1. If differential input to PLL1 is not required, this pin is available as the CLK1 input pin.
LVDSCLK2p	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK2 input pin.
LVDSCLK2n	Input, LVDS Input	Dual-purpose LVDS clock input to PLL2. If differential input to PLL2 is not required, this pin is available as the CLK3 input pin.
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.



Notes:

1.This is a top view of the silicon die.

2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

Bank & PLL Diagram

Version Number	Date	Changes Made
1.5	3/6/2006	Added CRC_ERROR pin in Pin List and Pin Definitions