



Bank Number	REF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A		TDO		TDO			U4							
3A		ACS0		DATA4			AA1							
3A		TMS		TMS			V2							
3A		AS_DATA3		DATA3			AB2							
3A		TCK		TCK			W3							
3A		AS_DATA2		DATA2			W3							
3A		TDI		TDI			W4							
3A		AS_DATA1		DATA1			AA2							
3A		DCLK		DCLK			V4							
3A		AS_DATA0/ASDD		DATA0			AB3							
3A	VREFB3A0	IO		DATA6	DIFFO_RX_B1n	DIFFOUT_B1n	Y5	DQ1B						
3A	VREFB3A0	IO		DATA5	DIFFO_TX_B2n	DIFFOUT_B2n	AB5							
3A	VREFB3A0	IO		DATA8	DIFFO_RX_B1p	DIFFOUT_B1p	W6	DQ1B						
3A	VREFB3A0	IO		DATA7	DIFFO_TX_B0p	DIFFOUT_B0p	AA5	DQ1B						
3A	VREFB3A0	IO		DATA10	DIFFO_RX_B3n	DIFFOUT_B3n	V5	DQS1B						
3A	VREFB3A0	IO		DATA9	DIFFO_TX_B4n	DIFFOUT_B4n	AB7	DQ1B						
3A	VREFB3A0	IO		DATA12	DIFFO_RX_B3p	DIFFOUT_B3p	U6	DQS1B						
3A	VREFB3A0	IO		DATA11	DIFFO_TX_B4p	DIFFOUT_B4p	AA6							
3A	VREFB3A0	IO		DATA14	DIFFO_RX_B5n	DIFFOUT_B5n	V7	DQ1B						
3A	VREFB3A0	IO		DATA13	DIFFO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B						
3A	VREFB3A0	IO		CLKUSR			U7	DQ1B						
3A	VREFB3A0	IO		DATA15	DIFFO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B						
3A	VREFB3A0	IO		PR_DONE	DIFFO_RX_B7n	DIFFOUT_B7n	W7							
3A	VREFB3A0	IO		PR_READY	DIFFO_TX_B8n	DIFFOUT_B8n	W8	DQ1B						
3A	VREFB3A0	IO		PR_ERROR	DIFFO_RX_B7p	DIFFOUT_B7p	V6							
3A	VREFB3A0	IO			DIFFO_TX_B8p	DIFFOUT_B8p	V9	DQ1B						
3B	VREFB3B0	IO	CLK0n,FPLL_BL_FBn		DIFFO_RX_B15n	DIFFOUT_B15n	V10							
3B	VREFB3B0	IO	CLK0p,FPLL_BL_FBp		DIFFO_TX_B15p	DIFFOUT_B15p	V10							
3B	VREFB3B0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFO_TX_B21n	DIFFOUT_B21n	AB10							
3B	VREFB3B0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFO_TX_B21p	DIFFOUT_B21p	AB9							
3B	VREFB3B0	IO	CLK1n		DIFFO_RX_B23n	DIFFOUT_B23n	AB8							
3B	VREFB3B0	IO	CLK1p		DIFFO_TX_B23p	DIFFOUT_B23p	AA8							
4A	VREFB4A0	IO	RZQ_0		DIFFO_TX_B25n	DIFFOUT_B25n	AA11							
4A	VREFB4A0	IO			DIFFO_RX_B26n	DIFFOUT_B26n	AB13	DQ2B						
4A	VREFB4A0	IO			DIFFO_TX_B25p	DIFFOUT_B25p	W11	DQ2B						
4A	VREFB4A0	IO			DIFFO_RX_B26p	DIFFOUT_B26p	AB12	DQ2B						
4A	VREFB4A0	IO			DIFFO_TX_B27n	DIFFOUT_B27n	W11	DQS2B						
4A	VREFB4A0	IO			DIFFO_TX_B26n	DIFFOUT_B26n	AB14	DQ2B						
4A	VREFB4A0	IO			DIFFO_TX_B27p	DIFFOUT_B27p	W11	DQS2B						
4A	VREFB4A0	IO			DIFFO_TX_B28p	DIFFOUT_B28p	AA13							
4A	VREFB4A0	IO			DIFFO_TX_B29n	DIFFOUT_B29n	AB17	DQ2B						
4A	VREFB4A0	IO			DIFFO_RX_B30n	DIFFOUT_B30n	AB15	DQ2B						
4A	VREFB4A0	IO			DIFFO_TX_B29p	DIFFOUT_B29p	AA16	DQ2B						
4A	VREFB4A0	IO			DIFFO_RX_B30p	DIFFOUT_B30p	AA15	DQ2B						
4A	VREFB4A0	IO	CLK2n		DIFFO_RX_B31n	DIFFOUT_B31n	Y14							
4A	VREFB4A0	IO	CLK2p		DIFFO_TX_B32n	DIFFOUT_B32n	AB20	DQ2B						
4A	VREFB4A0	IO	CLK3p		DIFFO_RX_B31p	DIFFOUT_B31p	W14							
4A	VREFB4A0	IO			DIFFO_TX_B32p	DIFFOUT_B32p	AB19	DQ2B						
4A	VREFB4A0	IO	CLK3n		DIFFO_RX_B33n	DIFFOUT_B33n	Y13							
4A	VREFB4A0	IO	CLK3p		DIFFO_TX_B33p	DIFFOUT_B33p	W12							
4A	VREFB4A0	IO			DIFFO_TX_B53n	DIFFOUT_B53n	AB18							
4A	VREFB4A0	IO			DIFFO_RX_B54n	DIFFOUT_B54n	Y16							
4A	VREFB4A0	IO			DIFFO_TX_B53p	DIFFOUT_B53p	AA18							
4A	VREFB4A0	IO			DIFFO_RX_B54p	DIFFOUT_B54p	Y15							
5A	VREFB5A0	IO	RZQ_1		DIFFO_TX_R1p	DIFFOUT_R1p	Y19	DQ1R						
5A	VREFB5A0	IO		INT_DONE	DIFFO_RX_R2p	DIFFOUT_R2p	W17							
5A	VREFB5A0	IO		PR_REQUEST	DIFFO_TX_R1n	DIFFOUT_R1n	V20	DQ1R						
5A	VREFB5A0	IO		CRC_ERROR	DIFFO_RX_R2n	DIFFOUT_R2n	W18							
5A	VREFB5A0	IO		ICE0	DIFFO_TX_R3p	DIFFOUT_R3p	AA21	DQ1R						
5A	VREFB5A0	IO			DIFFO_RX_R4n	DIFFOUT_R4n	U18							
5A	VREFB5A0	IO		CvP_CONFDONE	DIFFO_TX_R3n	DIFFOUT_R3n	Y21	DQ1R						
5A	VREFB5A0	IO			DIFFO_RX_R4n	DIFFOUT_R4n	V19	DQ1R						
5A	VREFB5A0	IO		DEV_0E	DIFFO_TX_R5p	DIFFOUT_R5p	AB22							
5A	VREFB5A0	IO			DIFFO_RX_R6p	DIFFOUT_R6p	V16	DQS1R						
5A	VREFB5A0	IO		DEV CLRn	DIFFO_TX_R5n	DIFFOUT_R5n	AA22	DQ1R						
5A	VREFB5A0	IO			DIFFO_RX_R6n	DIFFOUT_R6n	U17	DQS1R						
5A	VREFB5A0	IO			DIFFO_TX_R7p	DIFFOUT_R7p	V20							
5A	VREFB5A0	IO			DIFFO_RX_R8p	DIFFOUT_R8p	V15	DQ1R						
5A	VREFB5A0	IO			DIFFO_TX_R7n	DIFFOUT_R7n	W21							
5A	VREFB5A0	IO			DIFFO_RX_R8n	DIFFOUT_R8n	W16	DQ1R						
6B	VREFB6B0_HPS	HPS_DDR					R16		HPS_DM_3				HPS_DM_3	
6B	VREFB6B0_HPS	HPS_DDR					T17		HPS_DO_31				HPS_DO_31	
6B	VREFB6B0_HPS	HPS_DDR					F18		HPS_DO_29				HPS_DO_29	
6B	VREFB6B0_HPS	HPS_DDR					F18		HPS_DO_30				HPS_DO_30	
6B	VREFB6B0_HPS	HPS_DDR					F18		HPS_DO_28				HPS_DO_28	
6B	VREFB6B0_HPS	VREFB6B0_HPS					U20							
6B	VREFB6B0_HPS	HPS_DDR					M15		HPS_DQS_3				HPS_DQS_3	
6B	VREFB6B0_HPS	HPS_DDR					N15		HPS_DQS#_3				HPS_DQS#_3	
6B	VREFB6B0_HPS	HPS_DDR					V22		HPS_DO_27				HPS_DO_27	
6B	VREFB6B0_HPS	HPS_DDR					R15		HPS_DO_25				HPS_DO_25	
6B	VREFB6B0_HPS	HPS_DDR					T20		HPS_DO_26				HPS_DO_26	
6B	VREFB6B0_HPS	HPS_DDR					N17		HPS_DO_24				HPS_DO_24	
6B	VREFB6B0_HPS	HPS_DDR					U19		HPS_DM_2				HPS_DM_2	
6B	VREFB6B0_HPS	HPS_DDR					R20		HPS_DO_23				HPS_DO_23	
6B	VREFB6B0_HPS	HPS_DDR					N16		HPS_DO_21				HPS_DO_21	
6B	VREFB6B0_HPS	HPS_DDR					V21		HPS_DO_22				HPS_DO_22	
6B	VREFB6B0_HPS	HPS_DDR					F16		HPS_DO_20				HPS_DO_20	
6B	VREFB6B0_HPS	HPS_DDR					M14		HPS_DQS_2				HPS_DQS_2	
6B	VREFB6B0_HPS	HPS_DDR					W22		HPS_RESET#				HPS_RESET#	
6B	VREFB6B0_HPS	HPS_DDR					P14		HPS_DQS#_2				HPS_DQS#_2	
6B	VREFB6B0_HPS	HPS_DDR					U22		HPS_DO_19				HPS_DO_19	
6B	VREFB6B0_HPS	HPS_DDR					W19		HPS_DO_17				HPS_DO_17	
6B	VREFB6B0_HPS	HPS_DDR					R19		HPS_DO_18				HPS_DO_18	
6B	VREFB6B0_HPS	HPS_DDR					M17		HPS_DO_16				HPS_DO_16	
6A	VREFB6A0_HPS	HPS_DDR					T22		HPS_DM_1				HPS_DM_1	
6A	VREFB6A0_HPS	HPS_DDR					R21		HPS_DO_15				HPS_DO_15	
6A	VREFB6A0_HPS	HPS_DDR					L18		HPS_DO_13				HPS_DO_13	
6A	VREFB6A0_HPS	HPS_DDR					F22		HPS_DO_14				HPS_DO_14	
6A	VREFB6A0_HPS	HPS_DDR					L16		HPS_DO_12				HPS_DO_12	
6A	VREFB6A0_HPS	HPS_DDR					T21		HPS_CKE_0				HPS_CKE_0	
6A	VREFB6A0_HPS	HPS_DDR					M14		HPS_DQS_1				HPS_DQS_1	
6A	VREFB6A0_HPS	HPS_DDR					R21		HPS_CKE_1				HPS_CKE_1	
6A	VREFB6A0_HPS	HPS_DDR					N13		HPS_DQS#_1				HPS_DQS#_1	
6A	VREFB6A0_HPS	HPS_DDR					N20		HPS_DO_11				HPS_DO_11	
6A	VREFB6A0_HPS	HPS_DDR					K19		HPS_DO_9				HPS_DO_9	
6A	VREFB6A0_HPS	HPS_DDR					N21		HPS_DO_10				HPS_DO_10	
6A	VREFB6A0_HPS	HPS_DDR					R20		HPS_DO_8				HPS_DO_8	
6A	VREFB6A0_HPS	HPS_DDR					M20		HPS_DM_0				HPS_DM_0	
6A	VREFB6A0_HPS	HPS_DDR					M22		HPS_DO_7				HPS_DO_7	
6A	VREFB6A0_HPS	HPS_DDR					K16		HPS_DO_5				HPS_DO_5	
6A	VREFB6A0_HPS	HPS_DDR					L22		HPS_DO_6				HPS_DO_6	
6A	VREFB6A0_HPS	HPS_DDR					K18		HPS_DO_4				HPS_DO_4	
6A	VREFB6A0_HPS	HPS_DDR					N19		HPS_ODT_1				HPS_ODT_1	
6A	VREFB6A0_HPS	HPS_DDR					L15		HPS_DQS_0				HPS_DQS_0	



Bank Number	WEPF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFB6A0_HPS	HPS_DDR					L20		HPS.ODT_0	HPS.ODT_0				
6A	VREFB6A0_HPS	HPS_DDR					K14		HPS.DQS#_0	HPS.DQS#_0				
6A	VREFB6A0_HPS	HPS_DDR					K21		HPS.DQ_3	HPS.DQ_3				
6A	VREFB6A0_HPS	HPS_DDR					J19		HPS.DQ_1	HPS.DQ_1				
6A	VREFB6A0_HPS	HPS_DDR					M20		HPS.DQ_2	HPS.DQ_2				
6A	VREFB6A0_HPS	HPS_DDR					J18		HPS.DQ_0	HPS.DQ_0				
6A	VREFB6A0_HPS	VREFB6A0_HPS					H19							
6A	VREFB6A0_HPS	HPS_DDR					L21		HPS.A_0	HPS.A_0				
6A	VREFB6A0_HPS	HPS_DDR					J22		HPS.A_1	HPS.A_1				
6A	VREFB6A0_HPS	HPS_DDR					H17		HPS.A_4	HPS.A_4				
6A	VREFB6A0_HPS	HPS_DDR					J21		HPS.A_2	HPS.A_2				
6A	VREFB6A0_HPS	HPS_DDR					J19		HPS.A_5	HPS.A_5				
6A	VREFB6A0_HPS	HPS_DDR					H20		HPS.A_3	HPS.A_3				
6A	VREFB6A0_HPS	HPS_DDR					K15		HPS.CK	HPS.CK				
6A	VREFB6A0_HPS	HPS_DDR					H22		HPS.A_6	HPS.A_6				
6A	VREFB6A0_HPS	HPS_DDR					J14		HPS.CK#	HPS.CK#				
6A	VREFB6A0_HPS	HPS_DDR					H21		HPS.A_7	HPS.A_7				
6A	VREFB6A0_HPS	HPS_DDR					G20		HPS.BA_1					
6A	VREFB6A0_HPS	HPS_DDR					G22		HPS.BA_0					
6A	VREFB6A0_HPS	HPS_DDR					G18		HPS.BA_2					
6A	VREFB6A0_HPS	HPS_DDR					F20		HPS.CAS#					
6A	VREFB6A0_HPS	HPS_DDR					F21		HPS.RAS#					
6A	VREFB6A0_HPS	HPS_DDR					G22		HPS.A_8	HPS.A_8				
6A	VREFB6A0_HPS	HPS_DDR					F22		HPS.A_10					
6A	VREFB6A0_HPS	HPS_DDR					B22		HPS.A_9	HPS.A_9				
6A	VREFB6A0_HPS	HPS_DDR					E19		HPS.A_11					
6A	VREFB6A0_HPS	HPS_DDR					H15		HPS.CS#_0	HPS.CS#_0				
6A	VREFB6A0_HPS	HPS_DDR					G20		HPS.A_12					
6A	VREFB6A0_HPS	HPS_DDR					J16		HPS.CS#_1	HPS.CS#_1				
6A	VREFB6A0_HPS	HPS_DDR					E21		HPS.A_13					
6A	VREFB6A0_HPS	HPS_DDR					G21		HPS.A_14					
6A	VREFB6A0_HPS	HPS_DDR					D22		HPS.VEN#					
6A	VREFB6A0_HPS	HPS_DDR					E18		HPS.A_15					
6A	VREFB6A0_HPS	HPS_RZQ_0					D21							
		GND					G17							
		GND					F17							
7A		HPS_nRST					D18							
7A		HPS_nPOR					E16							
7A		HPS_TDO					B18							
7A		VCCRSTCLK_HPS					G15							
7A		HPS_TMS					D17							
7A		HPS_TCK					J13							
7A		HPS_TRST					H14							
7A		HPS_TDI					F16							
7A		GND					F15							
7A		HPS_PORSEL					G14							
7A		HPS_CLK1					C16							
7A		HPS_CLK2					E14							
7A	VREFB7A7B7C7D0_HPS	TRACE_CLK					B15				TRACE_CLK			HPS_GP048
7A	VREFB7A7B7C7D0_HPS	TRACE_D0					D19				TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GP049
7A	VREFB7A7B7C7D0_HPS	TRACE_D1					C15				TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GP050
7A	VREFB7A7B7C7D0_HPS	TRACE_D2					C20				TRACE_D2	SPIS0_MISO	IC1_SDA	HPS_GP051
7A	VREFB7A7B7C7D0_HPS	TRACE_D3					F13				TRACE_D3	SPIS0_SCK	IC1_SCL	HPS_GP052
7A	VREFB7A7B7C7D0_HPS	TRACE_D4					C19				TRACE_D4	SPIS1_CLK	CAN1_RX	HPS_GP053
7A	VREFB7A7B7C7D0_HPS	TRACE_D5					C14				TRACE_D5	SPIS1_MOSI	CAN1_TX	HPS_GP054
7A	VREFB7A7B7C7D0_HPS	TRACE_D6					B19				TRACE_D6	SPIS1_SCK	IC0_SDA	HPS_GP055
7A	VREFB7A7B7C7D0_HPS	TRACE_D7					B20				TRACE_D7	SPIS1_MISO	IC0_SCL	HPS_GP056
7A	VREFB7A7B7C7D0_HPS	SPIM0_CLK					A21				SPIM0_CLK	IC1_SDA	UART0_CTS	HPS_GP057
7A	VREFB7A7B7C7D0_HPS	SPIM0_MOSI					A22				SPIM0_MOSI	IC1_SCL	UART0_RTS	HPS_GP058
7A	VREFB7A7B7C7D0_HPS	SPIM0_MISO					A20				SPIM0_MISO	CAN1_RX	UART1_CTS	HPS_GP059
7A	VREFB7A7B7C7D0_HPS	SPIM0_SS0/BOOTSEL0					D14				SPIM0_SS0	CAN1_TX	UART1_RTS	HPS_GP060
7A	VREFB7A7B7C7D0_HPS	UART0_RX					A16				UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GP061
7A	VREFB7A7B7C7D0_HPS	UART0_TX/CLKSEL1					E13				UART0_TX	CAN0_TX	SPIM1_SS1	HPS_GP062
7A	VREFB7A7B7C7D0_HPS	IC0_SDA					A15				IC0_SDA	UART1_RX	SPIM1_CLK	HPS_GP063
7A	VREFB7A7B7C7D0_HPS	IC0_SCL					A18				IC0_SCL	UART1_TX	SPIM1_MOSI	HPS_GP064
7A	VREFB7A7B7C7D0_HPS	CAN0_RX					B14				CAN0_RX	UART0_RX	SPIM1_MISO	HPS_GP065
7A	VREFB7A7B7C7D0_HPS	CAN0_TX/CLKSEL0					A17				CAN0_TX	UART0_TX	SPIM1_SS0	HPS_GP066
7B	VREFB7A7B7C7D0_HPS	NAND_ALE					J11				NAND_ALE	RGMI1_TX_CLK	OSPI_SS3	HPS_GP014
7B	VREFB7A7B7C7D0_HPS	NAND_CE					J12				NAND_CE	RGMI1_TXD0	USB1_D0	HPS_GP015
7B	VREFB7A7B7C7D0_HPS	NAND_CLE					J8				NAND_CLE	RGMI1_TXD1	USB1_D1	HPS_GP016
7B	VREFB7A7B7C7D0_HPS	NAND_RE					D13				NAND_RE	RGMI1_TXD2	USB1_D2	HPS_GP017
7B	VREFB7A7B7C7D0_HPS	NAND_RB					H12				NAND_RB	RGMI1_TXD3	USB1_D3	HPS_GP018
7B	VREFB7A7B7C7D0_HPS	NAND_D00					B13				NAND_D00	RGMI1_RXD0	USB1_D0	HPS_GP019
7B	VREFB7A7B7C7D0_HPS	NAND_D01					H10				NAND_D01	RGMI1_RXD1	IC3_SDA	HPS_GP020
7B	VREFB7A7B7C7D0_HPS	NAND_D02					C12				NAND_D02	RGMI1_MDC	IC3_SCL	HPS_GP021
7B	VREFB7A7B7C7D0_HPS	NAND_D03					H11				NAND_D03	RGMI1_RX_CTL	USB1_D4	HPS_GP022
7B	VREFB7A7B7C7D0_HPS	NAND_D04					A13				NAND_D04	RGMI1_TX_CTL	USB1_D5	HPS_GP023
7B	VREFB7A7B7C7D0_HPS	NAND_D05					C12				NAND_D05	RGMI1_RX_CLK	USB1_D6	HPS_GP024
7B	VREFB7A7B7C7D0_HPS	NAND_D06					G10				NAND_D06	RGMI1_RXD1	USB1_D7	HPS_GP025
7B	VREFB7A7B7C7D0_HPS	NAND_D07					E11				NAND_D07	RGMI1_RXD2	USB1_D8	HPS_GP026
7B	VREFB7A7B7C7D0_HPS	NAND_WP					A12				NAND_WP	RGMI1_RXD3	OSPI_SS2	HPS_GP027
7B	VREFB7A7B7C7D0_HPS	NAND_WE/BOOTSEL2					B12				NAND_WE	OSPI_SS1		HPS_GP028
7B	VREFB7A7B7C7D0_HPS	OSPI_I00					D11				OSPI_I00		USB1_CLK	HPS_GP029
7B	VREFB7A7B7C7D0_HPS	OSPI_I01					D12				OSPI_I01		USB1_STP	HPS_GP030
7B	VREFB7A7B7C7D0_HPS	OSPI_I02					F10				OSPI_I02		USB1_D9	HPS_GP031
7B	VREFB7A7B7C7D0_HPS	OSPI_I03					F11				OSPI_I03		USB1_NXT	HPS_GP032
7B	VREFB7A7B7C7D0_HPS	OSPI_SS0/BOOTSEL1					A11				OSPI_SS0			HPS_GP033
7B	VREFB7A7B7C7D0_HPS	OSPI_CLK					C11				OSPI_CLK			HPS_GP034
7C	VREFB7A7B7C7D0_HPS	IO					G8				SDMMC_CMD			HPS_GP036
7C	VREFB7A7B7C7D0_HPS	IO					E8				SDMMC_PWREN			HPS_GP037
7C	VREFB7A7B7C7D0_HPS	IO					B10				SDMMC_D0			HPS_GP038
7C	VREFB7A7B7C7D0_HPS	IO					A10				SDMMC_D1			HPS_GP039
7C	VREFB7A7B7C7D0_HPS	IO					C10				SDMMC_D2			HPS_GP040
7C	VREFB7A7B7C7D0_HPS	IO					E9				SDMMC_CCLK_OUT			HPS_GP045
7C	VREFB7A7B7C7D0_HPS	IO					F8				SDMMC_D3			HPS_GP046
7C	VREFB7A7B7C7D0_HPS	IO					B9				SDMMC_D4			HPS_GP047
7D	VREFB7A7B7C7D0_HPS	RGMI0_TX_CLK					H7				RGMI0_TX_CLK			HPS_GP000
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD0					F7				RGMI0_TXD0	USB1_D0		HPS_GP001
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD1					G7				RGMI0_TXD1	USB1_D1		HPS_GP002
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD2					A8				RGMI0_TXD2	USB1_D2		HPS_GP003
7D	VREFB7A7B7C7D0_HPS	RGMI0_TXD3					D8				RGMI0_TXD3	USB1_D3		HPS_GP004
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD0					F6				RGMI0_RXD0	USB1_D4		HPS_GP005
7D	VREFB7A7B7C7D0_HPS	RGMI0_MDO					A7				RGMI0_MDO	USB1_D5	IC2_SDA	HPS_GP006
7D	VREFB7A7B7C7D0_HPS	RGMI0_MDC					G7				RGMI0_MDC	IC2_SCL		HPS_GP007
7D	VREFB7A7B7C7D0_HPS	RGMI0_RX_CTL					H6				RGMI0_RX_CTL	USB1_D7		HPS_GP008
7D	VREFB7A7B7C7D0_HPS	RGMI0_TX_CTL					D7				RGMI0_TX_CTL			HPS_GP009
7D	VREFB7A7B7C7D0_HPS	RGMI0_RX_CLK					C9				RGMI0_RX_CLK	USB1_CLK		HPS_GP010
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD1					B7				RGMI0_RXD1	USB1_STP		HPS_GP011
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD2					B8				RGMI0_RXD2	USB1_DIR		HPS_GP012
7D	VREFB7A7B7C7D0_HPS	RGMI0_RXD3					E8				RGMI0_RXD3	USB1_NXT		HPS_GP013
8A	VREFB8A0	IO	CLKp		DIFFIO_RX_T1p	DIFFOUT_T1p	F5							
8A	VREFB8A0	IO	CLKn		DIFFIO_RX_T1n	DIFFOUT_T1n	E5							
8A	VREFB8A0	IO			FPPLL_TL_CLKOUT0/FPPLL_TL_CLKOUT1/FPPLL_TL_CLKOUT2/FPPLL_TL_CLKOUT3	DIFFOUT_T4p	A6							
8A	VREFB8A0	IO			DIFFIO_TL_T1n	DIFFOUT_T4n	A5							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BA	VREFSBAN0	IO	CLK9p,FPLL_TL_FBp		DIFFIO_RX_T9p	DIFFOUT_T9p	C6							
BA	VREFSBAN0	IO	CLK9p,FPLL_TL_FBn		DIFFIO_RX_T9n	DIFFOUT_T9n	C5							
BA		MSEL0		MSEL0			R4							
BA		CONF_DONE		CONF_DONE			A3							
BA		MSEL1		MSEL1			E4							
BA		STATUS		STATUS			B3							
BA		HCE		HCE			A2							
BA		MSEL2		MSEL2			A1							
BA		MSEL3		MSEL3			C4							
BA		KCONFIG		KCONFIG			B2							
BA		MSEL4		MSEL4			C2							
GND							C1							
GND							A14							
GND							A4							
GND							AA14							
GND							AA4							
GND							AB1							
GND							AB11							
GND							AB21							
GND							B1							
GND							B11							
GND							B21							
GND							B6							
GND							C18							
GND							C3							
GND							C8							
GND							D1							
GND							D15							
GND							E1							
GND							E12							
GND							E2							
GND							E22							
GND							E3							
GND							F14							
GND							F19							
GND							F2							
GND							F3							
GND							F4							
GND							F9							
GND							G1							
GND							G16							
GND							G2							
GND							G4							
GND							G5							
GND							G8							
GND							H13							
GND							H2							
GND							H4							
GND							H5							
GND							J10							
GND							J20							
GND							J3							
GND							K							
GND							J7							
GND							K1							
GND							K11							
GND							K13							
GND							K17							
GND							K2							
GND							K4							
GND							K6							
GND							K8							
GND							K9							
GND							L10							
GND							L12							
GND							L14							
GND							L2							
GND							L3							
GND							L5							
GND							L7							
GND							L8							
GND							M1							
GND							M11							
GND							M2							
GND							M21							
GND							M4							
GND							M8							
GND							M9							
GND							N1							
GND							N10							
GND							N12							
GND							N16							
GND							N2							
GND							N3							
GND							N5							
GND							N6							
GND							N7							
GND							N8							
GND							P11							
GND							P15							
GND							P2							
GND							P4							
GND							P6							
GND							P9							
GND							R1							
GND							R12							
GND							R14							
GND							R2							
GND							R22							
GND							R3							
GND							R5							
GND							R7							
GND							R9							
GND							T1							
GND							T13							
GND							T15							
GND							T19							
GND							T2							
GND							T4							
GND							T6							
GND							T8							
GND							U11							
GND							U12							
GND							U13							
GND							U14							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U15							
		GND					U16							
		GND					U17							
		GND					U3							
		GND					U5							
		GND					U6							
		GND					U9							
		GND					V1							
		GND					V13							
		GND					V3							
		GND					V8							
		GND					W10							
		GND					W15							
		GND					W20							
		GND					Y1							
		GND					Y17							
		GND					Y2							
		GND					Y7							
		GND					R16							
		GND					P13							
		VCC					R8							
		VCC					J4							
		VCC					J6							
		VCC					J8							
		VCC					R3							
		VCC					R5							
		VCC					R7							
		VCC					L4							
		VCC					L6							
		VCC					M3							
		VCC					M5							
		VCC					M7							
		VCC					M8							
		VCC					N4							
		VCC					N6							
		VCC					P3							
		VCC					P5							
		VCC					P7							
		VCC					P8							
		VCC					R4							
		VCC					R8							
		VCC					T3							
		VCC					T5							
		VCC					T7							
		VCC					PT7							
		DNU					J2							
		DNU					H1							
		DNU					G17							
		DNU					G8							
		DNU					W2							
		DNU					Y9							
		VCCPGM					Y4							
		VCCPGM					Y18							
		VCCPGM					D4							
		VCCBAT					D2							
		VCCD3A					AB6							
		VCCD3A					W5							
		VCCD3B					AA9							
		VCCD4A					AB18							
		VCCD4A					Y12							
		VCCD6A					Y18							
		VCCD6A					Y22							
		VCCD6A_HPS					Q20							
		VCCD6A_HPS					E17							
		VCCD6A_HPS					G21							
		VCCD6A_HPS					H18							
		VCCD6A_HPS					J15							
		VCCD6A_HPS					K22							
		VCCD6A_HPS					L13							
		VCCD6A_HPS					L19							
		VCCD6B_HPS					M16							
		VCCD6B_HPS					N13							
		VCCD6B_HPS					P20							
		VCCD6B_HPS					R17							
		VCCD6B_HPS					T14							
		VCCD6B_HPS					U21							
		VCCD7A_HPS					A19							
		VCCD7A_HPS					B16							
		VCCD7B_HPS					C13							
		VCCD7B_HPS					G11							
		VCCD7C_HPS					D10							
		VCCD7D_HPS					A9							
		VCCD7D_HPS					E7							
		VCCD8A					D5							
		VCCPD3A					Y6							
		VCCPD3B4A					AA12							
		VCCPD3B4A					V12							
		VCCPD3B4A					V14							
		VCCPD3B4A					W13							
		VCCPD3B4A					W8							
		VCCPD5A					T16							
		VCCPD6AB_HPS					H16							
		VCCPD6AB_HPS					J17							
		VCCPD6AB_HPS					L17							
		VCCPD6AB_HPS					M16							
		VCCPD7A_HPS					G13							
		VCCPD7B_HPS					F12							
		VCCPD7C_HPS					E10							
		VCCPD7D_HPS					C9							
		VCCPD8A					D8							
3A	VREFB3AN0	VREFB3AN0					AB4							
3B	VREFB3BN0	VREFB3BN0					AA10							
4A	VREFB4AN0	VREFB4AN0					AA20							
5A	VREFB5AN0	VREFB5AN0					AB16							
	VREFB7A7B7C7DNO_HPS	VREFB7A7B7C7DNO_HPS					B17							
8A	VREFB8AN0	VREFB8AN0					B5							
		NC					G3							
		NC					H3							
		NC					R10							
		NC					R11							
		NC					T10							
		NC					T11							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		NC					T12							
		NC					T9							
		VCCRSTCLK_HPS					D16							
		RREF_TL					J1							
		VCCA_FPLL					L1							
		VCCA_FPLL					P1							
		VCCA_FPLL					U1							
		VCCA_FPLL					W1							
		VCCA_FPLL					F1							
		VCCA_FPLL					W17							
		VCC_ALIX					AA17							
		VCC_ALIX					AA3							
		VCC_ALIX					D3							
		VCC_ALIX					D9							
		VCC_ALIX					Y10							
		VCC_ALIX_SHARED					E16							
		VCCPLL_HPS					F16							
		VCC_HPS					R13							
		VCC_HPS					R10							
		VCC_HPS					R12							
		VCC_HPS					L11							
		VCC_HPS					L9							
		VCC_HPS					M10							
		VCC_HPS					M12							
		VCC_HPS					N11							
		VCC_HPS					N9							
		VCC_HPS					P10							
		VCC_HPS					P12							

Notes:

- (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).
- (2) HPS\_DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
- (3) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DQS3/DQSBZ (Z)	HMC Pin Assignment for LPDQSBZ	HPS Pin Max Select 3	HPS Pin Max Select 2	HPS Pin Max Select 1	HPS Pin Max Select 0	
3A		TDO		TDO			Y5									
3A		HCS0		DATA4			AA6									
3A		TMS		TMS			AC7									
3A		AS_DATA3		DATA3			AB6									
3A		TKC		TKC			AB5									
3A		AS_DATA2		DATA2			AC5									
3A		TDI		TDI			W10									
3A		AS_DATA1		DATA1			AC6									
3A		DCLK		DCLK			AA8									
3A		AS_DATA0.ASSO		DATA0			AD7									
3A	VREFBAND	ID		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	Y8	DO1B								
3A	VREFBAND	ID		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	V4									
3A	VREFBAND	ID		DATA8	DIFFIO_RX_B1n	DIFFOUT_B1n	V9B	DO1B								
3A	VREFBAND	ID		DATA7	DIFFIO_TX_B2n	DIFFOUT_B2n	Y5	DO1B								
3A	VREFBAND	ID		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	T8	DQS3B1B								
3A	VREFBAND	ID		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB4	DO1B								
3A	VREFBAND	ID		DATA12	DIFFIO_RX_B3n	DIFFOUT_B3n	U9	DQS3B1B								
3A	VREFBAND	ID		DATA11	DIFFIO_TX_B4n	DIFFOUT_B4n	AA4									
3A	VREFBAND	ID		DATA14	DIFFIO_RX_B6n	DIFFOUT_B6n	V10	DO1B								
3A	VREFBAND	ID		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AD4	DO1B								
3A	VREFBAND	ID		CLKUSR	DIFFIO_RX_B5n	DIFFOUT_B5n	U10	DO1B								
3A	VREFBAND	ID		DATA15	DIFFIO_TX_B6n	DIFFOUT_B6n	AC5	DO1B								
3A	VREFBAND	ID		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AA11									
3A	VREFBAND	ID		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AE6	DO1B								
3A	VREFBAND	ID		PR_ERR02C	DIFFIO_RX_B7n	DIFFOUT_B7n	Y11									
3A	VREFBAND	ID			DIFFIO_TX_B8n	DIFFOUT_B8n	AD6	DO1B								
3B	VREFBAND	ID			DIFFIO_TX_B8n	DIFFOUT_B8n	AF4									
3B	VREFBAND	ID			DIFFIO_RX_B10n	DIFFOUT_B10n	AE9	DO2B								
3B	VREFBAND	ID			DIFFIO_TX_B9n	DIFFOUT_B9n	AE4	DO2B								
3B	VREFBAND	ID			DIFFIO_RX_B10n	DIFFOUT_B10n	AD9	DO2B								
3B	VREFBAND	ID			DIFFIO_RX_B11n	DIFFOUT_B11n	U11	DQS2B								
3B	VREFBAND	ID			DIFFIO_TX_B12n	DIFFOUT_B12n	AF8	DO2B								
3B	VREFBAND	ID			DIFFIO_RX_B11n	DIFFOUT_B11n	T11	DQS2B								
3B	VREFBAND	ID			DIFFIO_TX_B12n	DIFFOUT_B12n	AE7									
3B	VREFBAND	ID			DIFFIO_TX_B13n	DIFFOUT_B13n	AF9	DO2B								
3B	VREFBAND	ID			DIFFIO_RX_B14n	DIFFOUT_B14n	AE11	DO2B								
3B	VREFBAND	ID			DIFFIO_TX_B13n	DIFFOUT_B13n	AE8	DO2B								
3B	VREFBAND	ID	CLK0n,FPLL_B1_FBn		DIFFIO_RX_B14n	DIFFOUT_B14n	AD11	DO2B								
3B	VREFBAND	ID			DIFFIO_RX_B15n	DIFFOUT_B15n	W11									
3B	VREFBAND	ID	CLK0n,FPLL_B1_FBn		DIFFIO_TX_B15n	DIFFOUT_B15n	AF5	DO2B								
3B	VREFBAND	ID			DIFFIO_RX_B15n	DIFFOUT_B15n	V11									
3B	VREFBAND	ID			DIFFIO_TX_B16n	DIFFOUT_B16n	AF3	DO2B								
3B	VREFBAND	ID			DIFFIO_TX_B17n	DIFFOUT_B17n	AG5									
3B	VREFBAND	ID			DIFFIO_RX_B18n	DIFFOUT_B18n	AF10	DO3B								
3B	VREFBAND	ID			DIFFIO_TX_B17n	DIFFOUT_B17n	AF7	DO3B								
3B	VREFBAND	ID			DIFFIO_RX_B19n	DIFFOUT_B19n	AF11	DO3B								
3B	VREFBAND	ID			DIFFIO_RX_B19n	DIFFOUT_B19n	T12	DQS3B								
3B	VREFBAND	ID			DIFFIO_TX_B20n	DIFFOUT_B20n	AN3	DO3B								
3B	VREFBAND	ID			DIFFIO_RX_B19n	DIFFOUT_B19n	T13	DQS3B								
3B	VREFBAND	ID			DIFFIO_TX_B20n	DIFFOUT_B20n	AN3	DO3B								
3B	VREFBAND	ID	FPLL_B1_CLKOUT1,FPLL_B1_CLKOUTn		DIFFIO_RX_B20n	DIFFOUT_B20n	AN3	DO3B								
3B	VREFBAND	ID			DIFFIO_TX_B21n	DIFFOUT_B21n	AG5	DO3B								
3B	VREFBAND	ID	FPLL_B1_CLKOUTn,FPLL_B1_CLKOUTn		DIFFIO_RX_B22n	DIFFOUT_B22n	AD12	DO3B								
3B	VREFBAND	ID			DIFFIO_RX_B22n	DIFFOUT_B22n	AD12	DO3B								
3B	VREFBAND	ID			DIFFIO_TX_B23n	DIFFOUT_B23n	W12									
3B	VREFBAND	ID			DIFFIO_RX_B24n	DIFFOUT_B24n	AN5	DO3B								
3B	VREFBAND	ID			DIFFIO_TX_B23n	DIFFOUT_B23n	V13									
3B	VREFBAND	ID	CLK1n		DIFFIO_TX_B24n	DIFFOUT_B24n	AN5	DO3B								
3B	VREFBAND	ID			DIFFIO_RX_B25n	DIFFOUT_B25n	AN7									
4A	VREFBAND	ID	RZQ_0		DIFFIO_RX_B25n	DIFFOUT_B25n	AN7									
4A	VREFBAND	ID			DIFFIO_TX_B26n	DIFFOUT_B26n	AF13	DO4B								
4A	VREFBAND	ID			DIFFIO_TX_B26n	DIFFOUT_B26n	AG8	DO4B								
4A	VREFBAND	ID			DIFFIO_RX_B26n	DIFFOUT_B26n	AG13	DO4B								
4A	VREFBAND	ID			DIFFIO_TX_B27n	DIFFOUT_B27n	U13	DQS4B								
4A	VREFBAND	ID			DIFFIO_TX_B28n	DIFFOUT_B28n	AN8	DO4B								
4A	VREFBAND	ID			DIFFIO_RX_B27n	DIFFOUT_B27n	U14	DQS4B								
4A	VREFBAND	ID			DIFFIO_TX_B28n	DIFFOUT_B28n	AG9									
4A	VREFBAND	ID			DIFFIO_TX_B29n	DIFFOUT_B29n	AN9	DO4B								
4A	VREFBAND	ID			DIFFIO_RX_B30n	DIFFOUT_B30n	AE15	DO4B								
4A	VREFBAND	ID			DIFFIO_TX_B29n	DIFFOUT_B29n	AG10	DO4B								
4A	VREFBAND	ID			DIFFIO_RX_B30n	DIFFOUT_B30n	AF15	DO4B								
4A	VREFBAND	ID	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	AA13									
4A	VREFBAND	ID			DIFFIO_TX_B30n	DIFFOUT_B30n	W11	DO4B								
4A	VREFBAND	ID	CLK2n		DIFFIO_RX_B31n	DIFFOUT_B31n	Y13									
4A	VREFBAND	ID			DIFFIO_TX_B32n	DIFFOUT_B32n	AG11	DO4B								
4A	VREFBAND	ID			DIFFIO_TX_B34n	DIFFOUT_B34n	AG16	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B33n	DIFFOUT_B33n	AH12	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B34n	DIFFOUT_B34n	AF17	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B35n	DIFFOUT_B35n	V15	DQS5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B36n	DIFFOUT_B36n	AH13	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B36n	DIFFOUT_B36n	W14	DQS5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B36n	DIFFOUT_B36n	AG14									
4A	VREFBAND	ID			DIFFIO_TX_B37n	DIFFOUT_B37n	AH14	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B38n	DIFFOUT_B38n	AE17	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B37n	DIFFOUT_B37n	AG15	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B38n	DIFFOUT_B38n	AD17	DO5B	DO1B							
4A	VREFBAND	ID	CLK3n		DIFFIO_RX_B38n	DIFFOUT_B38n	AA15									
4A	VREFBAND	ID			DIFFIO_TX_B40n	DIFFOUT_B40n	AN16	DO5B	DO1B							
4A	VREFBAND	ID	CLK3n		DIFFIO_RX_B39n	DIFFOUT_B39n	V16									
4A	VREFBAND	ID			DIFFIO_TX_B40n	DIFFOUT_B40n	AH17	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B42n	DIFFOUT_B42n	AD19	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B41n	DIFFOUT_B41n	AF18	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B42n	DIFFOUT_B42n	AE19	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B43n	DIFFOUT_B43n	AN18	DQS5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B44n	DIFFOUT_B44n	AN18	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B43n	DIFFOUT_B43n	AN19	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B44n	DIFFOUT_B44n	AG18									
4A	VREFBAND	ID			DIFFIO_TX_B45n	DIFFOUT_B45n	AN19	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B46n	DIFFOUT_B46n	AD20	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B45n	DIFFOUT_B45n	AG19	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B46n	DIFFOUT_B46n	AE20	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B46n	DIFFOUT_B46n	AG20	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_TX_B48n	DIFFOUT_B48n	AF20	DO5B	DO1B							
4A	VREFBAND	ID			DIFFIO_RX_B50n	DIFFOUT_B50n	AF21	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B49n	DIFFOUT_B49n	AG21	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_RX_B50n	DIFFOUT_B50n	AF22	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_RX_B51n	DIFFOUT_B51n	AE22	DQS7B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B52n	DIFFOUT_B52n	AK21	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_RX_B51n	DIFFOUT_B51n	AD23	DQS7B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B53n	DIFFOUT_B53n	AK22	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_RX_B54n	DIFFOUT_B54n	AF23	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B53n	DIFFOUT_B53n	AK23	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B55n	DIFFOUT_B55n	AG24	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B56n	DIFFOUT_B56n	AG24	DO7B	DO2B							
4A	VREFBAND	ID			DIFFIO_RX_B56n	DIFFOUT_B56n	AE23	DO5B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B57n	DIFFOUT_B57n	AG25	DO5B	DO2B							
4A	VREFBAND	ID			DIFFIO_RX_B57n	DIFFOUT_B57n	AE24	DO5B	DO2B							
4A	VREFBAND	ID			DIFFIO_RX_B58n	DIFFOUT_B58n	AC23	DQS5B	DO2B							
4A	VREFBAND	ID			DIFFIO_TX_B59n	DIFFOUT_B59n	AK26	DO5B	DO2B							
4A	VREFBAND	ID														



Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (Z)	HMC Pin Assignment for LPDDR2	HPS Pin Max Select 3	HPS Pin Max Select 2	HPS Pin Max Select 1	HPS Pin Max Select 0
IA	VREFBIAND	IO	RZ0_1		DIFFIO_TX_R0a	DIFFOUT_R0a	AF37	DO3B	DO3B						
IA	VREFBIAND	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AF38	DO1R							
IA	VREFBIAND	IO			INT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AA30							
IA	VREFBIAND	IO			PK_REQUEST	DIFFIO_TX_R3a	DIFFOUT_R3a	AE38	DO1R						
IA	VREFBIAND	IO			CRD_ERROR	DIFFIO_RX_R2p	DIFFOUT_R2p	V19							
IA	VREFBIAND	IO			ICRD	DIFFIO_TX_R3p	DIFFOUT_R3p	AE39	DO1R						
IA	VREFBIAND	IO				DIFFIO_TX_R4p	DIFFOUT_R4p	V11	DO1R						
IA	VREFBIAND	IO			CVF_CONF_DONE	DIFFIO_TX_R3p	DIFFOUT_R3p	AD36	DO1R						
IA	VREFBIAND	IO				DIFFIO_TX_R4a	DIFFOUT_R4a	V18	DG1R						
IA	VREFBIAND	IO			DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC34							
IA	VREFBIAND	IO			DEV_CLKn	DIFFIO_RX_R6p	DIFFOUT_R6p	V16	DQS1R						
IA	VREFBIAND	IO				DIFFIO_TX_R5a	DIFFOUT_R5a	AE33	DO1R						
IA	VREFBIAND	IO				DIFFIO_TX_R6a	DIFFOUT_R6a	V15	DO21R						
IA	VREFBIAND	IO				DIFFIO_TX_R7p	DIFFOUT_R7p	AA34	DO1R						
IA	VREFBIAND	IO				DIFFIO_RX_R6p	DIFFOUT_R6p	V16	DG1R						
IA	VREFBIAND	IO				DIFFIO_TX_R7a	DIFFOUT_R7a	AA33							
IA	VREFBIAND	IO				DIFFIO_RX_R8a	DIFFOUT_R8a	V15	DO1B						
IB	VREFBIAND_HPS	HPS_DDR					AE28		HPS_DM_4	HPS_DM_4					
IB	VREFBIAND_HPS	HPS_DDR					AD28		HPS_DQ_36	HPS_DQ_36					
IB	VREFBIAND_HPS	HPS_DDR					V00		HPS_DQ_37	HPS_DQ_37					
IB	VREFBIAND_HPS	HPS_DDR					AE27		HPS_DQ_38	HPS_DQ_38					
IB	VREFBIAND_HPS	HPS_DDR					V52		HPS_DQ_36	HPS_DQ_36					
IB	VREFBIAND_HPS	HPS_DDR					V18		HPS_DQS_4	HPS_DQS_4					
IB	VREFBIAND_HPS	HPS_GPI3					V24								
IB	VREFBIAND_HPS	HPS_DDR					V17		HPS_DQS4_4	HPS_DQS4_4					
IB	VREFBIAND_HPS	HPS_DDR					V25		HPS_DQ_35	HPS_DQ_35					
IB	VREFBIAND_HPS	HPS_DDR					L25		HPS_DQ_33	HPS_DQ_33					
IB	VREFBIAND_HPS	HPS_DDR					AC28		HPS_DQ_34	HPS_DQ_34					
IB	VREFBIAND_HPS	HPS_DDR					T26		HPS_DQ_32	HPS_DQ_32					
IB	VREFBIAND_HPS	HPS_GPI2					AC27								
IB	VREFBIAND_HPS	HPS_GPI1					U16								
IB	VREFBIAND_HPS	HPS_DDR					AE29		HPS_DM_3	HPS_DM_3					
IB	VREFBIAND_HPS	HPS_GPI0					U15								
IB	VREFBIAND_HPS	HPS_DDR					AA27		HPS_DQ_31	HPS_DQ_31					
IB	VREFBIAND_HPS	HPS_DDR					T24		HPS_DQ_29	HPS_DQ_29					
IB	VREFBIAND_HPS	HPS_DDR					T27		HPS_DQ_30	HPS_DQ_30					
IB	VREFBIAND_HPS	HPS_DDR					R24		HPS_DQ_28	HPS_DQ_28					
IB	VREFBIAND_HPS	VREFBIAND_HPS					T27								
IB	VREFBIAND_HPS	HPS_DDR					V26		HPS_DQS_3	HPS_DQS_3					
IB	VREFBIAND_HPS	HPS_DDR					T20		HPS_DQS4_3	HPS_DQS4_3					
IB	VREFBIAND_HPS	HPS_DDR					V26		HPS_DQ_27	HPS_DQ_27					
IB	VREFBIAND_HPS	HPS_DDR					R25		HPS_DQ_25	HPS_DQ_25					
IB	VREFBIAND_HPS	HPS_DDR					AA28		HPS_DQ_26	HPS_DQ_26					
IB	VREFBIAND_HPS	HPS_DDR					R24		HPS_DQ_24	HPS_DQ_24					
IB	VREFBIAND_HPS	HPS_GPI5					V28								
IB	VREFBIAND_HPS	HPS_GPI7					T16								
IB	VREFBIAND_HPS	HPS_DDR					U28		HPS_DM_2	HPS_DM_2					
IB	VREFBIAND_HPS	HPS_GPI6					T17								
IB	VREFBIAND_HPS	HPS_DDR					V27		HPS_DQ_28	HPS_DQ_28					
IB	VREFBIAND_HPS	HPS_DDR					N27		HPS_DQ_21	HPS_DQ_21					
IB	VREFBIAND_HPS	HPS_DDR					R27		HPS_DQ_22	HPS_DQ_22					
IB	VREFBIAND_HPS	HPS_DDR					N26		HPS_DQ_20	HPS_DQ_20					
IB	VREFBIAND_HPS	HPS_GPI8					F26								
IB	VREFBIAND_HPS	HPS_DDR					T19		HPS_DQS_2	HPS_DQS_2					
IB	VREFBIAND_HPS	HPS_DDR					V28		HPS_RESETn	HPS_RESETn					
IB	VREFBIAND_HPS	HPS_DDR					T18		HPS_DQS2_2	HPS_DQS2_2					
IB	VREFBIAND_HPS	HPS_DDR					U28		HPS_DQ_19	HPS_DQ_19					
IB	VREFBIAND_HPS	HPS_DDR					N25		HPS_DQ_17	HPS_DQ_17					
IB	VREFBIAND_HPS	HPS_DDR					T28		HPS_DQ_18	HPS_DQ_18					
IB	VREFBIAND_HPS	HPS_DDR					N24		HPS_DQ_16	HPS_DQ_16					
IB	VREFBIAND_HPS	HPS_GPI4					R28								
IA	VREFBIAND_HPS	HPS_GPI1					R21								
IA	VREFBIAND_HPS	HPS_DDR					R28		HPS_DM_1	HPS_DM_1					
IA	VREFBIAND_HPS	HPS_GPI2					N28		HPS_DQ_15	HPS_DQ_15					
IA	VREFBIAND_HPS	HPS_DDR					M28		HPS_DQ_13	HPS_DQ_13					
IA	VREFBIAND_HPS	HPS_DDR					M28		HPS_DQ_14	HPS_DQ_14					
IA	VREFBIAND_HPS	HPS_DDR					M27		HPS_DQ_12	HPS_DQ_12					
IA	VREFBIAND_HPS	HPS_DDR					L28		HPS_CKE_0	HPS_CKE_0					
IA	VREFBIAND_HPS	HPS_DDR					R19		HPS_DQS_1	HPS_DQS_1					
IA	VREFBIAND_HPS	HPS_DDR					K28		HPS_CKE_1	HPS_CKE_1					
IA	VREFBIAND_HPS	HPS_DDR					R18		HPS_DQS#_1	HPS_DQS#_1					
IA	VREFBIAND_HPS	HPS_DDR					J28		HPS_DQ_11	HPS_DQ_11					
IA	VREFBIAND_HPS	HPS_DDR					L25		HPS_DQ_9	HPS_DQ_9					
IA	VREFBIAND_HPS	HPS_DDR					J27		HPS_DQ_10	HPS_DQ_10					
IA	VREFBIAND_HPS	HPS_GPI3					K27		HPS_DQ_8	HPS_DQ_8					
IA	VREFBIAND_HPS	HPS_GPI0					M25								
IA	VREFBIAND_HPS	HPS_DDR					G28		HPS_DM_0	HPS_DM_0					
IA	VREFBIAND_HPS	HPS_DDR					F28		HPS_DQ_7	HPS_DQ_7					
IA	VREFBIAND_HPS	HPS_DDR					K26		HPS_DQ_5	HPS_DQ_5					
IA	VREFBIAND_HPS	HPS_DDR					G27		HPS_DQ_6	HPS_DQ_6					
IA	VREFBIAND_HPS	HPS_DDR					J25		HPS_DQ_4	HPS_DQ_4					
IA	VREFBIAND_HPS	HPS_DDR					G26		HPS_ODT_1	HPS_ODT_1					
IA	VREFBIAND_HPS	HPS_DDR					R17		HPS_DQS_0	HPS_DQS_0					
IA	VREFBIAND_HPS	HPS_DDR					D28		HPS_ODT_0	HPS_ODT_0					
IA	VREFBIAND_HPS	HPS_DDR					R16		HPS_DQS#_0	HPS_DQS#_0					
IA	VREFBIAND_HPS	HPS_DDR					D27		HPS_DQ_3	HPS_DQ_3					
IA	VREFBIAND_HPS	HPS_DDR					J24		HPS_DQ_1	HPS_DQ_1					
IA	VREFBIAND_HPS	HPS_DDR					E28		HPS_DQ_2	HPS_DQ_2					
IA	VREFBIAND_HPS	HPS_GPI4					J23								
IA	VREFBIAND_HPS	VREFBIAND_HPS					H28		HPS_DQ_0	HPS_DQ_0					
IA	VREFBIAND_HPS	HPS_DDR					C28		HPS_A_0	HPS_A_0					
IA	VREFBIAND_HPS	HPS_DDR					J21		HPS_A_1	HPS_A_1					
IA	VREFBIAND_HPS	HPS_DDR					J21		HPS_A_4	HPS_A_4					
IA	VREFBIAND_HPS	HPS_DDR					E28		HPS_A_2	HPS_A_2					
IA	VREFBIAND_HPS	HPS_DDR					L25		HPS_A_6	HPS_A_6					
IA	VREFBIAND_HPS	HPS_DDR					D26		HPS_A_3	HPS_A_3					
IA	VREFBIAND_HPS	HPS_DDR					N21		HPS_CK	HPS_CK					
IA	VREFBIAND_HPS	HPS_DDR					C28		HPS_A_6	HPS_A_6					
IA	VREFBIAND_HPS	HPS_DDR					N20		HPS_CK#	HPS_CK#					
IA	VREFBIAND_HPS	HPS_DDR					B28		HPS_A_7	HPS_A_7					
IA	VREFBIAND_HPS	HPS_DDR					H25		HPS_CA_1	HPS_CA_1					
IA	VREFBIAND_HPS	HPS_DDR					A27		HPS_BA_0	HPS_BA_0					
IA	VREFBIAND_HPS	HPS_DDR					G25		HPS_BA_2	HPS_BA_2					
IA	VREFBIAND_HPS	HPS_DDR					A26		HPS_CAS#	HPS_CAS#					
IA	VREFBIAND_HPS	HPS_DDR					A25		HPS_BA5#	HPS_BA5#					
IA	VREFBIAND_HPS	HPS_DDR					F26		HPS_A_8	HPS_A_8					
IA	VREFBIAND_HPS	HPS_DDR					A24		HPS_A_10	HPS_A_10			</		



Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (Z)	HMC Pin Assignment for LPDDR2	HPS Pin Max Select 3	HPS Pin Max Select 2	HPS Pin Max Select 1	HPS Pin Max Select 0
7A		WCSBCLK_HPS					J15								
7A		HPS_TMS					C23								
7A		HPS_TCK					K19								
7A		HPS_TROZ					C23								
7A		HPS_TDI					Q52								
7A		GND					D21								
7A		HPS_PORSEL					E18								
7A		HPS_CLK1					E20								
7A		HPS_CLK2					D20								
7A	VREFE7A7B7C7D9G_HPS	TRACE_CLK					C21					TRACE_CLK			HPS_GPD08
7A	VREFE7A7B7C7D9G_HPS	TRACE_D0					A22					TRACE_D0	SPISO_CLK	LIART0_RX	HPS_GPD09
7A	VREFE7A7B7C7D9G_HPS	TRACE_D1					B21					TRACE_D1	SPISO_MOSI	LIART0_TX	HPS_GPD20
7A	VREFE7A7B7C7D9G_HPS	TRACE_D2					A21					TRACE_D2	SPISO_MISO	IC21_SDA	HPS_GPD01
7A	VREFE7A7B7C7D9G_HPS	TRACE_D3					K18					TRACE_D3	SPISO_SSD	IC21_SCL	HPS_GPD02
7A	VREFE7A7B7C7D9G_HPS	TRACE_D4					A20					TRACE_D4	SPISI_CLK	CANI1_RX	HPS_GPD03
7A	VREFE7A7B7C7D9G_HPS	TRACE_D5					J18					TRACE_D5	SPISI_MOSI	CANI1_TX	HPS_GPD04
7A	VREFE7A7B7C7D9G_HPS	TRACE_D6					A19					TRACE_D6	SPISI_SSD	IC2A_SDA	HPS_GPD05
7A	VREFE7A7B7C7D9G_HPS	TRACE_D7					C18					TRACE_D7	SPISI_MISO	IC2C_SCL	HPS_GPD06
7A	VREFE7A7B7C7D9G_HPS	SPIM0_CLK					A15					SPIM0_CLK	IC21_SDA	LIART0_CTS	HPS_GPD07
7A	VREFE7A7B7C7D9G_HPS	SPIM0_MOSI					C17					SPIM0_MOSI	IC21_SCL	LIART0_RTS	HPS_GPD08
7A	VREFE7A7B7C7D9G_HPS	SPIM0_MISO					B18					SPIM0_MISO	CANI1_RX	LIART0_CTS	HPS_GPD09
7A	VREFE7A7B7C7D9G_HPS	SPIM0_SS0/BOOTSEL0					J17					SPIM0_SS0	CANI1_TX	LIART0_RTS	HPS_GPD08
7A	VREFE7A7B7C7D9G_HPS	LIART0_RX					A17					LIART0_RX	CANI1_RX		HPS_GPD01
7A	VREFE7A7B7C7D9G_HPS	LIART0_TX_CLKSEL1					H17					LIART0_TX	CANI1_TX	LIART0_CTS	HPS_GPD02
7A	VREFE7A7B7C7D9G_HPS	IC2C_SDA					C19					IC2C_SDA	LIART0_RX		HPS_GPD03
7A	VREFE7A7B7C7D9G_HPS	IC2C_SCL					B16					IC2C_SCL	LIART0_TX		HPS_GPD04
7A	VREFE7A7B7C7D9G_HPS	CANI1_RX					B19					CANI1_RX	LIART0_TX	SPIM0_MISO	HPS_GPD05
7A	VREFE7A7B7C7D9G_HPS	CANI1_TX_CLKSEL0					C16					CANI1_TX	LIART0_TX	SPIM0_SS0	HPS_GPD06
7B	VREFE7A7B7C7D9G_HPS	NAND_ALE					J15					NAND_ALE	RGMB1_TX_CLK	QSP1_SS3	HPS_GPD14
7B	VREFE7A7B7C7D9G_HPS	NAND_CE					A16					NAND_CE	RGMB1_TXD0	USBI1_D0	HPS_GPD15
7B	VREFE7A7B7C7D9G_HPS	NAND_CLE					J14					NAND_CLE	RGMB1_TXD1	USBI1_D1	HPS_GPD16
7B	VREFE7A7B7C7D9G_HPS	NAND_RE					A15					NAND_RE	RGMB1_TXD2	USBI1_D2	HPS_GPD17
7B	VREFE7A7B7C7D9G_HPS	NAND_RB					D17					NAND_RB	RGMB1_TXD3	USBI1_D3	HPS_GPD18
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ0					A14					NAND_DQ0	RGMB1_RXD0		HPS_GPD19
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ1					E16					NAND_DQ1	RGMB1_MDO0	IC2C_SDA	HPS_GPD20
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ2					A13					NAND_DQ2	RGMB1_MDC	IC2C_SCL	HPS_GPD21
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ3					J13					NAND_DQ3	RGMB1_RX_CTL	USBI1_D4	HPS_GPD22
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ4					A12					NAND_DQ4	RGMB1_TX_CTL	USBI1_D5	HPS_GPD23
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ5					C12					NAND_DQ5	RGMB1_RX_CLK	USBI1_D6	HPS_GPD24
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ6					A11					NAND_DQ6	RGMB1_RXD1	USBI1_D7	HPS_GPD25
7B	VREFE7A7B7C7D9G_HPS	NAND_DQ7					J12					NAND_DQ7	RGMB1_RXD2		HPS_GPD26
7B	VREFE7A7B7C7D9G_HPS	NAND_WP					A2					NAND_WP	RGMB1_RXD3		HPS_GPD27
7B	VREFE7A7B7C7D9G_HPS	NAND_WE/BOOTSEL2					D15					NAND_WE	QSP1_SS1	QSP1_SS2	HPS_GPD28
7B	VREFE7A7B7C7D9G_HPS	QSP1_I00					A8					QSP1_I00	USBI1_CLK		HPS_GPD29
7B	VREFE7A7B7C7D9G_HPS	QSP1_I01					H16					QSP1_I01	USBI1_STP		HPS_GPD30
7B	VREFE7A7B7C7D9G_HPS	QSP1_I02					A7					QSP1_I02	USBI1_DR		HPS_GPD31
7B	VREFE7A7B7C7D9G_HPS	QSP1_I03					J16					QSP1_I03	USBI1_NXT		HPS_GPD32
7B	VREFE7A7B7C7D9G_HPS	QSP1_SS0/BOOTSEL1					A6					QSP1_SS0			HPS_GPD33
7B	VREFE7A7B7C7D9G_HPS	QSP1_CLK					C14					QSP1_CLK			HPS_GPD34
7B	VREFE7A7B7C7D9G_HPS	QSP1_SS1					B14					QSP1_SS1			HPS_GPD35
7C	VREFE7A7B7C7D9G_HPS	SDMMC_CMD					D14					SDMMC_CMD	USBI1_D0		HPS_GPD36
7C	VREFE7A7B7C7D9G_HPS	SDMMC_PVREN					A5					SDMMC_PVREN	USBI1_D1		HPS_GPD37
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D0					C13					SDMMC_D0	USBI1_D2		HPS_GPD38
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D1					B6					SDMMC_D1	USBI1_D3		HPS_GPD39
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D4					H13					SDMMC_D4	USBI1_D4		HPS_GPD40
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D5					A4					SDMMC_D5	USBI1_D5		HPS_GPD41
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D6					H12					SDMMC_D6	USBI1_D6		HPS_GPD42
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D7					B4					SDMMC_D7	USBI1_D7		HPS_GPD43
7C	VREFE7A7B7C7D9G_HPS	HPS_GPD04					B12					SDMMC_CLK	USBI1_CLK		HPS_GPD44
7C	VREFE7A7B7C7D9G_HPS	SDMMC_CLK_OUT					B8					SDMMC_CLK_OUT	USBI1_STP		HPS_GPD45
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D2					B11					SDMMC_D2	USBI1_DR		HPS_GPD46
7C	VREFE7A7B7C7D9G_HPS	SDMMC_D3					B9					SDMMC_D3	USBI1_NXT		HPS_GPD47
7D	VREFE7A7B7C7D9G_HPS	RGMB1_TX_CLK					E4					RGMB1_TX_CLK			HPS_GPD0
7D	VREFE7A7B7C7D9G_HPS	RGMB1_TXD0					C10					RGMB1_TXD0	USBI1_D0		HPS_GPD1
7D	VREFE7A7B7C7D9G_HPS	RGMB1_TXD1					P5					RGMB1_TXD1	USBI1_D1		HPS_GPD2
7D	VREFE7A7B7C7D9G_HPS	RGMB1_TXD2					C9					RGMB1_TXD2	USBI1_D2		HPS_GPD3
7D	VREFE7A7B7C7D9G_HPS	RGMB1_TXD3					C4					RGMB1_TXD3	USBI1_D3		HPS_GPD4
7D	VREFE7A7B7C7D9G_HPS	RGMB1_RXD0					C8					RGMB1_RXD0	USBI1_D4		HPS_GPD5
7D	VREFE7A7B7C7D9G_HPS	RGMB1_MDO0					C4					RGMB1_MDO0	USBI1_D5	IC2C_SDA	HPS_GPD6
7D	VREFE7A7B7C7D9G_HPS	RGMB1_MDC					C7					RGMB1_MDC	USBI1_D6	IC2C_SCL	HPS_GPD7
7D	VREFE7A7B7C7D9G_HPS	RGMB1_RX_CTL					F4					RGMB1_RX_CTL	USBI1_D7		HPS_GPD8
7D	VREFE7A7B7C7D9G_HPS	RGMB1_TX_CTL					C6					RGMB1_TX_CTL			HPS_GPD9
7D	VREFE7A7B7C7D9G_HPS	RGMB1_RX_CLK					G4					RGMB1_RX_CLK	USBI1_CLK		HPS_GPD10
7D	VREFE7A7B7C7D9G_HPS	RGMB1_RXD1					C5					RGMB1_RXD1	USBI1_STP		HPS_GPD11
7D	VREFE7A7B7C7D9G_HPS	RGMB1_RXD2					F5					RGMB1_RXD2	USBI1_DR		HPS_GPD12
7D	VREFE7A7B7C7D9G_HPS	RGMB1_RXD3					D5					RGMB1_RXD3	USBI1_NXT		HPS_GPD13
8A	VREFE7A7B7C7D9G_HPS	CLK0p					DFFD0_RX_T1p	DFFD0_T1p				D12			
8A	VREFE7A7B7C7D9G_HPS	CLK7n					DFFD0_RX_T7n	DFFD0_T7n				C12			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_TX_T4p	DFFD0_T4p				E8			
8A	VREFE7A7B7C7D9G_HPS						FPLL_TL_CLKOUT0_FPLL_TL_CLKOUTn								
8A	VREFE7A7B7C7D9G_HPS						DFFD0_RX_T8n	DFFD0_T8n				E11			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_RX_T9n	DFFD0_T9n				D11			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_RX_T21p	DFFD0_T21p				L10			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_TX_T22p	DFFD0_T22p				H6			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_RX_T31n	DFFD0_T31n				L8			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_TX_T22n	DFFD0_T22n				H6			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_RX_T23n	DFFD0_T23n				L8			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_RX_T23n	DFFD0_T23n				K8			
8A	VREFE7A7B7C7D9G_HPS						DFFD0_TX_T24n	DFFD0_T24n				H6			
8A		MSEL0		MSEL0								J10			
8A		CONF_DONE		CONF_DONE								J8			
8A		MSEL1		MSEL1								H9			
8A		HSTATUS		HSTATUS								H8			
8A		HCE		HCE								E6			
8A		MSEL2		MSEL2								C6			
8A		MSEL3		MSEL3								K10			
8A		HCONFIG		HCONFIG								F7			
8A		MSEL4		MSEL4								K9			
	GND											F5			
	GND											N8			
	GND											P8			
	GND											F2			
	GND											F1			
	GND											K2			
	GND											K1			
	GND											P2			
	GND											P1			
	GND											V2			
	GND											V1			
	GND											H82			
	GND											AB1			
	GND											AF2			
	GND											AF1			
	GND											V5			
	GND											V4			
	GND											AY0			
	GND											A3			
	GND											AA1			
	GND											AA7			
	GND											AA2			
	GND														





Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (Z)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
		GND					AC1									
		GND					AC2									
		GND					AC3									
		GND					AD14									
		GND					AD22									
		GND					AD25									
		GND					AD3									
		GND					AD6									
		GND					AD8									
		GND					AE1									
		GND					AE16									
		GND					AE18									
		GND					AE2									
		GND					AE3									
		GND					AF24									
		GND					AF3									
		GND					AG1									
		GND					AG17									
		GND					AG2									
		GND					AG27									
		GND					AG3									
		GND					AG7									
		GND					AH10									
		GND					AH20									
		GND					B15									
		GND					B17									
		GND					B20									
		GND					B22									
		GND					B25									
		GND					B27									
		GND					B3									
		GND					B5									
		GND					B7									
		GND					C1									
		GND					C11									
		GND					C2									
		GND					C3									
		GND					D10									
		GND					D15									
		GND					D16									
		GND					D3									
		GND					E1									
		GND					E19									
		GND					E2									
		GND					E22									
		GND					E24									
		GND					E27									
		GND					E3									
		GND					E9									
		GND					F3									
		GND					G1									
		GND					G2									
		GND					G3									
		GND					H11									
		GND					H15									
		GND					H18									
		GND					H20									
		GND					H24									
		GND					H27									
		GND					H3									
		GND					V3									
		GND					V25									
		GND					V28									
		GND					J1									
		GND					J2									
		GND					J3									
		GND					J5									
		GND					J9									
		GND					K11									
		GND					K12									
		GND					K14									
		GND					K16									
		GND					K20									
		GND					K3									
		GND					K4									
		GND					Y14									
		GND					L1									
		GND					Y12									
		GND					L3									
		GND					L15									
		GND					L17									
		GND					L19									
		GND					L2									
		GND					L24									
		GND					L27									
		GND					L3									
		GND					L5									
		GND					W4									
		GND					Q3									
		GND					M19									
		GND					M11									
		GND					M14									
		GND					M16									
		GND					M20									
		GND					M3									
		GND					M5									
		GND					N1									
		GND					N13									
		GND					N15									
		GND					N17									
		GND					N19									
		GND					N2									
		GND					N3									
		GND					N4									
		GND					P10									
		GND					P12									
		GND					P15									
		GND					P18									
		GND					P20									
		GND					P25									
		GND					P3									
		GND					P5									
		GND					P9									
		GND					R1									
		GND					R11									
		GND					R13									
		GND					R15									
		GND					R2									
		GND					R3									
		GND					R8									
		GND					T10									
		GND					T14									
		GND					T3									
		GND					U1									
		GND					U2									



Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (Z)	HMC Pin Assignment for LPDDR2	HPS Pin Max Select 3	HPS Pin Max Select 2	HPS Pin Max Select 1	HPS Pin Max Select 0
		GND					U17								
		GND					U2								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U3								
		GND					U8								
		GND					V14								
		GND					V3								
		GND					V8								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W18								
		GND					W2								
		GND					W25								
		GND					W24								
		GND					Y24								
		GND					Y26								
		GND					W20								
		GND					AB26								
		GND					W21								
		GND					V26								
		GND					V21								
		VCC					L11								
		VCC					K13								
		VCC					K15								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M16								
		VCC					M8								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N6								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P15								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T13								
		VCC					T9								
		VCC					L4								
		VCC					T4								
		VCC					M5								
		VCC					N5								
		VCC					R5								
		VCC					T5								
		VCC					U26								
		DNV					A2								
		DNV					B2								
		DNV					D1								
		DNV					D2								
		DNV					H1								
		DNV					H2								
		DNV					M1								
		DNV					M2								
		DNV					T1								
		DNV					T2								
		DNV					Y1								
		DNV					Y2								
		DNV					AD1								
		DNV					AD2								
		DNV					D23								
		DNV					E12								
		DNV					U8								
		DNV					AE14								
		VCCP6M					Y10								
		VCCP6M					AD24								
		VCCP6M					H10								
		VCCBAT					D7								
		VCCIO3A					AA5								
		VCCIO3A					W9								
		VCCIO3B					AA12								
		VCCIO3B					AE10								
		VCCIO3B					AE13								
		VCCIO3B					AE4								
		VCCIO3A					AA16								
		VCCIO3A					AE21								
		VCCIO3A					AF14								
		VCCIO3A					AF19								
		VCCIO3A					AG12								
		VCCIO3A					AG22								
		VCCIO3A					AH15								
		VCCIO3A					AH25								
		VCCIO3A					W13								
		VCCIO3A					AC26								
		VCCIO3A					W17								
		VCCIO3A HPS					C25								
		VCCIO3A HPS					C27								
		VCCIO3A HPS					C37								
		VCCIO3A HPS					G24								
		VCCIO3A HPS					H21								
		VCCIO3A HPS					H26								
		VCCIO3A HPS					L26								
		VCCIO3A HPS					M21								
		VCCIO3B HPS					AD27								
		VCCIO3B HPS					P27								
		VCCIO3B HPS					T21								
		VCCIO3B HPS					T25								
		VCCIO3B HPS					U18								
		VCCIO3B HPS					W27								
		VCCIO7A HPS					C20								
		VCCIO7A HPS					D18								
		VCCIO7B HPS					B13								
		VCCIO7B HPS					H14								
		VCCIO7C HPS					B10								
		VCCIO7D HPS					D6								
		VCCIO7D HPS					G5								
		VCCIO8A					E7								
		VCCPD3A					AA10								
		VCCPD3A4					AA14								
		VCCPD3B4					AD13								
		VCCPD3B4					AD16								
		VCCPD3B4					AD18								
		VCCPD3B4					AD21								
		VCCPD3B4					AD9								
		VCCPD3A					V21								



Bank Number	VREF	PinName/Function (Z)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (Z)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		WCPC06A0B_HPS					K21								
		WCPC06A0B_HPS					K24								
		WCPC06A0B_HPS					M24								
		WCPC06A0B_HPS					P21								
		WCPC06A0B_HPS					P24								
		WCPC07A_HPS					E21								
		WCPC07B_HPS					E17								
		WCPC07C_HPS					E14								
		WCPC07D_HPS					E13								
		WCPC08A					E10								
3A	VREFB3AND	VREFB3AND					AE5								
3B	VREFB3BND	VREFB3BND					AF12								
4A	VREFB4AND	VREFB4AND					AF16								
5A	VREFB5AND	VREFB5AND					AC26								
		VREFB7A7B7C7DND_HPS					D19								
8A	VREFB8AND	VREFB8AND					D9								
		NC					W25								
		NC					AA25								
		NC					W19								
		WCRCSTCLK_HPS					F22								
		RREF_TL					B1								
		VCCA_FPLL					K5								
		VCCA_FPLL					P4								
		VCCA_FPLL					U4								
		VCCA_FPLL					W5								
		VCCA_FPLL					J6								
		VCCA_FPLL					AA21								
		VCCA_FPLL					M6								
		VCCA_FPLL					R4								
		VCC_ALIX					AC21								
		VCC_ALIX					AC8								
		VCC_ALIX					AD15								
		VCC_ALIX					E16								
		VCC_ALIX					F8								
		VCC_ALIX_SHARED					F21								
		WCPLL_HPS					K23								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M18								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N18								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).  
 (2) HPS, DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.  
 (3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSEBA4 Device  
Version 1.3

Version Number	Date	Changes Made
1.0	7/8/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	1/4/2016	Removed the USB0 pin from Pin List U19.
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.