Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		DNU					E33				
		DNU					F33				
		RREF_TL					F34				
GXB_L1		REFCLK3Ln					R27				
GXB_L1		REFCLK3Lp					R26				
GXB_L1		GXB_TX_L11n					G31				
GXB_L1		GXB_TX_L11p					G32				
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					H34				
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					H33				
GXB_L1		GXB_TX_L10n					J31				
GXB_L1		GXB_TX_L10p					J32				
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					K34				
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					K33				
GXB_L1		GXB_TX_L9n					L31				
GXB_L1		GXB_TX_L9p					L32				
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					M34				
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					M33				
GXB_L1		GXB_TX_L8n					N31				
GXB_L1		GXB_TX_L8p					N32				
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					P34				
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					P33				
GXB_L1		GXB_TX_L7n					R31				
GXB_L1		GXB_TX_L7p					R32				
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					T34				
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					T33				
GXB_L1		GXB_TX_L6n					U31				
GXB_L1		GXB_TX_L6p					U32				
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					V34				
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					V33				
GXB_L1		REFCLK2Ln					U27				
GXB_L1		REFCLK2Lp					U26				
GXB_L0		REFCLK1Ln					W27				
GXB_L0		REFCLK1Lp					W26				
GXB_L0		GXB_TX_L5n					W31				
GXB_L0		GXB_TX_L5p					W32				
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					Y34				
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					Y33				
GXB_L0		GXB_TX_L4n					AA31				
GXB_L0		GXB_TX_L4p					AA32				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AB34				
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AB33				
GXB_L0		GXB_TX_L3n					AC31				
GXB_L0		GXB_TX_L3p					AC32				
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AD34				
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AD33				
GXB_L0		GXB_TX_L2n					AE31				
GXB_L0		GXB_TX_L2p					AE32				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AF34				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AF33				
GXB_L0		GXB_TX_L1n					AG31				
GXB_L0		GXB_TX_L1p					AG32				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AH34				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AH33				
GXB_L0		GXB_TX_L0n					AJ31				
GXB_L0		GXB_TX_L0p					AJ32				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AK34				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AK33				
GXB_L0		REFCLK0Ln					AA28				
GXB_L0		REFCLK0Lp					AA27				
		DNU					AL32				
3A		TDO		TDO			AC28				
3A		TMS		TMS			AF30				
3A		TCK		TCK			AN32				
3A		TDI		TDI			AC29				
3A		DCLK		DCLK			AM32				
3A		nCSO		DATA4			AM34				
3A		AS_DATA3		DATA3			AM33				
3A		AS_DATA2		DATA2			AP33				
3A		AS_DATA1		DATA1			AN33				
3A		AS_DATA0,ASDO		DATA0			AN34				
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AL31				
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AM31	DQ1B			
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AP31	DQ1B			
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AP32	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	AD27				
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AD26	DQ1B			
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AJ29	DQSn1B/QK1B			
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AK29	DQS1B/CQ1B/CQn1B/QKn1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AL30				
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AM30	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AN30	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AP30	DQ1B			
3A	VREFB3AN0	IO	VREFB3AN0				AE27				
3A	VREFB3AN0	IO					AF28	DQ1B			
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AH28	DQ1B			
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AJ28	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AL29				CS#_3A_1
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AM29	DQ2B	DQ1B		CS#_3A_0
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AN29	DQ2B	DQ1B		
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AP29	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AE29				ODT_3A_1
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AF29	DQ2B	DQ1B		ODT_3A_0
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AG27	DQSn2B/QK2B	DQ1B		WE#_3A
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AH27	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B		CAS#_3A
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AL28				RAS#_3A
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AM28	DQ2B	DQ1B		BA_3A_2
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AP27	DQ2B	DQ1B		BA_3A_1
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AP28	DQ2B	DQ1B		BA_3A_0
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AG29				A_3A_15

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Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AH29	DQ2B	DQ1B		A_3A_14
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AK27	DQ2B	DQ1B		A_3A_13
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AL27	DQ2B	DQ1B		A_3A_12
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AG26				A_3A_11
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AH26	DQ3B	DQ1B		A_3A_10
3A	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AJ26	DQ3B	DQ1B		A_3A_9
3A	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AK26	DQ3B	DQ1B		A_3A_8
3A	VREFB3AN0	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AD29				A_3A_7
3A	VREFB3AN0	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AE28	DQ3B	DQ1B		A_3A_6
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AL26	DQSn3B/QK3B	DQSn1B/QK1B		A_3A_5
3A	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AM26	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/CQ1B/CQn1B/QKn1B		A_3A_4
3A	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AN27				A_3A_3
3A	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AN26	DQ3B	DQ1B		A_3A_2
3A	VREFB3AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AP25	DQ3B	DQ1B		A_3A_1
3A	VREFB3AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AP26	DQ3B	DQ1B		A_3A_0
3A	VREFB3AN0	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AE26				CKE_3A_1
3A	VREFB3AN0	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AF26	DQ3B	DQ1B		CKE_3A_0
3A	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AL25	DQ3B	DQ1B		CK#_3A
3A	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AM25	DQ3B	DQ1B		CK_3A
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AE23				RESET#_3A
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AE24	DQ4B	DQ2B	DQ1B	DQ1_3B_8
3B	VREFB3BN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AC24	DQ4B	DQ2B	DQ1B	DQ1_3B_7
3B	VREFB3BN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AC25	DQ4B	DQ2B	DQ1B	DQ1_3B_6
3B	VREFB3BN0	IO			DIFFIO_TX_B26n	DIFFOUT_B26n	AA25				
3B	VREFB3BN0	IO			DIFFIO_TX_B26p	DIFFOUT_B26p	AB25	DQ4B	DQ2B	DQ1B	DM1_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AD24	DQSn4B/QK4B	DQ2B	DQ1B	DQS#1_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AE25	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	DQ1B	DQS1_3B
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AF25				
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AG24	DQ4B	DQ2B	DQ1B	DQ1_3B_5
3B	VREFB3BN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AH24	DQ4B	DQ2B	DQ1B	DQ1_3B_4
3B	VREFB3BN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AH25	DQ4B	DQ2B	DQ1B	DQ1_3B_3
3B	VREFB3BN0	IO	VREFB3BN0				Y23				
3B	VREFB3BN0	IO					AB24	DQ4B	DQ2B	DQ1B	DQ1_3B_2
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AJ25	DQ4B	DQ2B	DQ1B	DQ1_3B_1
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AK24	DQ4B	DQ2B	DQ1B	DQ1_3B_0
3B	VREFB3BN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AK23				
3B	VREFB3BN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AL24	DQ5B	DQ2B	DQ1B	DQ2_3B_8
3B	VREFB3BN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AF23	DQ5B	DQ2B	DQ1B	DQ2_3B_7
3B	VREFB3BN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AG23	DQ5B	DQ2B	DQ1B	DQ2_3B_6
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AC23				
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AD23	DQ5B	DQ2B	DQ1B	DM2_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AH23	DQSn5B/QK5B	DQSn2B/QK2B	DQ1B	DQS#2_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AJ23	DQS5B/CQ5B/CQn5B/QKn5B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	DQS2_3B
3B	VREFB3BN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AL23				
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AM23	DQ5B	DQ2B	DQ1B	DQ2_3B_5
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AN23	DQ5B	DQ2B	DQ1B	DQ2_3B_4
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AN24	DQ5B	DQ2B	DQ1B	DQ2_3B_3
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA23				
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB23	DQ5B	DQ2B	DQ1B	DQ2_3B_2
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AP22	DQ5B	DQ2B	DQ1B	DQ2_3B_1
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AP23	DQ5B	DQ2B	DQ1B	DQ2_3B_0
3C	VREFB3CN0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AE21				
3C	VREFB3CN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AE22	DQ6B	DQ3B	DQ1B	DQ3_3C_8
3C	VREFB3CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AL21	DQ6B	DQ3B	DQ1B	DQ3_3C_7
3C	VREFB3CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AL22	DQ6B	DQ3B	DQ1B	DQ3_3C_6
3C	VREFB3CN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22				
3C	VREFB3CN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AC22	DQ6B	DQ3B	DQ1B	DM3_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AH21	DQSn6B/QK6B	DQ3B	DQSn1B/QK1B	DQS#3_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AH22	DQS6B/CQ6B/CQn6B/QKn6B	DQ3B	DQS1B/CQ1B/CQn1B/QKn1B	DQS3_3C
3C	VREFB3CN0	IO			DIFFIO_TX_B43n	DIFFOUT_B43n	AF22				
3C	VREFB3CN0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AG21	DQ6B	DQ3B	DQ1B	DQ3_3C_5
3C	VREFB3CN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AJ22	DQ6B	DQ3B	DQ1B	DQ3_3C_4
3C	VREFB3CN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AK21	DQ6B	DQ3B	DQ1B	DQ3_3C_3
3C	VREFB3CN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AA21				
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AB21	DQ6B	DQ3B	DQ1B	DQ3_3C_2
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AM22	DQ6B	DQ3B	DQ1B	DQ3_3C_1
3C	VREFB3CN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AN21	DQ6B	DQ3B	DQ1B	DQ3_3C_0
3C	VREFB3CN0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	AC21				
3C	VREFB3CN0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AD21	DQ7B	DQ3B	DQ1B	DQ4_3C_8
3C	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AN20	DQ7B	DQ3B	DQ1B	DQ4_3C_7
3C	VREFB3CN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AP20	DQ7B	DQ3B	DQ1B	DQ4_3C_6
3C	VREFB3CN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AA20				
3C	VREFB3CN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB20	DQ7B	DQ3B	DQ1B	DM4_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AL20	DQSn7B/QK7B	DQSn3B/QK3B	DQ1B	DQS#4_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AM20	DQS7B/CQ7B/CQn7B/QKn7B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	DQS4_3C
3C	VREFB3CN0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AJ20				
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AK20	DQ7B	DQ3B	DQ1B	DQ4_3C_5
3C	VREFB3CN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AG20	DQ7B	DQ3B	DQ1B	DQ4_3C_4
3C	VREFB3CN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AH20	DQ7B	DQ3B	DQ1B	DQ4_3C_3
3C	VREFB3CN0	IO	VREFB3CN0				AC20				
3C	VREFB3CN0	IO					AD20	DQ7B	DQ3B	DQ1B	DQ4_3C_2
3C	VREFB3CN0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AE20	DQ7B	DQ3B	DQ1B	DQ4_3C_1
3C	VREFB3CN0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AF20	DQ7B	DQ3B	DQ1B	DQ4_3C_0
3D	VREFB3DN0	IO			DIFFIO_TX_B70n	DIFFOUT_B70n	AH19				
3D	VREFB3DN0	IO			DIFFIO_TX_B70p	DIFFOUT_B70p	AJ19	DQ8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AL19	DQ8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AM19	DQ8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AB19				
3D	VREFB3DN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AC19	DQ8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_RX_B73n	DIFFOUT_B73n	AN18	DQSn8B/QK8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_RX_B73p	DIFFOUT_B73p	AP19	DQS8B/CQ8B/CQn8B/QKn8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_TX_B74n	DIFFOUT_B74n	AE19				
3D	VREFB3DN0	IO			DIFFIO_TX_B74p	DIFFOUT_B74p	AF19	DQ8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AK18	DQ8B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AL18	DQ8B	DQ4B		
3D	VREFB3DN0	IO	VREFB3DN0				AB18				
3D	VREFB3DN0	IO					AA18	DQ8B	DQ4B		
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AG18	DQ8B	DQ4B		
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AH18	DQ8B	DQ4B		

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Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
3D	VREFB3DN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AN17				
3D	VREFB3DN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AP17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AG17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AH17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B79n	DIFFOUT_B79n	AA17				
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B79p	DIFFOUT_B79p	AB17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B80n	DIFFOUT_B80n	AJ17	DQSn9B/QK9B	DQSn4B/QK4B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B80p	DIFFOUT_B80p	AK17	DQS9B/CQ9B/CQn9B/QKn9B	DQS4B/CQ4B/CQn4B/QKn4B		
3D	VREFB3DN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AL17				
3D	VREFB3DN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AM17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AE17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AF17	DQ9B	DQ4B		
3D	VREFB3DN0	IO			DIFFIO_TX_B83n	DIFFOUT_B83n	AC17				
3D	VREFB3DN0	IO			DIFFIO_TX_B83p	DIFFOUT_B83p	AC18	DQ9B	DQ4B		
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AD17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AE18	DQ9B	DQ4B		
		VCCD_FPLL					Y17				
		VCCA_FPLL					Y18				
		DNU					AD18				
4D	VREFB4DN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AP16				CS#_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AN15	DQ10B	DQ5B		CS#_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AH16	DQ10B	DQ5B		
4D	VREFB4DN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AJ16	DQ10B	DQ5B		A_4D_15
4D	VREFB4DN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AE16				ODT_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AF16	DQ10B	DQ5B		ODT_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	Y15	DQSn10B/QK10B	DQ5B		WE#_4D
4D	VREFB4DN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AA15	DQS10B/CQ10B/CQn10B/QKn10B	DQ5B		CAS#_4D
4D	VREFB4DN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AB16				RAS#_4D
4D	VREFB4DN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	AC16	DQ10B	DQ5B		BA_4D_2
4D	VREFB4DN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AL16	DQ10B	DQ5B		BA_4D_1
4D	VREFB4DN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AM16	DQ10B	DQ5B		BA_4D_0
4D	VREFB4DN0	IO	VREFB4DN0				AJ14				
4D	VREFB4DN0	IO					AK14	DQ10B	DQ5B		A_4D_14
4D	VREFB4DN0	IO			DIFFIO_RX_B99n	DIFFOUT_B99n	AL14	DQ10B	DQ5B		A_4D_13
4D	VREFB4DN0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AM14	DQ10B	DQ5B		A_4D_12
4D	VREFB4DN0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	AA14				A_4D_11
4D	VREFB4DN0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AB15	DQ11B	DQ5B		A_4D_10
4D	VREFB4DN0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	AK15	DQ11B	DQ5B		A_4D_9
4D	VREFB4DN0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AL15	DQ11B	DQ5B		A_4D_8
4D	VREFB4DN0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	AG14				A_4D_7
4D	VREFB4DN0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AH14	DQ11B	DQ5B		A_4D_6
4D	VREFB4DN0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AG15	DQSn11B/QK11B	DQSn5B/QK5B		A_4D_5
4D	VREFB4DN0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AH15	DQS11B/CQ11B/CQn11B/QKn11B	DQS5B/CQ5B/CQn5B/QKn5B		A_4D_4
4D	VREFB4DN0	IO			DIFFIO_TX_B104n	DIFFOUT_B104n	AD15				A_4D_3
4D	VREFB4DN0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AE15	DQ11B	DQ5B		A_4D_2
4D	VREFB4DN0	IO			DIFFIO_RX_B105n	DIFFOUT_B105n	AE14	DQ11B	DQ5B		A_4D_1
4D	VREFB4DN0	IO			DIFFIO_RX_B105p	DIFFOUT_B105p	AF14	DQ11B	DQ5B		A_4D_0
4D	VREFB4DN0	IO			DIFFIO_TX_B106n	DIFFOUT_B106n	AB14				CKE_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B106p	DIFFOUT_B106p	AC15	DQ11B	DQ5B		CKE_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B107n	DIFFOUT_B107n	AC14	DQ11B	DQ5B		CK#_4D
4D	VREFB4DN0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AD14	DQ11B	DQ5B		CK_4D
4C	VREFB4CN0	IO			DIFFIO_TX_B108n	DIFFOUT_B108n	AB13				RESET#_4D
4C	VREFB4CN0	IO			DIFFIO_TX_B108p	DIFFOUT_B108p	AC13	DQ12B	DQ6B	DQ2B	DQ1_4C_8
4C	VREFB4CN0	IO			DIFFIO_RX_B109n	DIFFOUT_B109n	AN14	DQ12B	DQ6B	DQ2B	DQ1_4C_7
4C	VREFB4CN0	IO			DIFFIO_RX_B109p	DIFFOUT_B109p	AP14	DQ12B	DQ6B	DQ2B	DQ1_4C_6
4C	VREFB4CN0	IO			DIFFIO_TX_B110n	DIFFOUT_B110n	AN12				
4C	VREFB4CN0	IO			DIFFIO_TX_B110p	DIFFOUT_B110p	AP13	DQ12B	DQ6B	DQ2B	DM1_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B111n	DIFFOUT_B111n	AL13	DQSn12B/QK12B	DQ6B	DQ2B	DQS#1_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B111p	DIFFOUT_B111p	AM13	DQS12B/CQ12B/CQn12B/QKn12B	DQ6B	DQ2B	DQS1_4C
4C	VREFB4CN0	IO			DIFFIO_TX_B112n	DIFFOUT_B112n	Y11				
4C	VREFB4CN0	IO			DIFFIO_TX_B112p	DIFFOUT_B112p	AA12	DQ12B	DQ6B	DQ2B	DQ1_4C_5
4C	VREFB4CN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AK12	DQ12B	DQ6B	DQ2B	DQ1_4C_4
4C	VREFB4CN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AL12	DQ12B	DQ6B	DQ2B	DQ1_4C_3
4C	VREFB4CN0	IO	VREFB4CN0				AK11				
4C	VREFB4CN0	IO					AL11	DQ12B	DQ6B	DQ2B	DQ1_4C_2
4C	VREFB4CN0	IO			DIFFIO_RX_B114n	DIFFOUT_B114n	AH13	DQ12B	DQ6B	DQ2B	DQ1_4C_1
4C	VREFB4CN0	IO			DIFFIO_RX_B114p	DIFFOUT_B114p	AJ13	DQ12B	DQ6B	DQ2B	DQ1_4C_0
4C	VREFB4CN0	IO			DIFFIO_TX_B115n	DIFFOUT_B115n	AB11				
4C	VREFB4CN0	IO			DIFFIO_TX_B115p	DIFFOUT_B115p	AB12	DQ13B	DQ6B	DQ2B	DQ2_4C_8
4C	VREFB4CN0	IO			DIFFIO_RX_B116n	DIFFOUT_B116n	AG12	DQ13B	DQ6B	DQ2B	DQ2_4C_7
4C	VREFB4CN0	IO			DIFFIO_RX_B116p	DIFFOUT_B116p	AH12	DQ13B	DQ6B	DQ2B	DQ2_4C_6
4C	VREFB4CN0	IO			DIFFIO_TX_B117n	DIFFOUT_B117n	AH11				
4C	VREFB4CN0	IO			DIFFIO_TX_B117p	DIFFOUT_B117p	AJ11	DQ13B	DQ6B	DQ2B	DM2_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B118n	DIFFOUT_B118n	AE13	DQSn13B/QK13B	DQSn6B/QK6B	DQ2B	DQS#2_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B118p	DIFFOUT_B118p	AF13	DQS13B/CQ13B/CQn13B/QKn13B	DQS6B/CQ6B/CQn6B/QKn6B	DQ2B	DQS2_4C
4C	VREFB4CN0	IO			DIFFIO_TX_B119n	DIFFOUT_B119n	AC11				
4C	VREFB4CN0	IO			DIFFIO_TX_B119p	DIFFOUT_B119p	AC12	DQ13B	DQ6B	DQ2B	DQ2_4C_5
4C	VREFB4CN0	IO			DIFFIO_RX_B120n	DIFFOUT_B120n	AD12	DQ13B	DQ6B	DQ2B	DQ2_4C_4
4C	VREFB4CN0	IO			DIFFIO_RX_B120p	DIFFOUT_B120p	AE12	DQ13B	DQ6B	DQ2B	DQ2_4C_3
4C	VREFB4CN0	IO			DIFFIO_TX_B121n	DIFFOUT_B121n	AD11				
4C	VREFB4CN0	IO			DIFFIO_TX_B121p	DIFFOUT_B121p	AE11	DQ13B	DQ6B	DQ2B	DQ2_4C_2
4C	VREFB4CN0	IO			DIFFIO_RX_B122n	DIFFOUT_B122n	AF11	DQ13B	DQ6B	DQ2B	DQ2_4C_1
4C	VREFB4CN0	IO			DIFFIO_RX_B122p	DIFFOUT_B122p	AG11	DQ13B	DQ6B	DQ2B	DQ2_4C_0
4B	VREFB4BN0	IO			DIFFIO_TX_B123n	DIFFOUT_B123n	AD9				
4B	VREFB4BN0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AE9	DQ14B	DQ7B	DQ2B	DQ3_4B_8
4B	VREFB4BN0	IO			DIFFIO_RX_B124n	DIFFOUT_B124n	AM11	DQ14B	DQ7B	DQ2B	DQ3_4B_7
4B	VREFB4BN0	IO			DIFFIO_RX_B124p	DIFFOUT_B124p	AN11	DQ14B	DQ7B	DQ2B	DQ3_4B_6
4B	VREFB4BN0	IO			DIFFIO_TX_B125n	DIFFOUT_B125n	AL10				
4B	VREFB4BN0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AM10	DQ14B	DQ7B	DQ2B	DM3_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B126n	DIFFOUT_B126n	AP10	DQSn14B/QK14B	DQ7B	DQSn2B/QK2B	DQS#3_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B126p	DIFFOUT_B126p	AP11	DQS14B/CQ14B/CQn14B/QKn14B	DQ7B	DQS2B/CQ2B/CQn2B/QKn2B	DQS3_4B
4B	VREFB4BN0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	AA10				
4B	VREFB4BN0	IO			DIFFIO_TX_B127p	DIFFOUT_B127p	AB10	DQ14B	DQ7B	DQ2B	DQ3_4B_5
4B	VREFB4BN0	IO			DIFFIO_RX_B128n	DIFFOUT_B128n	AH10	DQ14B	DQ7B	DQ2B	DQ3_4B_4
4B	VREFB4BN0	IO			DIFFIO_RX_B128p	DIFFOUT_B128p	AJ10	DQ14B	DQ7B	DQ2B	DQ3_4B_3
4B	VREFB4BN0	IO			DIFFIO_TX_B129n	DIFFOUT_B129n	AK9				
4B	VREFB4BN0	IO			DIFFIO_TX_B129p	DIFFOUT_B129p	AL9	DQ14B	DQ7B	DQ2B	DQ3_4B_2
4B	VREFB4BN0	IO			DIFFIO_RX_B130n	DIFFOUT_B130n	AN9	DQ14B	DQ7B	DQ2B	DQ3_4B_1
4B	VREFB4BN0	IO			DIFFIO_RX_B130p	DIFFOUT_B130p	AN8	DQ14B	DQ7B	DQ2B	DQ3_4B_0

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Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
4B	VREFB4BN0	IO			DIFFIO_TX_B131n	DIFFOUT_B131n	AC9				
4B	VREFB4BN0	IO			DIFFIO_TX_B131p	DIFFOUT_B131p	AC10	DQ15B	DQ7B	DQ2B	DQ4_4B_8
4B	VREFB4BN0	IO			DIFFIO_RX_B132n	DIFFOUT_B132n	AG9	DQ15B	DQ7B	DQ2B	DQ4_4B_7
4B	VREFB4BN0	IO			DIFFIO_RX_B132p	DIFFOUT_B132p	AH9	DQ15B	DQ7B	DQ2B	DQ4_4B_6
4B	VREFB4BN0	IO			DIFFIO_TX_B133n	DIFFOUT_B133n	AE10				
4B	VREFB4BN0	IO			DIFFIO_TX_B133p	DIFFOUT_B133p	AF10	DQ15B	DQ7B	DQ2B	DM4_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B134n	DIFFOUT_B134n	AL8	DQSn15B/QK15B	DQSn7B/QK7B	DQ2B	DQS#4_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B134p	DIFFOUT_B134p	AM8	DQS15B/CQ15B/CQn15B/QKn15B	DQS7B/CQ7B/CQn7B/QKn7B	DQ2B	DQS4_4B
4B	VREFB4BN0	IO			DIFFIO_TX_B135n	DIFFOUT_B135n	AC8				
4B	VREFB4BN0	IO			DIFFIO_TX_B135p	DIFFOUT_B135p	AD8	DQ15B	DQ7B	DQ2B	DQ4_4B_5
4B	VREFB4BN0	IO			DIFFIO_RX_B136n	DIFFOUT_B136n	AJ8	DQ15B	DQ7B	DQ2B	DQ4_4B_4
4B	VREFB4BN0	IO			DIFFIO_RX_B136p	DIFFOUT_B136p	AK8	DQ15B	DQ7B	DQ2B	DQ4_4B_3
4B	VREFB4BN0	IO	VREFB4BN0				AE8				
4B	VREFB4BN0	IO					AF8	DQ15B	DQ7B	DQ2B	DQ4_4B_2
4B	VREFB4BN0	IO			DIFFIO_RX_B137n	DIFFOUT_B137n	AG8	DQ15B	DQ7B	DQ2B	DQ4_4B_1
4B	VREFB4BN0	IO			DIFFIO_RX_B137p	DIFFOUT_B137p	AH8	DQ15B	DQ7B	DQ2B	DQ4_4B_0
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B154n	DIFFOUT_B154n	AP8				
4A	VREFB4AN0	IO		DATA11	DIFFIO_TX_B154p	DIFFOUT_B154p	AP7	DQ16B	DQ8B		
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B155n	DIFFOUT_B155n	AL7	DQ16B	DQ8B		
4A	VREFB4AN0	IO		DATA6	DIFFIO_RX_B155p	DIFFOUT_B155p	AM7	DQ16B	DQ8B		
4A	VREFB4AN0	IO		DATA12	DIFFIO_TX_B156n	DIFFOUT_B156n	AM6				
4A	VREFB4AN0	IO		DATA13	DIFFIO_TX_B156p	DIFFOUT_B156p	AN6	DQ16B	DQ8B		
4A	VREFB4AN0	IO		DATA7	DIFFIO_RX_B157n	DIFFOUT_B157n	AP6	DQSn16B/QK16B	DQ8B		
4A	VREFB4AN0	IO		DATA8	DIFFIO_RX_B157p	DIFFOUT_B157p	AP5	DQS16B/CQ16B/CQn16B/QKn16B	DQ8B		
4A	VREFB4AN0	IO		DATA14	DIFFIO_TX_B158n	DIFFOUT_B158n	AE7				
4A	VREFB4AN0	IO		DATA15	DIFFIO_TX_B158p	DIFFOUT_B158p	AF7	DQ16B	DQ8B		
4A	VREFB4AN0	IO		DATA9	DIFFIO_RX_B159n	DIFFOUT_B159n	AM5	DQ16B	DQ8B		
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_RX_B159p	DIFFOUT_B159p	AN5	DQ16B	DQ8B		
4A	VREFB4AN0	IO	VREFB4AN0				AK6				
4A	VREFB4AN0	IO					AL6	DQ16B	DQ8B		
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B160n	DIFFOUT_B160n	AH7	DQ16B	DQ8B		
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B160p	DIFFOUT_B160p	AJ7	DQ16B	DQ8B		
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B161n	DIFFOUT_B161n	AD6				
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B161p	DIFFOUT_B161p	AE6	DQ17B	DQ8B		
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B162n	DIFFOUT_B162n	AP3	DQ17B	DQ8B		
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B162p	DIFFOUT_B162p	AP4	DQ17B	DQ8B		
4A	VREFB4AN0	IO			DIFFIO_TX_B163n	DIFFOUT_B163n	AH6				
4A	VREFB4AN0	IO			DIFFIO_TX_B163p	DIFFOUT_B163p	AJ6	DQ17B	DQ8B		
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B164n	DIFFOUT_B164n	AP2	DQSn17B/QK17B	DQSn8B/QK8B		
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B164p	DIFFOUT_B164p	AN3	DQS17B/CQ17B/CQn17B/QKn17B	DQS8B/CQ8B/CQn8B/QKn8B		
4A	VREFB4AN0	IO			DIFFIO_TX_B165n	DIFFOUT_B165n	AC7				
4A	VREFB4AN0	IO			DIFFIO_TX_B165p	DIFFOUT_B165p	AC6	DQ17B	DQ8B		
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B166n	DIFFOUT_B166n	AL4	DQ17B	DQ8B		
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B166p	DIFFOUT_B166p	AL5	DQ17B	DQ8B		
4A	VREFB4AN0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	AM3				
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B167p	DIFFOUT_B167p	AM4	DQ17B	DQ8B		
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B168n	DIFFOUT_B168n	AF6	DQ17B	DQ8B		
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B168p	DIFFOUT_B168p	AG6	DQ17B	DQ8B		
		RREF_BR					AM1				
		DNU					AM2				
		DNU					AN2				
GXB_R0		REFCLK0Rp					AA8				
GXB_R0		REFCLK0Rn					AA7				
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AK2				
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AK1				
GXB_R0		GXB_TX_R0p					AJ3				
GXB_R0		GXB_TX_R0n					AJ4				
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AH2				
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AH1				
GXB_R0		GXB_TX_R1p					AG3				
GXB_R0		GXB_TX_R1n					AG4				
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AF2				
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AF1				
GXB_R0		GXB_TX_R2p					AE3				
GXB_R0		GXB_TX_R2n					AE4				
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AD2				
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AD1				
GXB_R0		GXB_TX_R3p					AC3				
GXB_R0		GXB_TX_R3n					AC4				
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					AB2				
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					AB1				
GXB_R0		GXB_TX_R4p					AA3				
GXB_R0		GXB_TX_R4n					AA4				
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					Y2				
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					Y1				
GXB_R0		GXB_TX_R5p					W3				
GXB_R0		GXB_TX_R5n					W4				
GXB_R0		REFCLK1Rp					W9				
GXB_R0		REFCLK1Rn					W8				
GXB_R1		REFCLK2Rp					U9				
GXB_R1		REFCLK2Rn					U8				
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					V2				
GXB_R1		GXB_RX_R6p,GXB_REFCLK_R6p					V1				
GXB_R1		GXB_TX_R6p					U3				
GXB_R1		GXB_TX_R6n					U4				
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					T2				
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					T1				
GXB_R1		GXB_TX_R7p					R3				
GXB_R1		GXB_TX_R7n					R4				
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					P2				
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					P1				
GXB_R1		GXB_TX_R8p					N3				
GXB_R1		GXB_TX_R8n					N4				
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					M2				
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					M1				
GXB_R1		GXB_TX_R9p					L3				
GXB_R1		GXB_TX_R9n					L4				
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					K2				
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					K1				

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Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
GXB_R1		GXB_TX_R10p					J3				
GXB_R1		GXB_TX_R10n					J4				
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					H2				
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					H1				
GXB_R1		GXB_TX_R11p					G3				
GXB_R1		GXB_TX_R11n					G4				
GXB_R1		REFCLK3Rp					R9				
GXB_R1		REFCLK3Rn					R8				
		DNU					K5				
7A		GND					H5				
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	E3	DQ1T	DQ1T		
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T1n	DIFFOUT_T1n	E4	DQ1T	DQ1T		
7A	VREFB7AN0	IO	RZQ_5		DIFFIO_TX_T2p	DIFFOUT_T2p	E1	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	F1				
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	D1	DQ1T	DQ1T		
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	E2	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	G6	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	H6				
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	C1	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T		
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	C2	DQSn1T/QK1T	DQSn1T/QK1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	E5	DQ1T	DQ1T		
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	F6				
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	C3	DQ1T	DQ1T		
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	D3	DQ1T	DQ1T		
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	J6	DQ1T	DQ1T		
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	K6				
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	A3	DQ2T	DQ1T		
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	B3	DQ2T	DQ1T		
7A	VREFB7AN0	IO					L6	DQ2T	DQ1T		
7A	VREFB7AN0	IO	VREFB7AN0				M7				
7A	VREFB7AN0	IO		DEV_OE	DIFFIO_RX_T10p	DIFFOUT_T10p	C6	DQ2T	DQ1T		
7A	VREFB7AN0	IO		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	D5	DQ2T	DQ1T		
7A	VREFB7AN0	IO		nPERSTR0	DIFFIO_TX_T11p	DIFFOUT_T11p	A2	DQ2T	DQ1T		
7A	VREFB7AN0	IO		nPERSTL0	DIFFIO_TX_T11n	DIFFOUT_T11n	B2				
7A	VREFB7AN0	IO		CvP_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	B5	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T		
7A	VREFB7AN0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	C4	DQSn2T/QK2T	DQ1T		
7A	VREFB7AN0	IO		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	A5	DQ2T	DQ1T		
7A	VREFB7AN0	IO		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	A4				
7A	VREFB7AN0	IO		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	D6	DQ2T	DQ1T		
7A	VREFB7AN0	IO		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	E6	DQ2T	DQ1T		
7A	VREFB7AN0	IO		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	J7	DQ2T	DQ1T		
7A	VREFB7AN0	IO		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	K7				
7B	VREFB7BN0	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	K9	DQ3T	DQ2T	DQ1T	DQ4_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	K8	DQ3T	DQ2T	DQ1T	DQ4_7B_1
7B	VREFB7BN0	IO					M10	DQ3T	DQ2T	DQ1T	DQ4_7B_2
7B	VREFB7BN0	IO	VREFB7BN0				P11				
7B	VREFB7BN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	C8	DQ3T	DQ2T	DQ1T	DQ4_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	D7	DQ3T	DQ2T	DQ1T	DQ4_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	E8	DQ3T	DQ2T	DQ1T	DQ4_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	F7				
7B	VREFB7BN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	N10	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	DQS4_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	N11	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T	DQS#4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	G8	DQ3T	DQ2T	DQ1T	DM4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	G7				
7B	VREFB7BN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H8	DQ3T	DQ2T	DQ1T	DQ4_7B_6
7B	VREFB7BN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	J8	DQ3T	DQ2T	DQ1T	DQ4_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	L9	DQ3T	DQ2T	DQ1T	DQ4_7B_8
7B	VREFB7BN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	M8				
7B	VREFB7BN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	B6	DQ4T	DQ2T	DQ1T	DQ3_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	C7	DQ4T	DQ2T	DQ1T	DQ3_7B_1
7B	VREFB7BN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	E9	DQ4T	DQ2T	DQ1T	DQ3_7B_2
7B	VREFB7BN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	F8				
7B	VREFB7BN0	IO			DIFFIO_RX_T41p	DIFFOUT_T41p	A7	DQ4T	DQ2T	DQ1T	DQ3_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T41n	DIFFOUT_T41n	A6	DQ4T	DQ2T	DQ1T	DQ3_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	G9	DQ4T	DQ2T	DQ1T	DQ3_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	H9				
7B	VREFB7BN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D8	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQS1T/CQ1T/CQn1T/QKn1T	DQS3_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	D9	DQSn4T/QK4T	DQ2T	DQSn1T/QK1T	DQS#3_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	A8	DQ4T	DQ2T	DQ1T	DM3_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	B8				
7B	VREFB7BN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	A10	DQ4T	DQ2T	DQ1T	DQ3_7B_6
7B	VREFB7BN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	B9	DQ4T	DQ2T	DQ1T	DQ3_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	J10	DQ4T	DQ2T	DQ1T	DQ3_7B_8
7B	VREFB7BN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	K10				
7C	VREFB7CN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	F10	DQ5T	DQ3T	DQ1T	DQ2_7C_0
7C	VREFB7CN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	G10	DQ5T	DQ3T	DQ1T	DQ2_7C_1
7C	VREFB7CN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	J11	DQ5T	DQ3T	DQ1T	DQ2_7C_2
7C	VREFB7CN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	K11				
7C	VREFB7CN0	IO			DIFFIO_RX_T49p	DIFFOUT_T49p	G11	DQ5T	DQ3T	DQ1T	DQ2_7C_3
7C	VREFB7CN0	IO			DIFFIO_RX_T49n	DIFFOUT_T49n	H11	DQ5T	DQ3T	DQ1T	DQ2_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	K12	DQ5T	DQ3T	DQ1T	DQ2_7C_5
7C	VREFB7CN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	L11				
7C	VREFB7CN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	E11	DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T	DQS2_7C
7C	VREFB7CN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	F11	DQSn5T/QK5T	DQSn3T/QK3T	DQ1T	DQS#2_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	C10	DQ5T	DQ3T	DQ1T	DM2_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	D10				
7C	VREFB7CN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	G12	DQ5T	DQ3T	DQ1T	DQ2_7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	H12	DQ5T	DQ3T	DQ1T	DQ2_7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	L12	DQ5T	DQ3T	DQ1T	DQ2_7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	M12				
7C	VREFB7CN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	A11	DQ6T	DQ3T	DQ1T	DQ1_7C_0
7C	VREFB7CN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	B11	DQ6T	DQ3T	DQ1T	DQ1_7C_1
7C	VREFB7CN0	IO					N13	DQ6T	DQ3T	DQ1T	DQ1_7C_2
7C	VREFB7CN0	IO	VREFB7CN0				M13				
7C	VREFB7CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	C11	DQ6T	DQ3T	DQ1T	DQ1_7C_3
7C	VREFB7CN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	D11	DQ6T	DQ3T	DQ1T	DQ1_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	J13	DQ6T	DQ3T	DQ1T	DQ1_7C_5
7C	VREFB7CN0	IO			DIFFIO_TX_T57n	DIFFOUT_T57n	K13				
7C	VREFB7CN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	A13	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQ1T	DQS1_7C

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Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
7C	VREFB7CN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	B12	DQSn6T/QK6T	DQ3T	DQ1T	DQS#1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	D12	DQ6T	DQ3T	DQ1T	DM1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T59n	DIFFOUT_T59n	E12				
7C	VREFB7CN0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	F13	DQ6T	DQ3T	DQ1T	DQ1_7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T60n	DIFFOUT_T60n	G13	DQ6T	DQ3T	DQ1T	DQ1_7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T61p	DIFFOUT_T61p	M11	DQ6T	DQ3T	DQ1T	DQ1_7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T61n	DIFFOUT_T61n	N12				RESET#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T62p	DIFFOUT_T62p	H14	DQ7T	DQ4T		CK_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T62n	DIFFOUT_T62n	J14	DQ7T	DQ4T		CK#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T63p	DIFFOUT_T63p	K14	DQ7T	DQ4T		CKE_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T63n	DIFFOUT_T63n	L14				CKE_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T64p	DIFFOUT_T64p	F14	DQ7T	DQ4T		A_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T64n	DIFFOUT_T64n	G14	DQ7T	DQ4T		A_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T65p	DIFFOUT_T65p	M14	DQ7T	DQ4T		A_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T65n	DIFFOUT_T65n	M15				A_7D_3
7D	VREFB7DN0	IO			DIFFIO_RX_T66p	DIFFOUT_T66p	G15	DQS7T/CQ7T/CQn7T/QKn7T	DQS4T/CQ4T/CQn4T/QKn4T		A_7D_4
7D	VREFB7DN0	IO			DIFFIO_RX_T66n	DIFFOUT_T66n	H15	DQSn7T/QK7T	DQSn4T/QK4T		A_7D_5
7D	VREFB7DN0	IO			DIFFIO_TX_T67p	DIFFOUT_T67p	C13	DQ7T	DQ4T		A_7D_6
7D	VREFB7DN0	IO			DIFFIO_TX_T67n	DIFFOUT_T67n	D13				A_7D_7
7D	VREFB7DN0	IO			DIFFIO_RX_T68p	DIFFOUT_T68p	D14	DQ7T	DQ4T		A_7D_8
7D	VREFB7DN0	IO			DIFFIO_RX_T68n	DIFFOUT_T68n	E14	DQ7T	DQ4T		A_7D_9
7D	VREFB7DN0	IO			DIFFIO_TX_T69p	DIFFOUT_T69p	K15	DQ7T	DQ4T		A_7D_10
7D	VREFB7DN0	IO			DIFFIO_TX_T69n	DIFFOUT_T69n	L15				A_7D_11
7D	VREFB7DN0	IO			DIFFIO_RX_T70p	DIFFOUT_T70p	B14	DQ8T	DQ4T		A_7D_12
7D	VREFB7DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	C14	DQ8T	DQ4T		A_7D_13
7D	VREFB7DN0	IO					N15	DQ8T	DQ4T		A_7D_14
7D	VREFB7DN0	IO	VREFB7DN0				N14				
7D	VREFB7DN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	A14	DQ8T	DQ4T		BA_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	B15	DQ8T	DQ4T		BA_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	D15	DQ8T	DQ4T		BA_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T72n	DIFFOUT_T72n	E15				RAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	F16	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T		CAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	G16	DQSn8T/QK8T	DQ4T		WE#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	J16	DQ8T	DQ4T		ODT_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	K16				ODT_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	C16	DQ8T	DQ4T		A_7D_15
7D	VREFB7DN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	D16	DQ8T	DQ4T		
7D	VREFB7DN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	M16	DQ8T	DQ4T		CS#_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	N16				CS#_7D_1
		VCCA_FPLL					R17				
		VCCD_FPLL					R16				
		DNU					L18				
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T85p	DIFFOUT_T85p	A16	DQ9T	DQ5T		
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T85n	DIFFOUT_T85n	A17	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T86p	DIFFOUT_T86p	K17	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T86n	DIFFOUT_T86n	L17				
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T87p	DIFFOUT_T87p	K18	DQ9T	DQ5T		
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T87n	DIFFOUT_T87n	K19	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T88p	DIFFOUT_T88p	D17	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T88n	DIFFOUT_T88n	E17				
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T89p	DIFFOUT_T89p	F17	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T		
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T89n	DIFFOUT_T89n	G17	DQSn9T/QK9T	DQSn5T/QK5T		
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T90p	DIFFOUT_T90p	M17	DQ9T	DQ5T		
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T90n	DIFFOUT_T90n	N17				
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T91p	DIFFOUT_T91p	H17	DQ9T	DQ5T		
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T91n	DIFFOUT_T91n	J17	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T92p	DIFFOUT_T92p	B17	DQ9T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T92n	DIFFOUT_T92n	C17				
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T93p	DIFFOUT_T93p	A19	DQ10T	DQ5T		
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T93n	DIFFOUT_T93n	A20	DQ10T	DQ5T		
8D	VREFB8DN0	IO					M18	DQ10T	DQ5T		
8D	VREFB8DN0	IO	VREFB8DN0				N18				
8D	VREFB8DN0	IO			DIFFIO_RX_T94p	DIFFOUT_T94p	C19	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T94n	DIFFOUT_T94n	B18	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T95p	DIFFOUT_T95p	G18	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T95n	DIFFOUT_T95n	G19				
8D	VREFB8DN0	IO			DIFFIO_RX_T96p	DIFFOUT_T96p	H18	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T96n	DIFFOUT_T96n	J19	DQSn10T/QK10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T97p	DIFFOUT_T97p	M19	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T97n	DIFFOUT_T97n	N19				
8D	VREFB8DN0	IO			DIFFIO_RX_T98p	DIFFOUT_T98p	D19	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_RX_T98n	DIFFOUT_T98n	D18	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T99p	DIFFOUT_T99p	E18	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T99n	DIFFOUT_T99n	F19				
8C	VREFB8CN0	IO			DIFFIO_RX_T116p	DIFFOUT_T116p	K20	DQ11T	DQ6T	DQ2T	DQ4_8C_0
8C	VREFB8CN0	IO			DIFFIO_RX_T116n	DIFFOUT_T116n	L20	DQ11T	DQ6T	DQ2T	DQ4_8C_1
8C	VREFB8CN0	IO					M20	DQ11T	DQ6T	DQ2T	DQ4_8C_2
8C	VREFB8CN0	IO	VREFB8CN0				N20				
8C	VREFB8CN0	IO			DIFFIO_RX_T117p	DIFFOUT_T117p	A22	DQ11T	DQ6T	DQ2T	DQ4_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T117n	DIFFOUT_T117n	B21	DQ11T	DQ6T	DQ2T	DQ4_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T118p	DIFFOUT_T118p	B20	DQ11T	DQ6T	DQ2T	DQ4_8C_5
8C	VREFB8CN0	IO			DIFFIO_TX_T118n	DIFFOUT_T118n	C20				
8C	VREFB8CN0	IO			DIFFIO_RX_T119p	DIFFOUT_T119p	D20	DQS11T/CQ11T/CQn11T/QKn11T	DQS6T/CQ6T/CQn6T/QKn6T	DQ2T	DQS4_8C
8C	VREFB8CN0	IO			DIFFIO_RX_T119n	DIFFOUT_T119n	E20	DQSn11T/QK11T	DQSn6T/QK6T	DQ2T	DQS#4_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T120p	DIFFOUT_T120p	K21	DQ11T	DQ6T	DQ2T	DM4_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T120n	DIFFOUT_T120n	L21				
8C	VREFB8CN0	IO			DIFFIO_RX_T121p	DIFFOUT_T121p	F20	DQ11T	DQ6T	DQ2T	DQ4_8C_6
8C	VREFB8CN0	IO			DIFFIO_RX_T121n	DIFFOUT_T121n	G20	DQ11T	DQ6T	DQ2T	DQ4_8C_7
8C	VREFB8CN0	IO			DIFFIO_TX_T122p	DIFFOUT_T122p	H20	DQ11T	DQ6T	DQ2T	DQ4_8C_8
8C	VREFB8CN0	IO			DIFFIO_TX_T122n	DIFFOUT_T122n	J20				
8C	VREFB8CN0	IO			DIFFIO_RX_T123p	DIFFOUT_T123p	D21	DQ12T	DQ6T	DQ2T	DQ3_8C_0
8C	VREFB8CN0	IO			DIFFIO_RX_T123n	DIFFOUT_T123n	E21	DQ12T	DQ6T	DQ2T	DQ3_8C_1
8C	VREFB8CN0	IO			DIFFIO_TX_T124p	DIFFOUT_T124p	M21	DQ12T	DQ6T	DQ2T	DQ3_8C_2
8C	VREFB8CN0	IO			DIFFIO_TX_T124n	DIFFOUT_T124n	N21				
8C	VREFB8CN0	IO			DIFFIO_RX_T125p	DIFFOUT_T125p	C22	DQ12T	DQ6T	DQ2T	DQ3_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T125n	DIFFOUT_T125n	D22	DQ12T	DQ6T	DQ2T	DQ3_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	G21	DQ12T	DQ6T	DQ2T	DQ3_8C_5
8C	VREFB8CN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	H21				
8C	VREFB8CN0	IO			DIFFIO_RX_T127p	DIFFOUT_T127p	F22	DQS12T/CQ12T/CQn12T/QKn12T	DQ6T	DQS2T/CQ2T/CQn2T/QKn2T	DQS3_8C

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Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
8C	VREFB8CN0	IO			DIFFIO_RX_T127n	DIFFOUT_T127n	G22	DQSn12T/QK12T	DQ6T	DQSn2T/QK2T	DQS#3_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	M22	DQ12T	DQ6T	DQ2T	DM3_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T128n	DIFFOUT_T128n	N22				
8C	VREFB8CN0	IO			DIFFIO_RX_T129p	DIFFOUT_T129p	A23	DQ12T	DQ6T	DQ2T	DQ3_8C_6
8C	VREFB8CN0	IO			DIFFIO_RX_T129n	DIFFOUT_T129n	B23	DQ12T	DQ6T	DQ2T	DQ3_8C_7
8C	VREFB8CN0	IO			DIFFIO_TX_T130p	DIFFOUT_T130p	J22	DQ12T	DQ6T	DQ2T	DQ3_8C_8
8C	VREFB8CN0	IO			DIFFIO_TX_T130n	DIFFOUT_T130n	K22				
8B	VREFB8BN0	IO			DIFFIO_RX_T131p	DIFFOUT_T131p	H23	DQ13T	DQ7T	DQ2T	DQ2_8B_0
8B	VREFB8BN0	IO			DIFFIO_RX_T131n	DIFFOUT_T131n	J23	DQ13T	DQ7T	DQ2T	DQ2_8B_1
8B	VREFB8BN0	IO			DIFFIO_TX_T132p	DIFFOUT_T132p	K24	DQ13T	DQ7T	DQ2T	DQ2_8B_2
8B	VREFB8BN0	IO			DIFFIO_TX_T132n	DIFFOUT_T132n	L24				
8B	VREFB8BN0	IO			DIFFIO_RX_T133p	DIFFOUT_T133p	B24	DQ13T	DQ7T	DQ2T	DQ2_8B_3
8B	VREFB8BN0	IO			DIFFIO_RX_T133n	DIFFOUT_T133n	C23	DQ13T	DQ7T	DQ2T	DQ2_8B_4
8B	VREFB8BN0	IO			DIFFIO_TX_T134p	DIFFOUT_T134p	D23	DQ13T	DQ7T	DQ2T	DQ2_8B_5
8B	VREFB8BN0	IO			DIFFIO_TX_T134n	DIFFOUT_T134n	E23				
8B	VREFB8BN0	IO			DIFFIO_RX_T135p	DIFFOUT_T135p	F23	DQS13T/CQ13T/CQn13T/QKn13T	DQS7T/CQ7T/CQn7T/QKn7T	DQ2T	DQS2_8B
8B	VREFB8BN0	IO			DIFFIO_RX_T135n	DIFFOUT_T135n	G23	DQSn13T/QK13T	DQSn7T/QK7T	DQ2T	DQS#2_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T136p	DIFFOUT_T136p	M23	DQ13T	DQ7T	DQ2T	DM2_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T136n	DIFFOUT_T136n	N23				
8B	VREFB8BN0	IO			DIFFIO_RX_T137p	DIFFOUT_T137p	D24	DQ13T	DQ7T	DQ2T	DQ2_8B_6
8B	VREFB8BN0	IO			DIFFIO_RX_T137n	DIFFOUT_T137n	E24	DQ13T	DQ7T	DQ2T	DQ2_8B_7
8B	VREFB8BN0	IO			DIFFIO_TX_T138p	DIFFOUT_T138p	K23	DQ13T	DQ7T	DQ2T	DQ2_8B_8
8B	VREFB8BN0	IO			DIFFIO_TX_T138n	DIFFOUT_T138n	L23				
8B	VREFB8BN0	IO			DIFFIO_RX_T139p	DIFFOUT_T139p	G24	DQ14T	DQ7T	DQ2T	DQ1_8B_0
8B	VREFB8BN0	IO			DIFFIO_RX_T139n	DIFFOUT_T139n	H24	DQ14T	DQ7T	DQ2T	DQ1_8B_1
8B	VREFB8BN0	IO					M24	DQ14T	DQ7T	DQ2T	DQ1_8B_2
8B	VREFB8BN0	IO	VREFB8BN0				N24				
8B	VREFB8BN0	IO			DIFFIO_RX_T140p	DIFFOUT_T140p	A26	DQ14T	DQ7T	DQ2T	DQ1_8B_3
8B	VREFB8BN0	IO			DIFFIO_RX_T140n	DIFFOUT_T140n	A25	DQ14T	DQ7T	DQ2T	DQ1_8B_4
8B	VREFB8BN0	IO			DIFFIO_TX_T141p	DIFFOUT_T141p	C25	DQ14T	DQ7T	DQ2T	DQ1_8B_5
8B	VREFB8BN0	IO			DIFFIO_TX_T141n	DIFFOUT_T141n	D25				
8B	VREFB8BN0	IO			DIFFIO_RX_T142p	DIFFOUT_T142p	F25	DQS14T/CQ14T/CQn14T/QKn14T	DQ7T	DQ2T	DQS1_8B
8B	VREFB8BN0	IO			DIFFIO_RX_T142n	DIFFOUT_T142n	G25	DQSn14T/QK14T	DQ7T	DQ2T	DQS#1_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T143p	DIFFOUT_T143p	M25	DQ14T	DQ7T	DQ2T	DM1_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T143n	DIFFOUT_T143n	N25				
8B	VREFB8BN0	IO			DIFFIO_RX_T144p	DIFFOUT_T144p	B26	DQ14T	DQ7T	DQ2T	DQ1_8B_6
8B	VREFB8BN0	IO			DIFFIO_RX_T144n	DIFFOUT_T144n	C26	DQ14T	DQ7T	DQ2T	DQ1_8B_7
8B	VREFB8BN0	IO			DIFFIO_TX_T145p	DIFFOUT_T145p	J25	DQ14T	DQ7T	DQ2T	DQ1_8B_8
8B	VREFB8BN0	IO			DIFFIO_TX_T145n	DIFFOUT_T145n	K25				RESET#_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T146p	DIFFOUT_T146p	E26	DQ15T	DQ8T		CK_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T146n	DIFFOUT_T146n	F26	DQ15T	DQ8T		CK#_8A
8A	VREFB8AN0	IO			DIFFIO_TX_T147p	DIFFOUT_T147p	K29	DQ15T	DQ8T		CKE_8A_0
8A	VREFB8AN0	IO			DIFFIO_TX_T147n	DIFFOUT_T147n	L29				CKE_8A_1
8A	VREFB8AN0	IO			DIFFIO_RX_T148p	DIFFOUT_T148p	D26	DQ15T	DQ8T		A_8A_0
8A	VREFB8AN0	IO			DIFFIO_RX_T148n	DIFFOUT_T148n	E27	DQ15T	DQ8T		A_8A_1
8A	VREFB8AN0	IO			DIFFIO_TX_T149p	DIFFOUT_T149p	A27	DQ15T	DQ8T		A_8A_2
8A	VREFB8AN0	IO			DIFFIO_TX_T149n	DIFFOUT_T149n	B27				A_8A_3
8A	VREFB8AN0	IO			DIFFIO_RX_T150p	DIFFOUT_T150p	G26	DQS15T/CQ15T/CQn15T/QKn15T	DQS8T/CQ8T/CQn8T/QKn8T		A_8A_4
8A	VREFB8AN0	IO			DIFFIO_RX_T150n	DIFFOUT_T150n	H26	DQSn15T/QK15T	DQSn8T/QK8T		A_8A_5
8A	VREFB8AN0	IO			DIFFIO_TX_T151p	DIFFOUT_T151p	K27	DQ15T	DQ8T		A_8A_6
8A	VREFB8AN0	IO			DIFFIO_TX_T151n	DIFFOUT_T151n	L27				A_8A_7
8A	VREFB8AN0	IO			DIFFIO_RX_T152p	DIFFOUT_T152p	D27	DQ15T	DQ8T		A_8A_8
8A	VREFB8AN0	IO			DIFFIO_RX_T152n	DIFFOUT_T152n	C28	DQ15T	DQ8T		A_8A_9
8A	VREFB8AN0	IO			DIFFIO_TX_T153p	DIFFOUT_T153p	C29	DQ15T	DQ8T		A_8A_10
8A	VREFB8AN0	IO			DIFFIO_TX_T153n	DIFFOUT_T153n	D28				A_8A_11
8A	VREFB8AN0	IO			DIFFIO_RX_T154p	DIFFOUT_T154p	G27	DQ16T	DQ8T		A_8A_12
8A	VREFB8AN0	IO			DIFFIO_RX_T154n	DIFFOUT_T154n	G28	DQ16T	DQ8T		A_8A_13
8A	VREFB8AN0	IO			DIFFIO_TX_T155p	DIFFOUT_T155p	J26	DQ16T	DQ8T		A_8A_14
8A	VREFB8AN0	IO			DIFFIO_TX_T155n	DIFFOUT_T155n	K26				A_8A_15
8A	VREFB8AN0	IO			DIFFIO_RX_T156p	DIFFOUT_T156p	A29	DQ16T	DQ8T		BA_8A_0
8A	VREFB8AN0	IO			DIFFIO_RX_T156n	DIFFOUT_T156n	A28	DQ16T	DQ8T		BA_8A_1
8A	VREFB8AN0	IO			DIFFIO_TX_T157p	DIFFOUT_T157p	B29	DQ16T	DQ8T		BA_8A_2
8A	VREFB8AN0	IO			DIFFIO_TX_T157n	DIFFOUT_T157n	B30				RAS#_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T158p	DIFFOUT_T158p	F28	DQS16T/CQ16T/CQn16T/QKn16T	DQ8T		CAS#_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T158n	DIFFOUT_T158n	F29	DQSn16T/QK16T	DQ8T		WE#_8A
8A	VREFB8AN0	IO			DIFFIO_TX_T159p	DIFFOUT_T159p	H27	DQ16T	DQ8T		ODT_8A_0
8A	VREFB8AN0	IO			DIFFIO_TX_T159n	DIFFOUT_T159n	J27				ODT_8A_1
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T160p	DIFFOUT_T160p	D29	DQ16T	DQ8T		
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T160n	DIFFOUT_T160n	E29	DQ16T	DQ8T		
8A	VREFB8AN0	IO			DIFFIO_TX_T161p	DIFFOUT_T161p	D30	DQ16T	DQ8T		CS#_8A_0
8A	VREFB8AN0	IO			DIFFIO_TX_T161n	DIFFOUT_T161n	E30				CS#_8A_1
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T162p	DIFFOUT_T162p	G29	DQ17T			
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T162n	DIFFOUT_T162n	H29	DQ17T			
8A	VREFB8AN0	IO					L26	DQ17T			
8A	VREFB8AN0	IO	VREFB8AN0				M27				
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T163p	DIFFOUT_T163p	A31	DQ17T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T163n	DIFFOUT_T163n	A30	DQ17T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T164p	DIFFOUT_T164p	C31	DQ17T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T164n	DIFFOUT_T164n	D31				
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T165p	DIFFOUT_T165p	A32	DQS17T/CQ17T/CQn17T/QKn17T			
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T165n	DIFFOUT_T165n	B32	DQSn17T/QK17T			
8A	VREFB8AN0	IO			DIFFIO_TX_T166p	DIFFOUT_T166p	J28	DQ17T			
8A	VREFB8AN0	IO			DIFFIO_TX_T166n	DIFFOUT_T166n	K28				
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T167p	DIFFOUT_T167p	D33	DQ17T			
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T167n	DIFFOUT_T167n	C32	DQ17T			
8A	VREFB8AN0	IO			DIFFIO_TX_T168p	DIFFOUT_T168p	D32	DQ17T			
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T168n	DIFFOUT_T168n	E32				
8A		MSEL0		MSEL0			D34				
8A		MSEL1		MSEL1			H30				
8A		MSEL2		MSEL2			K30				
8A		MSEL3		MSEL3			M29				
8A		MSEL4		MSEL4			M30				
8A		CONF_DONE		CONF_DONE			C34				
8A		nSTATUS		nSTATUS			B34				
8A		nCE		nCE			A33				
8A		nCONFIG		nCONFIG			C33				
8A		GND					B33				
		GND					AA26				
		GND					AA33				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					AA34				
		GND					AB27				
		GND					AB28				
		GND					AB29				
		GND					AB30				
		GND					AB31				
		GND					AB32				
		GND					AC30				
		GND					AC33				
		GND					AC34				
		GND					AD31				
		GND					AD32				
		GND					AE30				
		GND					AE33				
		GND					AE34				
		GND					AF31				
		GND					AF32				
		GND					AG30				
		GND					AG33				
		GND					AG34				
		GND					AH31				
		GND					AH32				
		GND					AJ30				
		GND					AJ33				
		GND					AJ34				
		GND					AK31				
		GND					AK32				
		GND					AL33				
		GND					AL34				
		GND					E34				
		GND					F31				
		GND					F32				
		GND					G30				
		GND					G33				
		GND					G34				
		GND					H31				
		GND					H32				
		GND					J30				
		GND					J33				
		GND					J34				
		GND					K31				
		GND					K32				
		GND					L30				
		GND					L33				
		GND					L34				
		GND					M31				
		GND					M32				
		GND					N28				
		GND					N29				
		GND					N33				
		GND					N34				
		GND					P27				
		GND					P31				
		GND					P32				
		GND					R28				
		GND					R30				
		GND					R33				
		GND					R34				
		GND					T27				
		GND					T29				
		GND					T31				
		GND					T32				
		GND					U28				
		GND					U33				
		GND					U34				
		GND					V27				
		GND					V31				
		GND					V32				
		GND					W28				
		GND					W30				
		GND					W33				
		GND					W34				
		GND					Y27				
		GND					Y29				
		GND					Y31				
		GND					Y32				
		GND					AA1				
		GND					AA2				
		GND					AA9				
		GND					AB3				
		GND					AB4				
		GND					AB5				
		GND					AB7				
		GND					AB8				
		GND					AC1				
		GND					AC2				
		GND					AC5				
		GND					AD3				
		GND					AD4				
		GND					AE1				
		GND					AE2				
		GND					AE5				
		GND					AF3				
		GND					AF4				
		GND					AG1				
		GND					AG2				
		GND					AG5				
		GND					AH3				
		GND					AH4				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					AJ1				
		GND					AJ2				
		GND					AJ5				
		GND					AK3				
		GND					AK4				
		GND					AL1				
		GND					AL2				
		GND					AL3				
		GND					AN1				
		GND					F3				
		GND					F4				
		GND					G1				
		GND					G2				
		GND					G5				
		GND					H3				
		GND					H4				
		GND					J1				
		GND					J2				
		GND					J5				
		GND					K3				
		GND					K4				
		GND					L1				
		GND					L2				
		GND					L5				
		GND					M3				
		GND					M4				
		GND					M5				
		GND					N1				
		GND					N2				
		GND					N6				
		GND					P3				
		GND					P4				
		GND					P8				
		GND					R1				
		GND					R2				
		GND					R5				
		GND					R7				
		GND					T3				
		GND					T4				
		GND					T6				
		GND					T8				
		GND					U1				
		GND					U2				
		GND					U7				
		GND					V3				
		GND					V4				
		GND					V8				
		GND					W1				
		GND					W2				
		GND					W5				
		GND					W7				
		GND					Y3				
		GND					Y4				
		GND					Y6				
		GND					Y8				
		VCCP					P18				
		VCCP					R13				
		VCCP					R21				
		VCCP					T10				
		VCCP					U25				
		VCCP					V10				
		VCCP					W25				
		VCCP					Y12				
		VCCP					Y19				
		VCCP					Y22				
		VCCA_FPLL					V26				
		VCCA_FPLL					V9				
		VCCA_FPLL					T26				
		VCCA_FPLL					T9				
		VCCBAT					M28				
		VCC_AUX					P12				
		VCC_AUX					P24				
		VCC_AUX					W11				
		VCC_AUX					Y24				
		VCCD_FPLL					Y26				
		VCCD_FPLL					Y9				
		VCCD_FPLL					P26				
		VCCD_FPLL					P9				
		VCCA_GXBL0					Y28				
		VCCA_GXBR0					Y7				
		VCCA_GXBL1					T28				
		VCCA_GXBR1					T7				
		VCCH_GXBL0					V28				
		VCCH_GXBR0					V7				
		VCCH_GXBL1					P28				
		VCCH_GXBR1					P7				
		VCCL_GXBL0					V29				
		VCCL_GXBL0					V30				
		VCCL_GXBR0					V5				
		VCCL_GXBR0					V6				
		VCCL_GXBL1					P29				
		VCCL_GXBL1					P30				
		VCCL_GXBR1					P5				
		VCCL_GXBR1					P6				
		VCCR_GXBL					AA29				
		VCCR_GXBL					AA30				
		VCCR_GXBL					N30				
		VCCR_GXBL					U29				
		VCCR_GXBL					U30				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		VCCR_GXBR					AA5				
		VCCR_GXBR					AA6				
		VCCR_GXBR					N5				
		VCCR_GXBR					U5				
		VCCR_GXBR					U6				
		VCCT_GXBL0					W29				
		VCCT_GXBL0					Y30				
		VCCT_GXBR0					W6				
		VCCT_GXBR0					Y5				
		VCCT_GXBL1					R29				
		VCCT_GXBL1					T30				
		VCCT_GXBR1					R6				
		VCCT_GXBR1					T5				
		VCC					R14				
		VCC					R15				
		VCC					R19				
		VCC					R23				
		VCC					R25				
		VCC					T12				
		VCC					T14				
		VCC					T16				
		VCC					T18				
		VCC					T20				
		VCC					T22				
		VCC					T24				
		VCC					U11				
		VCC					U12				
		VCC					U13				
		VCC					U15				
		VCC					U17				
		VCC					U19				
		VCC					U20				
		VCC					U21				
		VCC					U22				
		VCC					U23				
		VCC					V12				
		VCC					V14				
		VCC					V16				
		VCC					V20				
		VCC					V22				
		VCC					V24				
		VCC					W13				
		VCC					W15				
		VCC					W17				
		VCC					W19				
		VCC					W21				
		VCC					W23				
		VCC					Y13				
		VCC					Y20				
		VCC					V18				
		VCCIO3A					AD30				
		VCCIO3A					AF27				
		VCCIO3A					AH30				
		VCCIO3A					AJ27				
		VCCIO3A					AK30				
		VCCIO3A					AM27				
		VCCIO3B					AF24				
		VCCIO3B					AJ24				
		VCCIO3B					AM24				
		VCCIO3B					AP24				
		VCCIO3C					AF21				
		VCCIO3C					AJ21				
		VCCIO3C					AM21				
		VCCIO3C					AP21				
		VCCIO3D					AF18				
		VCCIO3D					AJ18				
		VCCIO3D					AM18				
		VCCIO3D					AP18				
		VCCIO4A					AD5				
		VCCIO4A					AF5				
		VCCIO4A					AH5				
		VCCIO4A					AK5				
		VCCIO4B					AF9				
		VCCIO4B					AJ9				
		VCCIO4B					AM9				
		VCCIO4B					AP9				
		VCCIO4C					AF12				
		VCCIO4C					AJ12				
		VCCIO4C					AM12				
		VCCIO4C					AP12				
		VCCIO4D					AF15				
		VCCIO4D					AJ15				
		VCCIO4D					AM15				
		VCCIO4D					AP15				
		VCCIO7A					C5				
		VCCIO7A					F2				
		VCCIO7A					F5				
		VCCIO7A					L7				
		VCCIO7B					A9				
		VCCIO7B					C9				
		VCCIO7B					F9				
		VCCIO7B					J9				
		VCCIO7C					A12				
		VCCIO7C					C12				
		VCCIO7C					F12				
		VCCIO7C					J12				
		VCCIO7D					A15				
		VCCIO7D					C15				
		VCCIO7D					F15				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		VCCIO7D					J15				
		VCCIO8A					C27				
		VCCIO8A					C30				
		VCCIO8A					F27				
		VCCIO8A					F30				
		VCCIO8A					J29				
		VCCIO8A					M26				
		VCCIO8B					A24				
		VCCIO8B					C24				
		VCCIO8B					F24				
		VCCIO8B					J24				
		VCCIO8C					A21				
		VCCIO8C					C21				
		VCCIO8C					F21				
		VCCIO8C					J21				
		VCCIO8D					A18				
		VCCIO8D					C18				
		VCCIO8D					F18				
		VCCIO8D					J18				
		VCCPD3					AB26				
		VCCPD3					AC27				
		VCCPD3					Y21				
		VCCPD3					Y25				
		VCCPD4A					AB6				
		VCCPD4A					AB9				
		VCCPD4BCD					Y10				
		VCCPD4BCD					Y14				
		VCCPD4BCD					Y16				
		VCCPD7A					N8				
		VCCPD7A					N9				
		VCCPD7BCD					P14				
		VCCPD7BCD					P16				
		VCCPD7BCD					R11				
		VCCPD8					N26				
		VCCPD8					N27				
		VCCPD8					P20				
		VCCPD8					P22				
		VCCPGM					M9				
		VCCPGM					AC26				
		GND					AA11				
		GND					AA13				
		GND					AA16				
		GND					AA19				
		GND					AA22				
		GND					AA24				
		GND					AD10				
		GND					AD13				
		GND					AD16				
		GND					AD19				
		GND					AD22				
		GND					AD25				
		GND					AD28				
		GND					AD7				
		GND					AG10				
		GND					AG13				
		GND					AG16				
		GND					AG19				
		GND					AG22				
		GND					AG25				
		GND					AG28				
		GND					AG7				
		GND					AK10				
		GND					AK13				
		GND					AK16				
		GND					AK19				
		GND					AK22				
		GND					AK25				
		GND					AK28				
		GND					AK7				
		GND					AN10				
		GND					AN13				
		GND					AN16				
		GND					AN19				
		GND					AN22				
		GND					AN25				
		GND					AN28				
		GND					AN31				
		GND					AN4				
		GND					AN7				
		GND					B1				
		GND					B10				
		GND					B13				
		GND					B16				
		GND					B19				
		GND					B22				
		GND					B25				
		GND					B28				
		GND					B31				
		GND					B4				
		GND					B7				
		GND					D2				
		GND					D4				
		GND					E10				
		GND					E13				
		GND					E16				
		GND					E19				
		GND					E22				
		GND					E25				
		GND					E28				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					E31				
		GND					E7				
		GND					H10				
		GND					H13				
		GND					H16				
		GND					H19				
		GND					H22				
		GND					H25				
		GND					H28				
		GND					H7				
		GND					L10				
		GND					L13				
		GND					L16				
		GND					L19				
		GND					L22				
		GND					L25				
		GND					L28				
		GND					L8				
		GND					M6				
		GND					N7				
		GND					P10				
		GND					P13				
		GND					P15				
		GND					P17				
		GND					P19				
		GND					P21				
		GND					P23				
		GND					P25				
		GND					R10				
		GND					R12				
		GND					R18				
		GND					R20				
		GND					R22				
		GND					R24				
		GND					T11				
		GND					T13				
		GND					T15				
		GND					T17				
		GND					T19				
		GND					T21				
		GND					T23				
		GND					T25				
		GND					U10				
		GND					U14				
		GND					U16				
		GND					U24				
		GND					V11				
		GND					V13				
		GND					V15				
		GND					V17				
		GND					V19				
		GND					V21				
		GND					V23				
		GND					V25				
		GND					W10				
		GND					W12				
		GND					W14				
		GND					W16				
		GND					W18				
		GND					W20				
		GND					W22				
		GND					W24				
		GND					U18				

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) RESET pin is only applicable for DDR3 device.

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		DNU					AJ38				
		DNU					B38				
		RREF_TL					B39				
GXB_L1		REFCLK3Ln					AA32				
GXB_L1		REFCLK3Lp					AA31				
GXB_L1		GXB_TX_L11n					R36				
GXB_L1		GXB_TX_L11p					R37				
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					T39				
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					T38				
GXB_L1		GXB_TX_L10n					U36				
GXB_L1		GXB_TX_L10p					U37				
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					V39				
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					V38				
GXB_L1		GXB_TX_L9n					W36				
GXB_L1		GXB_TX_L9p					W37				
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					Y39				
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					Y38				
GXB_L1		GXB_TX_L8n					AA36				
GXB_L1		GXB_TX_L8p					AA37				
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					AB39				
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					AB38				
GXB_L1		GXB_TX_L7n					AC36				
GXB_L1		GXB_TX_L7p					AC37				
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					AD39				
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					AD38				
GXB_L1		GXB_TX_L6n					AE36				
GXB_L1		GXB_TX_L6p					AE37				
GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p					AF39				
GXB_L1		GXB_RX_L6n,GXB_REFCLK_L6n					AF38				
GXB_L1		REFCLK2Ln					AC32				
GXB_L1		REFCLK2Lp					AC31				
GXB_L0		REFCLK1Ln					AE32				
GXB_L0		REFCLK1Lp					AE31				
GXB_L0		GXB_TX_L5n					AG36				
GXB_L0		GXB_TX_L5p					AG37				
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p					AH39				
GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n					AH38				
GXB_L0		GXB_TX_L4n					AJ36				
GXB_L0		GXB_TX_L4p					AJ37				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AK39				
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AK38				
GXB_L0		GXB_TX_L3n					AL36				
GXB_L0		GXB_TX_L3p					AL37				
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p					AM39				
GXB_L0		GXB_RX_L3n,GXB_REFCLK_L3n					AM38				
GXB_L0		GXB_TX_L2n					AN36				
GXB_L0		GXB_TX_L2p					AN37				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AP39				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AP38				
GXB_L0		GXB_TX_L1n					AR36				
GXB_L0		GXB_TX_L1p					AR37				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AT39				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AT38				
GXB_L0		GXB_TX_L0n					AU36				
GXB_L0		GXB_TX_L0p					AU37				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AW37				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AW36				
GXB_L0		REFCLK0Ln					AG33				
GXB_L0		REFCLK0Lp					AG32				
		DNU					AH31				
3A		TDO		TDO			AT34				
3A		TMS		TMS			AM35				
3A		TCK		TCK			AV34				
3A		TDI		TDI			AT33				
3A		DCLK		DCLK			AW34				
3A		nCSO		DATA4			AR34				
3A		AS_DATA3		DATA3			AU34				
3A		AS_DATA2		DATA2			AR33				
3A		AS_DATA1		DATA1			AU33				
3A		AS_DATA0,ASDO		DATA0			AV33				
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AN33				
3A	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AP33	DQ1B			
3A	VREFB3AN0	IO	CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AN34	DQ1B			
3A	VREFB3AN0	IO	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AP34	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B3n	DIFFOUT_B3n	AK32				
3A	VREFB3AN0	IO			DIFFIO_TX_B3p	DIFFOUT_B3p	AL32	DQ1B			
3A	VREFB3AN0	IO	CLK1n		DIFFIO_RX_B4n	DIFFOUT_B4n	AJ34	DQSn1B/QK1B			
3A	VREFB3AN0	IO	CLK1p		DIFFIO_RX_B4p	DIFFOUT_B4p	AK34	DQS1B/CQ1B/CQn1B/QKn1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AL34				
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AM34	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AJ33	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AK33	DQ1B			
3A	VREFB3AN0	IO	VREFB3AN0				AJ31				
3A	VREFB3AN0	IO					AK31	DQ1B			
3A	VREFB3AN0	IO	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AL33	DQ1B			
3A	VREFB3AN0	IO	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AM33	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B8n	DIFFOUT_B8n	AN32				CS#_3A_1
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AP32	DQ2B	DQ1B		CS#_3A_0
3A	VREFB3AN0	IO	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AT32	DQ2B	DQ1B		
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AU32	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AL31				ODT_3A_1
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AM31	DQ2B	DQ1B		ODT_3A_0
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AW33	DQSn2B/QK2B	DQ1B		WE#_3A
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AW32	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B		CAS#_3A
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AN31				RAS#_3A
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AP31	DQ2B	DQ1B		BA_3A_2

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
3A	VREFB3AN0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AR31	DQ2B	DQ1B		BA_3A_1
3A	VREFB3AN0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AT31	DQ2B	DQ1B		BA_3A_0
3A	VREFB3AN0	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AD29				A_3A_15
3A	VREFB3AN0	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AE29	DQ2B	DQ1B		A_3A_14
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AG30	DQ2B	DQ1B		A_3A_13
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AH30	DQ2B	DQ1B		A_3A_12
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AU31				A_3A_11
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AV31	DQ3B	DQ1B		A_3A_10
3A	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AW30	DQ3B	DQ1B		A_3A_9
3A	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AW31	DQ3B	DQ1B		A_3A_8
3A	VREFB3AN0	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AK30				A_3A_7
3A	VREFB3AN0	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AL30	DQ3B	DQ1B		A_3A_6
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AR30	DQSn3B/QK3B	DQSn1B/QK1B		A_3A_5
3A	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AT30	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/CQ1B/CQn1B/QKn1B		A_3A_4
3A	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AU30				A_3A_3
3A	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AV30	DQ3B	DQ1B		A_3A_2
3A	VREFB3AN0	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AT29	DQ3B	DQ1B		A_3A_1
3A	VREFB3AN0	IO			DIFFIO_RX_B21p	DIFFOUT_B21p	AU29	DQ3B	DQ1B		A_3A_0
3A	VREFB3AN0	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AN30				CKE_3A_1
3A	VREFB3AN0	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AP30	DQ3B	DQ1B		CKE_3A_0
3A	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AN29	DQ3B	DQ1B		CK#_3A
3A	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AP29	DQ3B	DQ1B		CK_3A
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AB29				RESET#_3A
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AC29	DQ4B	DQ2B	DQ1B	DQ1_3B_8
3B	VREFB3BN0	IO			DIFFIO_RX_B25n	DIFFOUT_B25n	AF28	DQ4B	DQ2B	DQ1B	DQ1_3B_7
3B	VREFB3BN0	IO			DIFFIO_RX_B25p	DIFFOUT_B25p	AG28	DQ4B	DQ2B	DQ1B	DQ1_3B_6
3B	VREFB3BN0	IO			DIFFIO_TX_B26n	DIFFOUT_B26n	AK29				
3B	VREFB3BN0	IO			DIFFIO_TX_B26p	DIFFOUT_B26p	AL29	DQ4B	DQ2B	DQ1B	DM1_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AH28	DQSn4B/QK4B	DQ2B	DQ1B	DQS#1_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AJ28	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	DQ1B	DQS1_3B
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AD28				
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AE28	DQ4B	DQ2B	DQ1B	DQ1_3B_5
3B	VREFB3BN0	IO			DIFFIO_RX_B29n	DIFFOUT_B29n	AB27	DQ4B	DQ2B	DQ1B	DQ1_3B_4
3B	VREFB3BN0	IO			DIFFIO_RX_B29p	DIFFOUT_B29p	AB28	DQ4B	DQ2B	DQ1B	DQ1_3B_3
3B	VREFB3BN0	IO	VREFB3BN0				AL28				
3B	VREFB3BN0	IO					AM28	DQ4B	DQ2B	DQ1B	DQ1_3B_2
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AC27	DQ4B	DQ2B	DQ1B	DQ1_3B_1
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AD27	DQ4B	DQ2B	DQ1B	DQ1_3B_0
3B	VREFB3BN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AP28				
3B	VREFB3BN0	IO			DIFFIO_TX_B31p	DIFFOUT_B31p	AR28	DQ5B	DQ2B	DQ1B	DQ2_3B_8
3B	VREFB3BN0	IO			DIFFIO_RX_B32n	DIFFOUT_B32n	AU28	DQ5B	DQ2B	DQ1B	DQ2_3B_7
3B	VREFB3BN0	IO			DIFFIO_RX_B32p	DIFFOUT_B32p	AV28	DQ5B	DQ2B	DQ1B	DQ2_3B_6
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AJ27				
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AK27	DQ5B	DQ2B	DQ1B	DM2_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AW29	DQSn5B/QK5B	DQSn2B/QK2B	DQ1B	DQS#2_3B
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AW28	DQS5B/CQ5B/CQn5B/QKn5B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	DQS2_3B
3B	VREFB3BN0	IO			DIFFIO_TX_B35n	DIFFOUT_B35n	AP27				
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AR27	DQ5B	DQ2B	DQ1B	DQ2_3B_5
3B	VREFB3BN0	IO			DIFFIO_RX_B36n	DIFFOUT_B36n	AT27	DQ5B	DQ2B	DQ1B	DQ2_3B_4
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AU27	DQ5B	DQ2B	DQ1B	DQ2_3B_3
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AM27				
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AN27	DQ5B	DQ2B	DQ1B	DQ2_3B_2
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AV27	DQ5B	DQ2B	DQ1B	DQ2_3B_1
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AW27	DQ5B	DQ2B	DQ1B	DQ2_3B_0
3C	VREFB3CN0	IO			DIFFIO_TX_B39n	DIFFOUT_B39n	AG27				
3C	VREFB3CN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AH27	DQ6B	DQ3B	DQ1B	DQ3_3C_8
3C	VREFB3CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AB25	DQ6B	DQ3B	DQ1B	DQ3_3C_7
3C	VREFB3CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AC25	DQ6B	DQ3B	DQ1B	DQ3_3C_6
3C	VREFB3CN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AE27				
3C	VREFB3CN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AF27	DQ6B	DQ3B	DQ1B	DM3_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AE25	DQSn6B/QK6B	DQ3B	DQSn1B/QK1B	DQS#3_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AF25	DQS6B/CQ6B/CQn6B/QKn6B	DQ3B	DQS1B/CQ1B/CQn1B/QKn1B	DQS3_3C
3C	VREFB3CN0	IO			DIFFIO_TX_B43n	DIFFOUT_B43n	AC24				
3C	VREFB3CN0	IO			DIFFIO_TX_B43p	DIFFOUT_B43p	AD25	DQ6B	DQ3B	DQ1B	DQ3_3C_5
3C	VREFB3CN0	IO			DIFFIO_RX_B44n	DIFFOUT_B44n	AG26	DQ6B	DQ3B	DQ1B	DQ3_3C_4
3C	VREFB3CN0	IO			DIFFIO_RX_B44p	DIFFOUT_B44p	AH26	DQ6B	DQ3B	DQ1B	DQ3_3C_3
3C	VREFB3CN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AD26				
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AE26	DQ6B	DQ3B	DQ1B	DQ3_3C_2
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AG25	DQ6B	DQ3B	DQ1B	DQ3_3C_1
3C	VREFB3CN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AH25	DQ6B	DQ3B	DQ1B	DQ3_3C_0
3C	VREFB3CN0	IO			DIFFIO_TX_B47n	DIFFOUT_B47n	AN26				
3C	VREFB3CN0	IO			DIFFIO_TX_B47p	DIFFOUT_B47p	AP26	DQ7B	DQ3B	DQ1B	DQ4_3C_8
3C	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AM25	DQ7B	DQ3B	DQ1B	DQ4_3C_7
3C	VREFB3CN0	IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AN25	DQ7B	DQ3B	DQ1B	DQ4_3C_6
3C	VREFB3CN0	IO			DIFFIO_TX_B49n	DIFFOUT_B49n	AJ25				
3C	VREFB3CN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AK25	DQ7B	DQ3B	DQ1B	DM4_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AT26	DQSn7B/QK7B	DQSn3B/QK3B	DQ1B	DQS#4_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AU26	DQS7B/CQ7B/CQn7B/QKn7B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	DQS4_3C
3C	VREFB3CN0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AR25				
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AT25	DQ7B	DQ3B	DQ1B	DQ4_3C_5
3C	VREFB3CN0	IO			DIFFIO_RX_B52n	DIFFOUT_B52n	AW25	DQ7B	DQ3B	DQ1B	DQ4_3C_4
3C	VREFB3CN0	IO			DIFFIO_RX_B52p	DIFFOUT_B52p	AW26	DQ7B	DQ3B	DQ1B	DQ4_3C_3
3C	VREFB3CN0	IO	VREFB3CN0				AK26				
3C	VREFB3CN0	IO					AL26	DQ7B	DQ3B	DQ1B	DQ4_3C_2
3C	VREFB3CN0	IO			DIFFIO_RX_B53n	DIFFOUT_B53n	AV25	DQ7B	DQ3B	DQ1B	DQ4_3C_1
3C	VREFB3CN0	IO			DIFFIO_RX_B53p	DIFFOUT_B53p	AV24	DQ7B	DQ3B	DQ1B	DQ4_3C_0
3C	VREFB3CN0	IO			DIFFIO_TX_B54n	DIFFOUT_B54n	AD23				
3C	VREFB3CN0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AD24	DQ8B	DQ4B	DQ2B	DQ5_3C_8
3C	VREFB3CN0	IO			DIFFIO_RX_B55n	DIFFOUT_B55n	AT24	DQ8B	DQ4B	DQ2B	DQ5_3C_7
3C	VREFB3CN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AU24	DQ8B	DQ4B	DQ2B	DQ5_3C_6
3C	VREFB3CN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AK24				
3C	VREFB3CN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AL24	DQ8B	DQ4B	DQ2B	DM5_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B57n	DIFFOUT_B57n	AE24	DQSn8B/QK8B	DQ4B	DQ2B	DQS#5_3C
3C	VREFB3CN0	IO			DIFFIO_RX_B57p	DIFFOUT_B57p	AF24	DQS8B/CQ8B/CQn8B/QKn8B	DQ4B	DQ2B	DQS5_3C
3C	VREFB3CN0	IO			DIFFIO_TX_B58n	DIFFOUT_B58n	AG24				
3C	VREFB3CN0	IO			DIFFIO_TX_B58p	DIFFOUT_B58p	AH24	DQ8B	DQ4B	DQ2B	DQ5_3C_5

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
3C	VREFB3CN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AW23	DQ8B	DQ4B	DQ2B	DQ5_3C_4
3C	VREFB3CN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AW24	DQ8B	DQ4B	DQ2B	DQ5_3C_3
3C	VREFB3CN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AN24				
3C	VREFB3CN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AP24	DQ8B	DQ4B	DQ2B	DQ5_3C_2
3C	VREFB3CN0	IO			DIFFIO_RX_B61n	DIFFOUT_B61n	AT23	DQ8B	DQ4B	DQ2B	DQ5_3C_1
3C	VREFB3CN0	IO			DIFFIO_RX_B61p	DIFFOUT_B61p	AU23	DQ8B	DQ4B	DQ2B	DQ5_3C_0
3D	VREFB3DN0	IO			DIFFIO_TX_B62n	DIFFOUT_B62n	AN23				
3D	VREFB3DN0	IO			DIFFIO_TX_B62p	DIFFOUT_B62p	AP23	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B63n	DIFFOUT_B63n	AD22	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B63p	DIFFOUT_B63p	AE23	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AK23				
3D	VREFB3DN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AL23	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B65n	DIFFOUT_B65n	AT22	DQSn9B/QK9B	DQSn4B/QK4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B65p	DIFFOUT_B65p	AU22	DQS9B/CQ9B/CQn9B/QKn9B	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B66n	DIFFOUT_B66n	AV22				
3D	VREFB3DN0	IO			DIFFIO_TX_B66p	DIFFOUT_B66p	AW22	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AV21	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AW21	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AG23				
3D	VREFB3DN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AH23	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B69n	DIFFOUT_B69n	AE22	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B69p	DIFFOUT_B69p	AF22	DQ9B	DQ4B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B70n	DIFFOUT_B70n	AN22				
3D	VREFB3DN0	IO			DIFFIO_TX_B70p	DIFFOUT_B70p	AP22	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AW19	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AW20	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AK22				
3D	VREFB3DN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AL22	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B73n	DIFFOUT_B73n	AR21	DQSn10B/QK10B	DQ5B	DQSn2B/QK2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B73p	DIFFOUT_B73p	AT21	DQS10B/CQ10B/CQn10B/QKn10B	DQ5B	DQS2B/CQ2B/CQn2B/QKn2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B74n	DIFFOUT_B74n	AG22				
3D	VREFB3DN0	IO			DIFFIO_TX_B74p	DIFFOUT_B74p	AH22	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AT20	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AU20	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	VREFB3DN0				AJ21				
3D	VREFB3DN0	IO					AK21	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AU19	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AV19	DQ10B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AM21				
3D	VREFB3DN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AN21	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AE21	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AF21	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B79n	DIFFOUT_B79n	AD21				
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B79p	DIFFOUT_B79p	AC22	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B80n	DIFFOUT_B80n	AG21	DQSn11B/QK11B	DQSn5B/QK5B	DQ2B	
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B80p	DIFFOUT_B80p	AH21	DQS11B/CQ11B/CQn11B/QKn11B	DQS5B/CQ5B/CQn5B/QKn5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AN20				
3D	VREFB3DN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AP20	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AC21	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AD20	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO			DIFFIO_TX_B83n	DIFFOUT_B83n	AG20				
3D	VREFB3DN0	IO			DIFFIO_TX_B83p	DIFFOUT_B83p	AH20	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AK20	DQ11B	DQ5B	DQ2B	
3D	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AL20	DQ11B	DQ5B	DQ2B	
		VCCD_FPLL					AB20				
		VCCA_FPLL					AB21				
		DNU					AE20				
4D	VREFB4DN0	IO			DIFFIO_TX_B85n	DIFFOUT_B85n	AV18				
4D	VREFB4DN0	IO			DIFFIO_TX_B85p	DIFFOUT_B85p	AW18	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B86n	DIFFOUT_B86n	AG19	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B86p	DIFFOUT_B86p	AH19	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_TX_B87n	DIFFOUT_B87n	AN19				
4D	VREFB4DN0	IO			DIFFIO_TX_B87p	DIFFOUT_B87p	AP19	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B88n	DIFFOUT_B88n	AK19	DQSn12B/QK12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B88p	DIFFOUT_B88p	AL19	DQS12B/CQ12B/CQn12B/QKn12B			
4D	VREFB4DN0	IO			DIFFIO_TX_B89n	DIFFOUT_B89n	AH18				
4D	VREFB4DN0	IO			DIFFIO_TX_B89p	DIFFOUT_B89p	AJ18	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AU18	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AT19	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_TX_B91n	DIFFOUT_B91n	AE19				
4D	VREFB4DN0	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AF19	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B92n	DIFFOUT_B92n	AW17	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_RX_B92p	DIFFOUT_B92p	AW16	DQ12B			
4D	VREFB4DN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AK17				CS#_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AL17	DQ13B	DQ6B		CS#_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AT17	DQ13B	DQ6B		
4D	VREFB4DN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AU17	DQ13B	DQ6B		A_4D_15
4D	VREFB4DN0	IO			DIFFIO_TX_B95n	DIFFOUT_B95n	AC19				ODT_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B95p	DIFFOUT_B95p	AD19	DQ13B	DQ6B		ODT_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B96n	DIFFOUT_B96n	AP18	DQSn13B/QK13B	DQ6B		WE#_4D
4D	VREFB4DN0	IO			DIFFIO_RX_B96p	DIFFOUT_B96p	AR18	DQS13B/CQ13B/CQn13B/QKn13B	DQ6B		CAS#_4D
4D	VREFB4DN0	IO			DIFFIO_TX_B97n	DIFFOUT_B97n	AD17				RAS#_4D
4D	VREFB4DN0	IO			DIFFIO_TX_B97p	DIFFOUT_B97p	AC18	DQ13B	DQ6B		BA_4D_2
4D	VREFB4DN0	IO			DIFFIO_RX_B98n	DIFFOUT_B98n	AD18	DQ13B	DQ6B		BA_4D_1
4D	VREFB4DN0	IO			DIFFIO_RX_B98p	DIFFOUT_B98p	AE18	DQ13B	DQ6B		BA_4D_0
4D	VREFB4DN0	IO	VREFB4DN0				AF18				
4D	VREFB4DN0	IO					AG18	DQ13B	DQ6B		A_4D_14
4D	VREFB4DN0	IO			DIFFIO_RX_B99n	DIFFOUT_B99n	AL18	DQ13B	DQ6B		A_4D_13
4D	VREFB4DN0	IO			DIFFIO_RX_B99p	DIFFOUT_B99p	AM18	DQ13B	DQ6B		A_4D_12
4D	VREFB4DN0	IO			DIFFIO_TX_B100n	DIFFOUT_B100n	AG17				A_4D_11
4D	VREFB4DN0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AH17	DQ14B	DQ6B		A_4D_10
4D	VREFB4DN0	IO			DIFFIO_RX_B101n	DIFFOUT_B101n	AN17	DQ14B	DQ6B		A_4D_9
4D	VREFB4DN0	IO			DIFFIO_RX_B101p	DIFFOUT_B101p	AP17	DQ14B	DQ6B		A_4D_8
4D	VREFB4DN0	IO			DIFFIO_TX_B102n	DIFFOUT_B102n	AR16				A_4D_7
4D	VREFB4DN0	IO			DIFFIO_TX_B102p	DIFFOUT_B102p	AT16	DQ14B	DQ6B		A_4D_6
4D	VREFB4DN0	IO			DIFFIO_RX_B103n	DIFFOUT_B103n	AU16	DQSn14B/QK14B	DQSn6B/QK6B		A_4D_5

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
4D	VREFB4DN0	IO			DIFFIO_RX_B103p	DIFFOUT_B103p	AV16	DQS14B/CQ14B/CQn14B/QKn14B	DQS6B/CQ6B/CQn6B/QKn6B		A_4D_4
4D	VREFB4DN0	IO			DIFFIO_TX_B104n	DIFFOUT_B104n	AJ16				A_4D_3
4D	VREFB4DN0	IO			DIFFIO_TX_B104p	DIFFOUT_B104p	AK16	DQ14B	DQ6B		A_4D_2
4D	VREFB4DN0	IO			DIFFIO_RX_B105n	DIFFOUT_B105n	AN16	DQ14B	DQ6B		A_4D_1
4D	VREFB4DN0	IO			DIFFIO_RX_B105p	DIFFOUT_B105p	AP16	DQ14B	DQ6B		A_4D_0
4D	VREFB4DN0	IO			DIFFIO_TX_B106n	DIFFOUT_B106n	AL16				CKE_4D_1
4D	VREFB4DN0	IO			DIFFIO_TX_B106p	DIFFOUT_B106p	AM16	DQ14B	DQ6B		CKE_4D_0
4D	VREFB4DN0	IO			DIFFIO_RX_B107n	DIFFOUT_B107n	AE17	DQ14B	DQ6B		CK#_4D
4D	VREFB4DN0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AF16	DQ14B	DQ6B		CK_4D
4C	VREFB4CN0	IO			DIFFIO_TX_B108n	DIFFOUT_B108n	AN15				RESET#_4D
4C	VREFB4CN0	IO			DIFFIO_TX_B108p	DIFFOUT_B108p	AP15	DQ15B	DQ7B	DQ3B	DQ1_4C_8
4C	VREFB4CN0	IO			DIFFIO_RX_B109n	DIFFOUT_B109n	AW14	DQ15B	DQ7B	DQ3B	DQ1_4C_7
4C	VREFB4CN0	IO			DIFFIO_RX_B109p	DIFFOUT_B109p	AW15	DQ15B	DQ7B	DQ3B	DQ1_4C_6
4C	VREFB4CN0	IO			DIFFIO_TX_B110n	DIFFOUT_B110n	AC16				
4C	VREFB4CN0	IO			DIFFIO_TX_B110p	DIFFOUT_B110p	AD16	DQ15B	DQ7B	DQ3B	DM1_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B111n	DIFFOUT_B111n	AG16	DQSn15B/QK15B	DQ7B	DQ3B	DQS#1_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B111p	DIFFOUT_B111p	AH16	DQS15B/CQ15B/CQn15B/QKn15B	DQ7B	DQ3B	DQS1_4C
4C	VREFB4CN0	IO			DIFFIO_TX_B112n	DIFFOUT_B112n	AK15				
4C	VREFB4CN0	IO			DIFFIO_TX_B112p	DIFFOUT_B112p	AL15	DQ15B	DQ7B	DQ3B	DQ1_4C_5
4C	VREFB4CN0	IO			DIFFIO_RX_B113n	DIFFOUT_B113n	AV13	DQ15B	DQ7B	DQ3B	DQ1_4C_4
4C	VREFB4CN0	IO			DIFFIO_RX_B113p	DIFFOUT_B113p	AW13	DQ15B	DQ7B	DQ3B	DQ1_4C_3
4C	VREFB4CN0	IO	VREFB4CN0				AG15				
4C	VREFB4CN0	IO					AH15	DQ15B	DQ7B	DQ3B	DQ1_4C_2
4C	VREFB4CN0	IO			DIFFIO_RX_B114n	DIFFOUT_B114n	AT15	DQ15B	DQ7B	DQ3B	DQ1_4C_1
4C	VREFB4CN0	IO			DIFFIO_RX_B114p	DIFFOUT_B114p	AU15	DQ15B	DQ7B	DQ3B	DQ1_4C_0
4C	VREFB4CN0	IO			DIFFIO_TX_B115n	DIFFOUT_B115n	AC15				
4C	VREFB4CN0	IO			DIFFIO_TX_B115p	DIFFOUT_B115p	AD14	DQ16B	DQ7B	DQ3B	DQ2_4C_8
4C	VREFB4CN0	IO			DIFFIO_RX_B116n	DIFFOUT_B116n	AT14	DQ16B	DQ7B	DQ3B	DQ2_4C_7
4C	VREFB4CN0	IO			DIFFIO_RX_B116p	DIFFOUT_B116p	AU14	DQ16B	DQ7B	DQ3B	DQ2_4C_6
4C	VREFB4CN0	IO			DIFFIO_TX_B117n	DIFFOUT_B117n	AT13				
4C	VREFB4CN0	IO			DIFFIO_TX_B117p	DIFFOUT_B117p	AU13	DQ16B	DQ7B	DQ3B	DM2_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B118n	DIFFOUT_B118n	AE16	DQSn16B/QK16B	DQSn7B/QK7B	DQ3B	DQS#2_4C
4C	VREFB4CN0	IO			DIFFIO_RX_B118p	DIFFOUT_B118p	AF15	DQS16B/CQ16B/CQn16B/QKn16B	DQS7B/CQ7B/CQn7B/QKn7B	DQ3B	DQS2_4C
4C	VREFB4CN0	IO			DIFFIO_TX_B119n	DIFFOUT_B119n	AK14				
4C	VREFB4CN0	IO			DIFFIO_TX_B119p	DIFFOUT_B119p	AL14	DQ16B	DQ7B	DQ3B	DQ2_4C_5
4C	VREFB4CN0	IO			DIFFIO_RX_B120n	DIFFOUT_B120n	AN14	DQ16B	DQ7B	DQ3B	DQ2_4C_4
4C	VREFB4CN0	IO			DIFFIO_RX_B120p	DIFFOUT_B120p	AP14	DQ16B	DQ7B	DQ3B	DQ2_4C_3
4C	VREFB4CN0	IO			DIFFIO_TX_B121n	DIFFOUT_B121n	AG14				
4C	VREFB4CN0	IO			DIFFIO_TX_B121p	DIFFOUT_B121p	AH14	DQ16B	DQ7B	DQ3B	DQ2_4C_2
4C	VREFB4CN0	IO			DIFFIO_RX_B122n	DIFFOUT_B122n	AD15	DQ16B	DQ7B	DQ3B	DQ2_4C_1
4C	VREFB4CN0	IO			DIFFIO_RX_B122p	DIFFOUT_B122p	AE15	DQ16B	DQ7B	DQ3B	DQ2_4C_0
4B	VREFB4BN0	IO			DIFFIO_TX_B123n	DIFFOUT_B123n	AP13				
4B	VREFB4BN0	IO			DIFFIO_TX_B123p	DIFFOUT_B123p	AR13	DQ17B	DQ8B	DQ3B	DQ3_4B_8
4B	VREFB4BN0	IO			DIFFIO_RX_B124n	DIFFOUT_B124n	AE14	DQ17B	DQ8B	DQ3B	DQ3_4B_7
4B	VREFB4BN0	IO			DIFFIO_RX_B124p	DIFFOUT_B124p	AE13	DQ17B	DQ8B	DQ3B	DQ3_4B_6
4B	VREFB4BN0	IO			DIFFIO_TX_B125n	DIFFOUT_B125n	AT12				
4B	VREFB4BN0	IO			DIFFIO_TX_B125p	DIFFOUT_B125p	AU12	DQ17B	DQ8B	DQ3B	DM3_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B126n	DIFFOUT_B126n	AV12	DQSn17B/QK17B	DQ8B	DQSn3B/QK3B	DQS#3_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B126p	DIFFOUT_B126p	AW12	DQS17B/CQ17B/CQn17B/QKn17B	DQ8B	DQS3B/CQ3B/CQn3B/QKn3B	DQS3_4B
4B	VREFB4BN0	IO			DIFFIO_TX_B127n	DIFFOUT_B127n	AL13				
4B	VREFB4BN0	IO			DIFFIO_TX_B127p	DIFFOUT_B127p	AM13	DQ17B	DQ8B	DQ3B	DQ3_4B_5
4B	VREFB4BN0	IO			DIFFIO_RX_B128n	DIFFOUT_B128n	AW10	DQ17B	DQ8B	DQ3B	DQ3_4B_4
4B	VREFB4BN0	IO			DIFFIO_RX_B128p	DIFFOUT_B128p	AW11	DQ17B	DQ8B	DQ3B	DQ3_4B_3
4B	VREFB4BN0	IO			DIFFIO_TX_B129n	DIFFOUT_B129n	AN12				
4B	VREFB4BN0	IO			DIFFIO_TX_B129p	DIFFOUT_B129p	AP12	DQ17B	DQ8B	DQ3B	DQ3_4B_2
4B	VREFB4BN0	IO			DIFFIO_RX_B130n	DIFFOUT_B130n	AH13	DQ17B	DQ8B	DQ3B	DQ3_4B_1
4B	VREFB4BN0	IO			DIFFIO_RX_B130p	DIFFOUT_B130p	AJ13	DQ17B	DQ8B	DQ3B	DQ3_4B_0
4B	VREFB4BN0	IO			DIFFIO_TX_B131n	DIFFOUT_B131n	AH12				
4B	VREFB4BN0	IO			DIFFIO_TX_B131p	DIFFOUT_B131p	AJ12	DQ18B	DQ8B	DQ3B	DQ4_4B_8
4B	VREFB4BN0	IO			DIFFIO_RX_B132n	DIFFOUT_B132n	AF13	DQ18B	DQ8B	DQ3B	DQ4_4B_7
4B	VREFB4BN0	IO			DIFFIO_RX_B132p	DIFFOUT_B132p	AG13	DQ18B	DQ8B	DQ3B	DQ4_4B_6
4B	VREFB4BN0	IO			DIFFIO_TX_B133n	DIFFOUT_B133n	AU10				
4B	VREFB4BN0	IO			DIFFIO_TX_B133p	DIFFOUT_B133p	AV10	DQ18B	DQ8B	DQ3B	DM4_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B134n	DIFFOUT_B134n	AT11	DQSn18B/QK18B	DQSn8B/QK8B	DQ3B	DQS#4_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B134p	DIFFOUT_B134p	AU11	DQS18B/CQ18B/CQn18B/QKn18B	DQS8B/CQ8B/CQn8B/QKn8B	DQ3B	DQS4_4B
4B	VREFB4BN0	IO			DIFFIO_TX_B135n	DIFFOUT_B135n	AK12				
4B	VREFB4BN0	IO			DIFFIO_TX_B135p	DIFFOUT_B135p	AL12	DQ18B	DQ8B	DQ3B	DQ4_4B_5
4B	VREFB4BN0	IO			DIFFIO_RX_B136n	DIFFOUT_B136n	AC13	DQ18B	DQ8B	DQ3B	DQ4_4B_4
4B	VREFB4BN0	IO			DIFFIO_RX_B136p	DIFFOUT_B136p	AD13	DQ18B	DQ8B	DQ3B	DQ4_4B_3
4B	VREFB4BN0	IO	VREFB4BN0				AN11				
4B	VREFB4BN0	IO					AP11	DQ18B	DQ8B	DQ3B	DQ4_4B_2
4B	VREFB4BN0	IO			DIFFIO_RX_B137n	DIFFOUT_B137n	AV9	DQ18B	DQ8B	DQ3B	DQ4_4B_1
4B	VREFB4BN0	IO			DIFFIO_RX_B137p	DIFFOUT_B137p	AW9	DQ18B	DQ8B	DQ3B	DQ4_4B_0
4B	VREFB4BN0	IO			DIFFIO_TX_B138n	DIFFOUT_B138n	AC12				
4B	VREFB4BN0	IO			DIFFIO_TX_B138p	DIFFOUT_B138p	AD11	DQ19B	DQ9B	DQ4B	DQ5_4B_8
4B	VREFB4BN0	IO			DIFFIO_RX_B139n	DIFFOUT_B139n	AF12	DQ19B	DQ9B	DQ4B	DQ5_4B_7
4B	VREFB4BN0	IO			DIFFIO_RX_B139p	DIFFOUT_B139p	AG12	DQ19B	DQ9B	DQ4B	DQ5_4B_6
4B	VREFB4BN0	IO			DIFFIO_TX_B140n	DIFFOUT_B140n	AT9				
4B	VREFB4BN0	IO			DIFFIO_TX_B140p	DIFFOUT_B140p	AU9	DQ19B	DQ9B	DQ4B	DM5_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B141n	DIFFOUT_B141n	AG11	DQSn19B/QK19B	DQ9B	DQ4B	DQS#5_4B
4B	VREFB4BN0	IO			DIFFIO_RX_B141p	DIFFOUT_B141p	AH11	DQS19B/CQ19B/CQn19B/QKn19B	DQ9B	DQ4B	DQS5_4B
4B	VREFB4BN0	IO			DIFFIO_TX_B142n	DIFFOUT_B142n	AD12				
4B	VREFB4BN0	IO			DIFFIO_TX_B142p	DIFFOUT_B142p	AE12	DQ19B	DQ9B	DQ4B	DQ5_4B_5
4B	VREFB4BN0	IO			DIFFIO_RX_B143n	DIFFOUT_B143n	AP10	DQ19B	DQ9B	DQ4B	DQ5_4B_4
4B	VREFB4BN0	IO			DIFFIO_RX_B143p	DIFFOUT_B143p	AR10	DQ19B	DQ9B	DQ4B	DQ5_4B_3
4B	VREFB4BN0	IO			DIFFIO_TX_B144n	DIFFOUT_B144n	AK11				
4B	VREFB4BN0	IO			DIFFIO_TX_B144p	DIFFOUT_B144p	AL11	DQ19B	DQ9B	DQ4B	DQ5_4B_2
4B	VREFB4BN0	IO			DIFFIO_RX_B145n	DIFFOUT_B145n	AL10	DQ19B	DQ9B	DQ4B	DQ5_4B_1
4B	VREFB4BN0	IO			DIFFIO_RX_B145p	DIFFOUT_B145p	AM10	DQ19B	DQ9B	DQ4B	DQ5_4B_0
4A	VREFB4AN0	IO			DIFFIO_TX_B146n	DIFFOUT_B146n	AL9				
4A	VREFB4AN0	IO			DIFFIO_TX_B146p	DIFFOUT_B146p	AM9	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B147n	DIFFOUT_B147n	AW7	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B147p	DIFFOUT_B147p	AW8	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B148n	DIFFOUT_B148n	AV7				
4A	VREFB4AN0	IO			DIFFIO_TX_B148p	DIFFOUT_B148p	AV6	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B149n	DIFFOUT_B149n	AW6	DQSn20B/QK20B	DQSn9B/QK9B	DQ4B	

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
4A	VREFB4AN0	IO			DIFFIO_RX_B149p	DIFFOUT_B149p	AW5	DQS20B/CQ20B/CQn20B/QKn20B	DQS9B/CQ9B/CQn9B/QKn9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B150n	DIFFOUT_B150n	AK9				
4A	VREFB4AN0	IO			DIFFIO_TX_B150p	DIFFOUT_B150p	AK10	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B151n	DIFFOUT_B151n	AU7	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B151p	DIFFOUT_B151p	AU8	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B152n	DIFFOUT_B152n	AN9				
4A	VREFB4AN0	IO			DIFFIO_TX_B152p	DIFFOUT_B152p	AP9	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B153n	DIFFOUT_B153n	AT8	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_RX_B153p	DIFFOUT_B153p	AR9	DQ20B	DQ9B	DQ4B	
4A	VREFB4AN0	IO		DATA10	DIFFIO_TX_B154n	DIFFOUT_B154n	AH10				
4A	VREFB4AN0	IO		DATA11	DIFFIO_TX_B154p	DIFFOUT_B154p	AJ10	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B155n	DIFFOUT_B155n	AF10	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO		DATA6	DIFFIO_RX_B155p	DIFFOUT_B155p	AE11	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO		DATA12	DIFFIO_TX_B156n	DIFFOUT_B156n	AK6				
4A	VREFB4AN0	IO		DATA13	DIFFIO_TX_B156p	DIFFOUT_B156p	AL6	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO		DATA7	DIFFIO_RX_B157n	DIFFOUT_B157n	AH6	DQSn21B/QK21B	DQ10B	DQSn4B/QK4B	
4A	VREFB4AN0	IO		DATA8	DIFFIO_RX_B157p	DIFFOUT_B157p	AJ6	DQS21B/CQ21B/CQn21B/QKn21B	DQ10B	DQS4B/CQ4B/CQn4B/QKn4B	
4A	VREFB4AN0	IO		DATA14	DIFFIO_TX_B158n	DIFFOUT_B158n	AH9				
4A	VREFB4AN0	IO		DATA15	DIFFIO_TX_B158p	DIFFOUT_B158p	AJ9	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO		DATA9	DIFFIO_RX_B159n	DIFFOUT_B159n	AM6	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO		CLKUSR	DIFFIO_RX_B159p	DIFFOUT_B159p	AN6	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	VREFB4AN0				AH7				
4A	VREFB4AN0	IO					AH8	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	CLK11n		DIFFIO_RX_B160n	DIFFOUT_B160n	AJ7	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	CLK11p		DIFFIO_RX_B160p	DIFFOUT_B160p	AK7	DQ21B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B161n	DIFFOUT_B161n	AL7				
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B161p	DIFFOUT_B161p	AM7	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B162n	DIFFOUT_B162n	AN8	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B162p	DIFFOUT_B162p	AP8	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B163n	DIFFOUT_B163n	AT6				
4A	VREFB4AN0	IO			DIFFIO_TX_B163p	DIFFOUT_B163p	AU6	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	CLK10n		DIFFIO_RX_B164n	DIFFOUT_B164n	AR7	DQSn22B/QK22B		DQSn10B/QK10B	DQ4B
4A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B164p	DIFFOUT_B164p	AT7	DQS22B/CQ22B/CQn22B/QKn22B		DQS10B/CQ10B/CQn10B/QKn10B	DQ4B
4A	VREFB4AN0	IO			DIFFIO_TX_B165n	DIFFOUT_B165n	AK8				
4A	VREFB4AN0	IO			DIFFIO_TX_B165p	DIFFOUT_B165p	AL8	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	CLK9n		DIFFIO_RX_B166n	DIFFOUT_B166n	AV4	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	CLK9p		DIFFIO_RX_B166p	DIFFOUT_B166p	AW4	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO			DIFFIO_TX_B167n	DIFFOUT_B167n	AN7				
4A	VREFB4AN0	IO	RZQ_1		DIFFIO_TX_B167p	DIFFOUT_B167p	AP7	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	CLK8n		DIFFIO_RX_B168n	DIFFOUT_B168n	AP6	DQ22B	DQ10B	DQ4B	
4A	VREFB4AN0	IO	CLK8p		DIFFIO_RX_B168p	DIFFOUT_B168p	AR6	DQ22B	DQ10B	DQ4B	
		RREF_BR					AW2				
		DNU					AV3				
		DNU					AW3				
GXB_R0		REFCLK0Rp					AF8				
GXB_R0		REFCLK0Rn					AF7				
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AU2				
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AU1				
GXB_R0		GXB_TX_R0p					AT3				
GXB_R0		GXB_TX_R0n					AT4				
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AR2				
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AR1				
GXB_R0		GXB_TX_R1p					AP3				
GXB_R0		GXB_TX_R1n					AP4				
GXB_R0		GXB_RX_R2n,GXB_REFCLK_R2n					AN2				
GXB_R0		GXB_RX_R2p,GXB_REFCLK_R2p					AN1				
GXB_R0		GXB_TX_R2p					AM3				
GXB_R0		GXB_TX_R2n					AM4				
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AL2				
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AL1				
GXB_R0		GXB_TX_R3p					AK3				
GXB_R0		GXB_TX_R3n					AK4				
GXB_R0		GXB_RX_R4n,GXB_REFCLK_R4n					AJ2				
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p					AJ1				
GXB_R0		GXB_TX_R4p					AH3				
GXB_R0		GXB_TX_R4n					AH4				
GXB_R0		GXB_RX_R5n,GXB_REFCLK_R5n					AG2				
GXB_R0		GXB_RX_R5p,GXB_REFCLK_R5p					AG1				
GXB_R0		GXB_TX_R5p					AF3				
GXB_R0		GXB_TX_R5n					AF4				
GXB_R0		REFCLK1Rp					AD9				
GXB_R0		REFCLK1Rn					AD8				
GXB_R1		REFCLK2Rp					AB9				
GXB_R1		REFCLK2Rn					AB8				
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					AE2				
GXB_R1		GXB_RX_R6p,GXB_REFCLK_R6p					AE1				
GXB_R1		GXB_TX_R6p					AD3				
GXB_R1		GXB_TX_R6n					AD4				
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					AC2				
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					AC1				
GXB_R1		GXB_TX_R7p					AB3				
GXB_R1		GXB_TX_R7n					AB4				
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					AA2				
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					AA1				
GXB_R1		GXB_TX_R8p					Y3				
GXB_R1		GXB_TX_R8n					Y4				
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					W2				
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					W1				
GXB_R1		GXB_TX_R9p					V3				
GXB_R1		GXB_TX_R9n					V4				
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					U2				
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					U1				
GXB_R1		GXB_TX_R10p					T3				
GXB_R1		GXB_TX_R10n					T4				
GXB_R1		GXB_RX_R11n,GXB_REFCLK_R11n					R2				
GXB_R1		GXB_RX_R11p,GXB_REFCLK_R11p					R1				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
GXB_R1		GXB_TX_R11p					P3				
GXB_R1		GXB_TX_R11n					P4				
GXB_R1		REFCLK3Rp					Y9				
GXB_R1		REFCLK3Rn					Y8				
		DNU					C5				
7A		GND					N6				
7A	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	C6	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK12n		DIFFIO_RX_T1n	DIFFOUT_T1n	D6	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	RZQ_5		DIFFIO_TX_T2p	DIFFOUT_T2p	F6	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	G6				
7A	VREFB7AN0	IO	CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	A6	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	B6	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	F7	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	G7				
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	E6	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T	DQ1T	
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	E7	DQSn1T/QK1T	DQSn1T/QK1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	C7	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	D7				
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	F8	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	G8	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	J8	DQ1T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	K8				
7A	VREFB7AN0	IO	CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	H6	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	J6	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO					K7	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO	VREFB7AN0				J7				
7A	VREFB7AN0	IO		DEV_OE	DIFFIO_RX_T10p	DIFFOUT_T10p	K6	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	L6	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO		nPERSTR0	DIFFIO_TX_T11p	DIFFOUT_T11p	M8	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO		nPERSTL0	DIFFIO_TX_T11n	DIFFOUT_T11n	N9				
7A	VREFB7AN0	IO		CvP_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	P10	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	DQS1T/CQ1T/CQn1T/QKn1T	
7A	VREFB7AN0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	P9	DQSn2T/QK2T	DQ1T	DQSn1T/QK1T	
7A	VREFB7AN0	IO		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	L7	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	M6				
7A	VREFB7AN0	IO		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	M7	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	N7	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	L10	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	IO		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	M10				
7A	VREFB7AN0	IO			DIFFIO_RX_T16p	DIFFOUT_T16p	D9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_RX_T16n	DIFFOUT_T16n	E9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T17p	DIFFOUT_T17p	F9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T17n	DIFFOUT_T17n	G9				
7A	VREFB7AN0	IO			DIFFIO_RX_T18p	DIFFOUT_T18p	C8	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_RX_T18n	DIFFOUT_T18n	D8	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T19p	DIFFOUT_T19p	K9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T19n	DIFFOUT_T19n	L9				
7A	VREFB7AN0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	A7	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	B7	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T21p	DIFFOUT_T21p	B9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T21n	DIFFOUT_T21n	C9				
7A	VREFB7AN0	IO			DIFFIO_RX_T22p	DIFFOUT_T22p	A9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_RX_T22n	DIFFOUT_T22n	A8	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T23p	DIFFOUT_T23p	H9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T23n	DIFFOUT_T23n	J9				
7B	VREFB7BN0	IO			DIFFIO_RX_T24p	DIFFOUT_T24p	E10	DQ4T	DQ2T	DQ1T	DQ5_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T24n	DIFFOUT_T24n	F10	DQ4T	DQ2T	DQ1T	DQ5_7B_1
7B	VREFB7BN0	IO			DIFFIO_TX_T25p	DIFFOUT_T25p	N10	DQ4T	DQ2T	DQ1T	DQ5_7B_2
7B	VREFB7BN0	IO			DIFFIO_TX_T25n	DIFFOUT_T25n	M11				
7B	VREFB7BN0	IO			DIFFIO_RX_T26p	DIFFOUT_T26p	B10	DQ4T	DQ2T	DQ1T	DQ5_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	C10	DQ4T	DQ2T	DQ1T	DQ5_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T27p	DIFFOUT_T27p	H10	DQ4T	DQ2T	DQ1T	DQ5_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T27n	DIFFOUT_T27n	J10				
7B	VREFB7BN0	IO			DIFFIO_RX_T28p	DIFFOUT_T28p	P12	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQ1T	DQS5_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	R12	DQSn4T/QK4T	DQ2T	DQ1T	DQS#5_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T29p	DIFFOUT_T29p	R11	DQ4T	DQ2T	DQ1T	DM5_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T29n	DIFFOUT_T29n	T11				
7B	VREFB7BN0	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	A11	DQ4T	DQ2T	DQ1T	DQ5_7B_6
7B	VREFB7BN0	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	A10	DQ4T	DQ2T	DQ1T	DQ5_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T31p	DIFFOUT_T31p	J11	DQ4T	DQ2T	DQ1T	DQ5_7B_8
7B	VREFB7BN0	IO			DIFFIO_TX_T31n	DIFFOUT_T31n	K11				
7B	VREFB7BN0	IO			DIFFIO_RX_T32p	DIFFOUT_T32p	M12	DQ5T	DQ3T	DQ2T	DQ4_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	N12	DQ5T	DQ3T	DQ2T	DQ4_7B_1
7B	VREFB7BN0	IO					F11	DQ5T	DQ3T	DQ2T	DQ4_7B_2
7B	VREFB7BN0	IO	VREFB7BN0				G11				
7B	VREFB7BN0	IO			DIFFIO_RX_T33p	DIFFOUT_T33p	C11	DQ5T	DQ3T	DQ2T	DQ4_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T33n	DIFFOUT_T33n	D11	DQ5T	DQ3T	DQ2T	DQ4_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	K12	DQ5T	DQ3T	DQ2T	DQ4_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	L12				
7B	VREFB7BN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D12	DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ2T	DQS4_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	E12	DQSn5T/QK5T	DQSn3T/QK3T	DQ2T	DQS#4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	F12	DQ5T	DQ3T	DQ2T	DM4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	G12				
7B	VREFB7BN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	P13	DQ5T	DQ3T	DQ2T	DQ4_7B_6
7B	VREFB7BN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	R13	DQ5T	DQ3T	DQ2T	DQ4_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	H12	DQ5T	DQ3T	DQ2T	DQ4_7B_8
7B	VREFB7BN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	J12				
7B	VREFB7BN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	B12	DQ6T	DQ3T	DQ2T	DQ3_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	C12	DQ6T	DQ3T	DQ2T	DQ3_7B_1
7B	VREFB7BN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	M13	DQ6T	DQ3T	DQ2T	DQ3_7B_2
7B	VREFB7BN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	N13				
7B	VREFB7BN0	IO			DIFFIO_RX_T41p	DIFFOUT_T41p	A13	DQ6T	DQ3T	DQ2T	DQ3_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T41n	DIFFOUT_T41n	A12	DQ6T	DQ3T	DQ2T	DQ3_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	J13	DQ6T	DQ3T	DQ2T	DQ3_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	K13				
7B	VREFB7BN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D13	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQS2T/CQ2T/CQn2T/QKn2T	DQS3_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	E13	DQSn6T/QK6T	DQ3T	DQSn2T/QK2T	DQS#3_7B

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
7B	VREFB7BN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	A14	DQ6T	DQ3T	DQ2T	DM3_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	B13				
7B	VREFB7BN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	C14	DQ6T	DQ3T	DQ2T	DQ3_7B_6
7B	VREFB7BN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	D14	DQ6T	DQ3T	DQ2T	DQ3_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	G13	DQ6T	DQ3T	DQ2T	DQ3_7B_8
7B	VREFB7BN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	H13				
7C	VREFB7CN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	R14	DQ7T	DQ4T	DQ2T	DQ2_7C_0
7C	VREFB7CN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	T14	DQ7T	DQ4T	DQ2T	DQ2_7C_1
7C	VREFB7CN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	M14	DQ7T	DQ4T	DQ2T	DQ2_7C_2
7C	VREFB7CN0	IO			DIFFIO_TX_T48n	DIFFOUT_T48n	N14				
7C	VREFB7CN0	IO			DIFFIO_RX_T49p	DIFFOUT_T49p	F14	DQ7T	DQ4T	DQ2T	DQ2_7C_3
7C	VREFB7CN0	IO			DIFFIO_RX_T49n	DIFFOUT_T49n	G14	DQ7T	DQ4T	DQ2T	DQ2_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	L15	DQ7T	DQ4T	DQ2T	DQ2_7C_5
7C	VREFB7CN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	M15				
7C	VREFB7CN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	R15	DQS7T/CQ7T/CQn7T/QKn7T	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQS2_7C
7C	VREFB7CN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	T15	DQSn7T/QK7T	DQSn4T/QK4T	DQ2T	DQS#2_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T52p	DIFFOUT_T52p	N15	DQ7T	DQ4T	DQ2T	DM2_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	P15				
7C	VREFB7CN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	E15	DQ7T	DQ4T	DQ2T	DQ2_7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	F15	DQ7T	DQ4T	DQ2T	DQ2_7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	J14	DQ7T	DQ4T	DQ2T	DQ2_7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	K14				
7C	VREFB7CN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	P16	DQ8T	DQ4T	DQ2T	DQ1_7C_0
7C	VREFB7CN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	R16	DQ8T	DQ4T	DQ2T	DQ1_7C_1
7C	VREFB7CN0	IO					C15	DQ8T	DQ4T	DQ2T	DQ1_7C_2
7C	VREFB7CN0	IO	VREFB7CN0				D15				
7C	VREFB7CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	M16	DQ8T	DQ4T	DQ2T	DQ1_7C_3
7C	VREFB7CN0	IO			DIFFIO_RX_T56n	DIFFOUT_T56n	N16	DQ8T	DQ4T	DQ2T	DQ1_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	H15	DQ8T	DQ4T	DQ2T	DQ1_7C_5
7C	VREFB7CN0	IO			DIFFIO_TX_T57n	DIFFOUT_T57n	J15				
7C	VREFB7CN0	IO			DIFFIO_RX_T58p	DIFFOUT_T58p	G16	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T	DQ2T	DQS1_7C
7C	VREFB7CN0	IO			DIFFIO_RX_T58n	DIFFOUT_T58n	H16	DQSn8T/QK8T	DQ4T	DQ2T	DQS#1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T59p	DIFFOUT_T59p	A15	DQ8T	DQ4T	DQ2T	DM1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T59n	DIFFOUT_T59n	B15				
7C	VREFB7CN0	IO			DIFFIO_RX_T60p	DIFFOUT_T60p	D16	DQ8T	DQ4T	DQ2T	DQ1_7C_6
7C	VREFB7CN0	IO			DIFFIO_RX_T60n	DIFFOUT_T60n	E16	DQ8T	DQ4T	DQ2T	DQ1_7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T61p	DIFFOUT_T61p	J16	DQ8T	DQ4T	DQ2T	DQ1_7C_8
7C	VREFB7CN0	IO			DIFFIO_TX_T61n	DIFFOUT_T61n	K16				RESET#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T62p	DIFFOUT_T62p	N18	DQ9T	DQ5T		CK_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T62n	DIFFOUT_T62n	P18	DQ9T	DQ5T		CK#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T63p	DIFFOUT_T63p	M17	DQ9T	DQ5T		CKE_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T63n	DIFFOUT_T63n	N17				CKE_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T64p	DIFFOUT_T64p	B16	DQ9T	DQ5T		A_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T64n	DIFFOUT_T64n	C16	DQ9T	DQ5T		A_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T65p	DIFFOUT_T65p	J17	DQ9T	DQ5T		A_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T65n	DIFFOUT_T65n	K17				A_7D_3
7D	VREFB7DN0	IO			DIFFIO_RX_T66p	DIFFOUT_T66p	F17	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T		A_7D_4
7D	VREFB7DN0	IO			DIFFIO_RX_T66n	DIFFOUT_T66n	G17	DQSn9T/QK9T	DQSn5T/QK5T		A_7D_5
7D	VREFB7DN0	IO			DIFFIO_TX_T67p	DIFFOUT_T67p	R17	DQ9T	DQ5T		A_7D_6
7D	VREFB7DN0	IO			DIFFIO_TX_T67n	DIFFOUT_T67n	T17				A_7D_7
7D	VREFB7DN0	IO			DIFFIO_RX_T68p	DIFFOUT_T68p	C17	DQ9T	DQ5T		A_7D_8
7D	VREFB7DN0	IO			DIFFIO_RX_T68n	DIFFOUT_T68n	D17	DQ9T	DQ5T		A_7D_9
7D	VREFB7DN0	IO			DIFFIO_TX_T69p	DIFFOUT_T69p	K18	DQ9T	DQ5T		A_7D_10
7D	VREFB7DN0	IO			DIFFIO_TX_T69n	DIFFOUT_T69n	L18				A_7D_11
7D	VREFB7DN0	IO			DIFFIO_RX_T70p	DIFFOUT_T70p	R19	DQ10T	DQ5T		A_7D_12
7D	VREFB7DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	T19	DQ10T	DQ5T		A_7D_13
7D	VREFB7DN0	IO					R18	DQ10T	DQ5T		A_7D_14
7D	VREFB7DN0	IO	VREFB7DN0				T18				
7D	VREFB7DN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	E18	DQ10T	DQ5T		BA_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	F18	DQ10T	DQ5T		BA_7D_1
7D	VREFB7DN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	H18	DQ10T	DQ5T		BA_7D_2
7D	VREFB7DN0	IO			DIFFIO_TX_T72n	DIFFOUT_T72n	J18				RAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	N19	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T		CAS#_7D
7D	VREFB7DN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	P19	DQSn10T/QK10T	DQ5T		WE#_7D
7D	VREFB7DN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	B18	DQ10T	DQ5T		ODT_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	C18				ODT_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	A17	DQ10T	DQ5T		A_7D_15
7D	VREFB7DN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	A16	DQ10T	DQ5T		
7D	VREFB7DN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	L19	DQ10T	DQ5T		CS#_7D_0
7D	VREFB7DN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	M19				CS#_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	F19	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	G19	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	J19	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	K19				
7D	VREFB7DN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	C19	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	D19	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	J20	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	K20				
7D	VREFB7DN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	A18	DQS11T/CQ11T/CQn11T/QKn11T			
7D	VREFB7DN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	A19	DQSn11T/QK11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	R20	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	T20				
7D	VREFB7DN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	F20	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	G20	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	M20	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	N20				
		VCCA_FPLL					V20				
		VCCD_FPLL					V19				
		DNU					P21				
8D	VREFB8DN0	IO	CLK19p		DIFFIO_RX_T85p	DIFFOUT_T85p	C20	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO	CLK19n		DIFFIO_RX_T85n	DIFFOUT_T85n	D20	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T86p	DIFFOUT_T86p	M21	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T86n	DIFFOUT_T86n	N21				
8D	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T87p	DIFFOUT_T87p	G21	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO	CLK18n		DIFFIO_RX_T87n	DIFFOUT_T87n	H21	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T88p	DIFFOUT_T88p	D21	DQ12T	DQ6T	DQ3T	

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
8D	VREFB8DN0	IO			DIFFIO_TX_T88n	DIFFOUT_T88n	E21				
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T89p	DIFFOUT_T89p	A20	DQS12T/CQ12T/CQn12T/QKn12T	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T89n	DIFFOUT_T89n	B21	DQSn12T/QK12T	DQSn6T/QK6T	DQ3T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T90p	DIFFOUT_T90p	J21	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T90n	DIFFOUT_T90n	K21				
8D	VREFB8DN0	IO	CLK17p		DIFFIO_RX_T91p	DIFFOUT_T91p	A22	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO	CLK17n		DIFFIO_RX_T91n	DIFFOUT_T91n	A21	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T92p	DIFFOUT_T92p	R21	DQ12T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T92n	DIFFOUT_T92n	T21				
8D	VREFB8DN0	IO	CLK16p		DIFFIO_RX_T93p	DIFFOUT_T93p	B22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO	CLK16n		DIFFIO_RX_T93n	DIFFOUT_T93n	C22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO					J22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO	VREFB8DN0				H22				
8D	VREFB8DN0	IO			DIFFIO_RX_T94p	DIFFOUT_T94p	E22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T94n	DIFFOUT_T94n	F22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T95p	DIFFOUT_T95p	A23	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T95n	DIFFOUT_T95n	A24				
8D	VREFB8DN0	IO			DIFFIO_RX_T96p	DIFFOUT_T96p	C23	DQS13T/CQ13T/CQn13T/QKn13T	DQ6T	DQS3T/CQ3T/CQn3T/QKn3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T96n	DIFFOUT_T96n	D23	DQSn13T/QK13T	DQ6T	DQSn3T/QK3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T97p	DIFFOUT_T97p	L22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T97n	DIFFOUT_T97n	M22				
8D	VREFB8DN0	IO			DIFFIO_RX_T98p	DIFFOUT_T98p	N22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T98n	DIFFOUT_T98n	P22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T99p	DIFFOUT_T99p	R22	DQ13T	DQ6T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T99n	DIFFOUT_T99n	T22				
8D	VREFB8DN0	IO			DIFFIO_RX_T100p	DIFFOUT_T100p	F23	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T100n	DIFFOUT_T100n	G23	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T101p	DIFFOUT_T101p	R23	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T101n	DIFFOUT_T101n	T23				
8D	VREFB8DN0	IO			DIFFIO_RX_T102p	DIFFOUT_T102p	B24	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T102n	DIFFOUT_T102n	C24	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T103p	DIFFOUT_T103p	M23	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T103n	DIFFOUT_T103n	N23				
8D	VREFB8DN0	IO			DIFFIO_RX_T104p	DIFFOUT_T104p	D24	DQS14T/CQ14T/CQn14T/QKn14T	DQS7T/CQ7T/CQn7T/QKn7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T104n	DIFFOUT_T104n	E24	DQSn14T/QK14T	DQSn7T/QK7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T105p	DIFFOUT_T105p	J23	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T105n	DIFFOUT_T105n	K23				
8D	VREFB8DN0	IO			DIFFIO_RX_T106p	DIFFOUT_T106p	F24	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_RX_T106n	DIFFOUT_T106n	G24	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T107p	DIFFOUT_T107p	H24	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	IO			DIFFIO_TX_T107n	DIFFOUT_T107n	J24				
8C	VREFB8CN0	IO			DIFFIO_RX_T108p	DIFFOUT_T108p	T26	DQ15T	DQ7T	DQ3T	DQ5_8C_0
8C	VREFB8CN0	IO			DIFFIO_RX_T108n	DIFFOUT_T108n	T25	DQ15T	DQ7T	DQ3T	DQ5_8C_1
8C	VREFB8CN0	IO			DIFFIO_TX_T109p	DIFFOUT_T109p	G25	DQ15T	DQ7T	DQ3T	DQ5_8C_2
8C	VREFB8CN0	IO			DIFFIO_TX_T109n	DIFFOUT_T109n	H25				
8C	VREFB8CN0	IO			DIFFIO_RX_T110p	DIFFOUT_T110p	N24	DQ15T	DQ7T	DQ3T	DQ5_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T110n	DIFFOUT_T110n	P24	DQ15T	DQ7T	DQ3T	DQ5_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T111p	DIFFOUT_T111p	R24	DQ15T	DQ7T	DQ3T	DQ5_8C_5
8C	VREFB8CN0	IO			DIFFIO_TX_T111n	DIFFOUT_T111n	T24				
8C	VREFB8CN0	IO			DIFFIO_RX_T112p	DIFFOUT_T112p	A25	DQS15T/CQ15T/CQn15T/QKn15T	DQ7T	DQ3T	DQS5_8C
8C	VREFB8CN0	IO			DIFFIO_RX_T112n	DIFFOUT_T112n	B25	DQSn15T/QK15T	DQ7T	DQ3T	DQS#5_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T113p	DIFFOUT_T113p	K24	DQ15T	DQ7T	DQ3T	DM5_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T113n	DIFFOUT_T113n	L24				
8C	VREFB8CN0	IO			DIFFIO_RX_T114p	DIFFOUT_T114p	D25	DQ15T	DQ7T	DQ3T	DQ5_8C_6
8C	VREFB8CN0	IO			DIFFIO_RX_T114n	DIFFOUT_T114n	E25	DQ15T	DQ7T	DQ3T	DQ5_8C_7
8C	VREFB8CN0	IO			DIFFIO_TX_T115p	DIFFOUT_T115p	P25	DQ15T	DQ7T	DQ3T	DQ5_8C_8
8C	VREFB8CN0	IO			DIFFIO_TX_T115n	DIFFOUT_T115n	R25				
8C	VREFB8CN0	IO			DIFFIO_RX_T116p	DIFFOUT_T116p	C26	DQ16T	DQ8T	DQ4T	DQ4_8C_0
8C	VREFB8CN0	IO			DIFFIO_RX_T116n	DIFFOUT_T116n	D26	DQ16T	DQ8T	DQ4T	DQ4_8C_1
8C	VREFB8CN0	IO					K25	DQ16T	DQ8T	DQ4T	DQ4_8C_2
8C	VREFB8CN0	IO	VREFB8CN0				L25				
8C	VREFB8CN0	IO			DIFFIO_RX_T117p	DIFFOUT_T117p	R26	DQ16T	DQ8T	DQ4T	DQ4_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T117n	DIFFOUT_T117n	T27	DQ16T	DQ8T	DQ4T	DQ4_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T118p	DIFFOUT_T118p	A26	DQ16T	DQ8T	DQ4T	DQ4_8C_5
8C	VREFB8CN0	IO			DIFFIO_TX_T118n	DIFFOUT_T118n	A27				
8C	VREFB8CN0	IO			DIFFIO_RX_T119p	DIFFOUT_T119p	M26	DQS16T/CQ16T/CQn16T/QKn16T	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T	DQS4_8C
8C	VREFB8CN0	IO			DIFFIO_RX_T119n	DIFFOUT_T119n	N26	DQSn16T/QK16T	DQSn8T/QK8T	DQ4T	DQS#4_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T120p	DIFFOUT_T120p	J26	DQ16T	DQ8T	DQ4T	DM4_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T120n	DIFFOUT_T120n	K26				
8C	VREFB8CN0	IO			DIFFIO_RX_T121p	DIFFOUT_T121p	F26	DQ16T	DQ8T	DQ4T	DQ4_8C_6
8C	VREFB8CN0	IO			DIFFIO_RX_T121n	DIFFOUT_T121n	G26	DQ16T	DQ8T	DQ4T	DQ4_8C_7
8C	VREFB8CN0	IO			DIFFIO_TX_T122p	DIFFOUT_T122p	M25	DQ16T	DQ8T	DQ4T	DQ4_8C_8
8C	VREFB8CN0	IO			DIFFIO_TX_T122n	DIFFOUT_T122n	N25				
8C	VREFB8CN0	IO			DIFFIO_RX_T123p	DIFFOUT_T123p	P27	DQ17T	DQ8T	DQ4T	DQ3_8C_0
8C	VREFB8CN0	IO			DIFFIO_RX_T123n	DIFFOUT_T123n	R27	DQ17T	DQ8T	DQ4T	DQ3_8C_1
8C	VREFB8CN0	IO			DIFFIO_TX_T124p	DIFFOUT_T124p	H27	DQ17T	DQ8T	DQ4T	DQ3_8C_2
8C	VREFB8CN0	IO			DIFFIO_TX_T124n	DIFFOUT_T124n	J27				
8C	VREFB8CN0	IO			DIFFIO_RX_T125p	DIFFOUT_T125p	B27	DQ17T	DQ8T	DQ4T	DQ3_8C_3
8C	VREFB8CN0	IO			DIFFIO_RX_T125n	DIFFOUT_T125n	C27	DQ17T	DQ8T	DQ4T	DQ3_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	E27	DQ17T	DQ8T	DQ4T	DQ3_8C_5
8C	VREFB8CN0	IO			DIFFIO_TX_T126n	DIFFOUT_T126n	F27				
8C	VREFB8CN0	IO			DIFFIO_RX_T127p	DIFFOUT_T127p	R28	DQS17T/CQ17T/CQn17T/QKn17T	DQ8T	DQS4T/CQ4T/CQn4T/QKn4T	DQS3_8C
8C	VREFB8CN0	IO			DIFFIO_RX_T127n	DIFFOUT_T127n	T28	DQSn17T/QK17T	DQ8T	DQSn4T/QK4T	DQS#3_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T128p	DIFFOUT_T128p	K27	DQ17T	DQ8T	DQ4T	DM3_8C
8C	VREFB8CN0	IO			DIFFIO_TX_T128n	DIFFOUT_T128n	L27				
8C	VREFB8CN0	IO			DIFFIO_RX_T129p	DIFFOUT_T129p	M27	DQ17T	DQ8T	DQ4T	DQ3_8C_6
8C	VREFB8CN0	IO			DIFFIO_RX_T129n	DIFFOUT_T129n	N27	DQ17T	DQ8T	DQ4T	DQ3_8C_7
8C	VREFB8CN0	IO			DIFFIO_TX_T130p	DIFFOUT_T130p	N28	DQ17T	DQ8T	DQ4T	DQ3_8C_8
8C	VREFB8CN0	IO			DIFFIO_TX_T130n	DIFFOUT_T130n	P28				
8B	VREFB8BN0	IO			DIFFIO_RX_T131p	DIFFOUT_T131p	L28	DQ18T	DQ9T	DQ4T	DQ2_8B_0
8B	VREFB8BN0	IO			DIFFIO_RX_T131n	DIFFOUT_T131n	M28	DQ18T	DQ9T	DQ4T	DQ2_8B_1
8B	VREFB8BN0	IO			DIFFIO_TX_T132p	DIFFOUT_T132p	H28	DQ18T	DQ9T	DQ4T	DQ2_8B_2
8B	VREFB8BN0	IO			DIFFIO_TX_T132n	DIFFOUT_T132n	J28				
8B	VREFB8BN0	IO			DIFFIO_RX_T133p	DIFFOUT_T133p	C28	DQ18T	DQ9T	DQ4T	DQ2_8B_3
8B	VREFB8BN0	IO			DIFFIO_RX_T133n	DIFFOUT_T133n	D28	DQ18T	DQ9T	DQ4T	DQ2_8B_4
8B	VREFB8BN0	IO			DIFFIO_TX_T134p	DIFFOUT_T134p	F28	DQ18T	DQ9T	DQ4T	DQ2_8B_5

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
8B	VREFB8BN0	IO			DIFFIO_TX_T134n	DIFFOUT_T134n	G28				
8B	VREFB8BN0	IO			DIFFIO_RX_T135p	DIFFOUT_T135p	R29	DQS18T/CQ18T/CQn18T/QKn18T	DQS9T/CQ9T/CQn9T/QKn9T	DQ4T	DQS2_8B
8B	VREFB8BN0	IO			DIFFIO_RX_T135n	DIFFOUT_T135n	T29	DQSn18T/QK18T	DQSn9T/QK9T	DQ4T	DQS#2_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T136p	DIFFOUT_T136p	J29	DQ18T	DQ9T	DQ4T	DM2_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T136n	DIFFOUT_T136n	K29				
8B	VREFB8BN0	IO			DIFFIO_RX_T137p	DIFFOUT_T137p	M29	DQ18T	DQ9T	DQ4T	DQ2_8B_6
8B	VREFB8BN0	IO			DIFFIO_RX_T137n	DIFFOUT_T137n	N29	DQ18T	DQ9T	DQ4T	DQ2_8B_7
8B	VREFB8BN0	IO			DIFFIO_TX_T138p	DIFFOUT_T138p	F29	DQ18T	DQ9T	DQ4T	DQ2_8B_8
8B	VREFB8BN0	IO			DIFFIO_TX_T138n	DIFFOUT_T138n	G29				
8B	VREFB8BN0	IO			DIFFIO_RX_T139p	DIFFOUT_T139p	B28	DQ19T	DQ9T	DQ4T	DQ1_8B_0
8B	VREFB8BN0	IO			DIFFIO_RX_T139n	DIFFOUT_T139n	C29	DQ19T	DQ9T	DQ4T	DQ1_8B_1
8B	VREFB8BN0	IO					R30	DQ19T	DQ9T	DQ4T	DQ1_8B_2
8B	VREFB8BN0	IO	VREFB8BN0				R31				
8B	VREFB8BN0	IO			DIFFIO_RX_T140p	DIFFOUT_T140p	A29	DQ19T	DQ9T	DQ4T	DQ1_8B_3
8B	VREFB8BN0	IO			DIFFIO_RX_T140n	DIFFOUT_T140n	A28	DQ19T	DQ9T	DQ4T	DQ1_8B_4
8B	VREFB8BN0	IO			DIFFIO_TX_T141p	DIFFOUT_T141p	L30	DQ19T	DQ9T	DQ4T	DQ1_8B_5
8B	VREFB8BN0	IO			DIFFIO_TX_T141n	DIFFOUT_T141n	M30				
8B	VREFB8BN0	IO			DIFFIO_RX_T142p	DIFFOUT_T142p	N30	DQS19T/CQ19T/CQn19T/QKn19T	DQ9T	DQ4T	DQS1_8B
8B	VREFB8BN0	IO			DIFFIO_RX_T142n	DIFFOUT_T142n	P30	DQSn19T/QK19T	DQ9T	DQ4T	DQS#1_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T143p	DIFFOUT_T143p	J30	DQ19T	DQ9T	DQ4T	DM1_8B
8B	VREFB8BN0	IO			DIFFIO_TX_T143n	DIFFOUT_T143n	K30				
8B	VREFB8BN0	IO			DIFFIO_RX_T144p	DIFFOUT_T144p	D30	DQ19T	DQ9T	DQ4T	DQ1_8B_6
8B	VREFB8BN0	IO			DIFFIO_RX_T144n	DIFFOUT_T144n	D29	DQ19T	DQ9T	DQ4T	DQ1_8B_7
8B	VREFB8BN0	IO			DIFFIO_TX_T145p	DIFFOUT_T145p	F30	DQ19T	DQ9T	DQ4T	DQ1_8B_8
8B	VREFB8BN0	IO			DIFFIO_TX_T145n	DIFFOUT_T145n	G30				RESET#_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T146p	DIFFOUT_T146p	B30	DQ20T	DQ10T		CK_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T146n	DIFFOUT_T146n	C30	DQ20T	DQ10T		CK#_8A
8A	VREFB8AN0	IO			DIFFIO_TX_T147p	DIFFOUT_T147p	E31	DQ20T	DQ10T		CKE_8A_0
8A	VREFB8AN0	IO			DIFFIO_TX_T147n	DIFFOUT_T147n	F31				CKE_8A_1
8A	VREFB8AN0	IO			DIFFIO_RX_T148p	DIFFOUT_T148p	B31	DQ20T	DQ10T		A_8A_0
8A	VREFB8AN0	IO			DIFFIO_RX_T148n	DIFFOUT_T148n	A30	DQ20T	DQ10T		A_8A_1
8A	VREFB8AN0	IO			DIFFIO_TX_T149p	DIFFOUT_T149p	A31	DQ20T	DQ10T		A_8A_2
8A	VREFB8AN0	IO			DIFFIO_TX_T149n	DIFFOUT_T149n	A32				A_8A_3
8A	VREFB8AN0	IO			DIFFIO_RX_T150p	DIFFOUT_T150p	A33	DQS20T/CQ20T/CQn20T/QKn20T	DQS10T/CQ10T/CQn10T/QKn10T		A_8A_4
8A	VREFB8AN0	IO			DIFFIO_RX_T150n	DIFFOUT_T150n	B33	DQSn20T/QK20T	DQSn10T/QK10T		A_8A_5
8A	VREFB8AN0	IO			DIFFIO_TX_T151p	DIFFOUT_T151p	H31	DQ20T	DQ10T		A_8A_6
8A	VREFB8AN0	IO			DIFFIO_TX_T151n	DIFFOUT_T151n	J31				A_8A_7
8A	VREFB8AN0	IO			DIFFIO_RX_T152p	DIFFOUT_T152p	C31	DQ20T	DQ10T		A_8A_8
8A	VREFB8AN0	IO			DIFFIO_RX_T152n	DIFFOUT_T152n	D31	DQ20T	DQ10T		A_8A_9
8A	VREFB8AN0	IO			DIFFIO_TX_T153p	DIFFOUT_T153p	C32	DQ20T	DQ10T		A_8A_10
8A	VREFB8AN0	IO			DIFFIO_TX_T153n	DIFFOUT_T153n	D32				A_8A_11
8A	VREFB8AN0	IO			DIFFIO_RX_T154p	DIFFOUT_T154p	N31	DQ21T	DQ10T		A_8A_12
8A	VREFB8AN0	IO			DIFFIO_RX_T154n	DIFFOUT_T154n	P31	DQ21T	DQ10T		A_8A_13
8A	VREFB8AN0	IO			DIFFIO_TX_T155p	DIFFOUT_T155p	J32	DQ21T	DQ10T		A_8A_14
8A	VREFB8AN0	IO			DIFFIO_TX_T155n	DIFFOUT_T155n	K32				A_8A_15
8A	VREFB8AN0	IO			DIFFIO_RX_T156p	DIFFOUT_T156p	M32	DQ21T	DQ10T		BA_8A_0
8A	VREFB8AN0	IO			DIFFIO_RX_T156n	DIFFOUT_T156n	N32	DQ21T	DQ10T		BA_8A_1
8A	VREFB8AN0	IO			DIFFIO_TX_T157p	DIFFOUT_T157p	J34	DQ21T	DQ10T		BA_8A_2
8A	VREFB8AN0	IO			DIFFIO_TX_T157n	DIFFOUT_T157n	K34				RAS#_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T158p	DIFFOUT_T158p	L33	DQS21T/CQ21T/CQn21T/QKn21T	DQ10T		CAS#_8A
8A	VREFB8AN0	IO			DIFFIO_RX_T158n	DIFFOUT_T158n	M33	DQSn21T/QK21T	DQ10T		WE#_8A
8A	VREFB8AN0	IO			DIFFIO_TX_T159p	DIFFOUT_T159p	L31	DQ21T	DQ10T		ODT_8A_0
8A	VREFB8AN0	IO			DIFFIO_TX_T159n	DIFFOUT_T159n	M31				ODT_8A_1
8A	VREFB8AN0	IO	CLK23p		DIFFIO_RX_T160p	DIFFOUT_T160p	N34	DQ21T	DQ10T		
8A	VREFB8AN0	IO	CLK23n		DIFFIO_RX_T160n	DIFFOUT_T160n	N33	DQ21T	DQ10T		
8A	VREFB8AN0	IO			DIFFIO_TX_T161p	DIFFOUT_T161p	L34	DQ21T	DQ10T		CS#_8A_0
8A	VREFB8AN0	IO			DIFFIO_TX_T161n	DIFFOUT_T161n	M34				CS#_8A_1
8A	VREFB8AN0	IO	CLK22p		DIFFIO_RX_T162p	DIFFOUT_T162p	E34	DQ22T			
8A	VREFB8AN0	IO	CLK22n		DIFFIO_RX_T162n	DIFFOUT_T162n	F34	DQ22T			
8A	VREFB8AN0	IO					J33	DQ22T			
8A	VREFB8AN0	IO	VREFB8AN0				H33				
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO_RX_T163p	DIFFOUT_T163p	B34	DQ22T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT3,FPLL_TL_FBn		DIFFIO_RX_T163n	DIFFOUT_T163n	A35	DQ22T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0		DIFFIO_TX_T164p	DIFFOUT_T164p	C33	DQ22T			
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T164n	DIFFOUT_T164n	D33				
8A	VREFB8AN0	IO	CLK21p		DIFFIO_RX_T165p	DIFFOUT_T165p	G34	DQS22T/CQ22T/CQn22T/QKn22T			
8A	VREFB8AN0	IO	CLK21n		DIFFIO_RX_T165n	DIFFOUT_T165n	H34	DQSn22T/QK22T			
8A	VREFB8AN0	IO			DIFFIO_TX_T166p	DIFFOUT_T166p	F32	DQ22T			
8A	VREFB8AN0	IO			DIFFIO_TX_T166n	DIFFOUT_T166n	G32				
8A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T167p	DIFFOUT_T167p	C34	DQ22T			
8A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T167n	DIFFOUT_T167n	D34	DQ22T			
8A	VREFB8AN0	IO			DIFFIO_TX_T168p	DIFFOUT_T168p	E33	DQ22T			
8A	VREFB8AN0	IO	RZQ_6		DIFFIO_TX_T168n	DIFFOUT_T168n	F33				
8A		MSEL0		MSEL0			H35				
8A		MSEL1		MSEL1			A34				
8A		MSEL2		MSEL2			D35				
8A		MSEL3		MSEL3			A37				
8A		MSEL4		MSEL4			P34				
8A		CONF_DONE		CONF_DONE			K35				
8A		nSTATUS		nSTATUS			F35				
8A		nCE		nCE			M35				
8A		nCONFIG		nCONFIG			A36				
8A		GND					P35				
		GND					AA33				
		GND					AA35				
		GND					AA38				
		GND					AA39				
		GND					AB31				
		GND					AB32				
		GND					AB34				
		GND					AB36				
		GND					AB37				
		GND					AC33				
		GND					AC38				
		GND					AC39				
		GND					AD30				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					AD32				
		GND					AD36				
		GND					AD37				
		GND					AE33				
		GND					AE35				
		GND					AE38				
		GND					AE39				
		GND					AF31				
		GND					AF32				
		GND					AF34				
		GND					AF36				
		GND					AF37				
		GND					AG38				
		GND					AG39				
		GND					AH32				
		GND					AH33				
		GND					AH34				
		GND					AH35				
		GND					AH36				
		GND					AH37				
		GND					AJ35				
		GND					AJ38				
		GND					AJ39				
		GND					AK36				
		GND					AK37				
		GND					AL35				
		GND					AL38				
		GND					AL39				
		GND					AM36				
		GND					AM37				
		GND					AN35				
		GND					AN38				
		GND					AN39				
		GND					AP36				
		GND					AP37				
		GND					AR35				
		GND					AR38				
		GND					AR39				
		GND					AT36				
		GND					AT37				
		GND					AU35				
		GND					AU38				
		GND					AU39				
		GND					AV35				
		GND					AV36				
		GND					AV37				
		GND					AV38				
		GND					AV39				
		GND					AW35				
		GND					AW38				
		GND					B36				
		GND					B37				
		GND					C35				
		GND					C38				
		GND					C39				
		GND					D36				
		GND					D37				
		GND					E35				
		GND					E38				
		GND					E39				
		GND					F36				
		GND					F37				
		GND					G35				
		GND					G38				
		GND					G39				
		GND					H36				
		GND					H37				
		GND					J35				
		GND					J38				
		GND					J39				
		GND					K36				
		GND					K37				
		GND					L35				
		GND					L38				
		GND					L39				
		GND					M36				
		GND					M37				
		GND					N35				
		GND					N38				
		GND					N39				
		GND					P36				
		GND					P37				
		GND					R34				
		GND					R38				
		GND					R39				
		GND					T32				
		GND					T36				
		GND					T37				
		GND					U33				
		GND					U35				
		GND					U38				
		GND					U39				
		GND					V32				
		GND					V34				
		GND					V36				
		GND					V37				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					W33				
		GND					W38				
		GND					W39				
		GND					Y31				
		GND					Y32				
		GND					Y36				
		GND					Y37				
		GND					A2				
		GND					A3				
		GND					A4				
		GND					A5				
		GND					AA3				
		GND					AA4				
		GND					AA6				
		GND					AA8				
		GND					AB1				
		GND					AB2				
		GND					AB7				
		GND					AC3				
		GND					AC4				
		GND					AC8				
		GND					AD1				
		GND					AD10				
		GND					AD2				
		GND					AD5				
		GND					AD7				
		GND					AE3				
		GND					AE4				
		GND					AE6				
		GND					AE8				
		GND					AF1				
		GND					AF2				
		GND					AF9				
		GND					AG3				
		GND					AG4				
		GND					AG5				
		GND					AG6				
		GND					AG7				
		GND					AG8				
		GND					AH1				
		GND					AH2				
		GND					AH5				
		GND					AJ3				
		GND					AJ4				
		GND					AK1				
		GND					AK2				
		GND					AK5				
		GND					AL3				
		GND					AL4				
		GND					AM1				
		GND					AM2				
		GND					AM5				
		GND					AN3				
		GND					AN4				
		GND					AP1				
		GND					AP2				
		GND					AP5				
		GND					AR3				
		GND					AR4				
		GND					AT1				
		GND					AT2				
		GND					AT5				
		GND					AU3				
		GND					AU4				
		GND					AV1				
		GND					AV2				
		GND					B1				
		GND					B2				
		GND					B5				
		GND					C3				
		GND					C4				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					E3				
		GND					E4				
		GND					F1				
		GND					F2				
		GND					F5				
		GND					G3				
		GND					G4				
		GND					H1				
		GND					H2				
		GND					H5				
		GND					J3				
		GND					J4				
		GND					K1				
		GND					K2				
		GND					K5				
		GND					L3				
		GND					L4				
		GND					M1				
		GND					M2				
		GND					M5				
		GND					N3				
		GND					N4				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					N5				
		GND					P1				
		GND					P2				
		GND					P6				
		GND					P7				
		GND					R3				
		GND					R4				
		GND					R8				
		GND					T1				
		GND					T10				
		GND					T2				
		GND					T5				
		GND					T7				
		GND					U3				
		GND					U4				
		GND					U6				
		GND					U8				
		GND					V1				
		GND					V2				
		GND					V7				
		GND					W3				
		GND					W4				
		GND					W8				
		GND					Y1				
		GND					Y2				
		GND					Y5				
		GND					Y7				
		VCCP					AA21				
		VCCP					AA25				
		VCCP					AB15				
		VCCP					U16				
		VCCP					V13				
		VCCP					V22				
		VCCP					V25				
		VCCP					V27				
		VCCP					Y13				
		VCCP					Y27				
		VCCA_FPLL					AC30				
		VCCA_FPLL					AC9				
		VCCA_FPLL					Y30				
		VCCA_FPLL					AA9				
		VCCBAT					R33				
		VCC_AUX					AB14				
		VCC_AUX					AB26				
		VCC_AUX					U14				
		VCC_AUX					U28				
		VCCD_FPLL					AD31				
		VCCD_FPLL					AE9				
		VCCD_FPLL					W30				
		VCCD_FPLL					W9				
		VCCA_GXBL0					AF33				
		VCCA_GXBR0					AE7				
		VCCA_GXBL1					AB33				
		VCCA_GXBR1					AA7				
		VCCH_GXBL0					AD33				
		VCCH_GXBR0					AC7				
		VCCH_GXBL1					Y33				
		VCCH_GXBR1					W7				
		VCCL_GXBL0					AD34				
		VCCL_GXBL0					AD35				
		VCCL_GXBR0					AC5				
		VCCL_GXBR0					AC6				
		VCCL_GXBL1					Y34				
		VCCL_GXBL1					Y35				
		VCCL_GXBR1					W5				
		VCCL_GXBR1					W6				
		VCCR_GXBL					AC34				
		VCCR_GXBL					AC35				
		VCCR_GXBL					AG34				
		VCCR_GXBL					AG35				
		VCCR_GXBL					R35				
		VCCR_GXBR					AB5				
		VCCR_GXBR					AB6				
		VCCR_GXBR					AF5				
		VCCR_GXBR					AF6				
		VCCR_GXBR					P5				
		VCCT_GXBL0					AE34				
		VCCT_GXBL0					AF35				
		VCCT_GXBR0					AD6				
		VCCT_GXBR0					AE5				
		VCCT_GXBL1					AA34				
		VCCT_GXBL1					AB35				
		VCCT_GXBR1					AA5				
		VCCT_GXBR1					Y6				
		VCC					AA10				
		VCC					AA12				
		VCC					AA14				
		VCC					AA16				
		VCC					AA18				
		VCC					AA20				
		VCC					AA22				
		VCC					AA24				
		VCC					AA26				
		VCC					AB11				
		VCC					AB17				
		VCC					U10				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		VCC					U12				
		VCC					V11				
		VCC					V15				
		VCC					V17				
		VCC					V23				
		VCC					V29				
		VCC					W10				
		VCC					W12				
		VCC					W14				
		VCC					W16				
		VCC					W18				
		VCC					W20				
		VCC					W22				
		VCC					W24				
		VCC					W26				
		VCC					W28				
		VCC					Y11				
		VCC					Y15				
		VCC					Y17				
		VCC					Y19				
		VCC					Y23				
		VCC					Y25				
		VCC					Y29				
		VCC					Y21				
		VCCIO3A					AH29				
		VCCIO3A					AJ30				
		VCCIO3A					AK35				
		VCCIO3A					AM30				
		VCCIO3A					AP35				
		VCCIO3A					AT35				
		VCCIO3B					AK28				
		VCCIO3B					AL27				
		VCCIO3B					AN28				
		VCCIO3B					AT28				
		VCCIO3C					AJ24				
		VCCIO3C					AL25				
		VCCIO3C					AM24				
		VCCIO3C					AP25				
		VCCIO3C					AR24				
		VCCIO3C					AU25				
		VCCIO3D					AJ22				
		VCCIO3D					AL21				
		VCCIO3D					AM22				
		VCCIO3D					AP21				
		VCCIO3D					AR22				
		VCCIO3D					AU21				
		VCCIO4A					AG10				
		VCCIO4A					AJ5				
		VCCIO4A					AL5				
		VCCIO4A					AN5				
		VCCIO4A					AR5				
		VCCIO4A					AU5				
		VCCIO4B					AK13				
		VCCIO4B					AM12				
		VCCIO4B					AN10				
		VCCIO4B					AN13				
		VCCIO4B					AR12				
		VCCIO4B					AT10				
		VCCIO4C					AJ15				
		VCCIO4C					AM15				
		VCCIO4C					AR15				
		VCCIO4C					AV15				
		VCCIO4D					AJ19				
		VCCIO4D					AK18				
		VCCIO4D					AM19				
		VCCIO4D					AN18				
		VCCIO4D					AR19				
		VCCIO4D					AT18				
		VCCIO7A					E5				
		VCCIO7A					G5				
		VCCIO7A					H7				
		VCCIO7A					J5				
		VCCIO7A					L5				
		VCCIO7A					M9				
		VCCIO7B					C13				
		VCCIO7B					D10				
		VCCIO7B					F13				
		VCCIO7B					G10				
		VCCIO7B					K10				
		VCCIO7B					L13				
		VCCIO7C					F16				
		VCCIO7C					G15				
		VCCIO7C					K15				
		VCCIO7C					L16				
		VCCIO7D					B19				
		VCCIO7D					D18				
		VCCIO7D					E19				
		VCCIO7D					G18				
		VCCIO7D					H19				
		VCCIO7D					M18				
		VCCIO8A					B35				
		VCCIO8A					G31				
		VCCIO8A					G33				
		VCCIO8A					K31				
		VCCIO8A					K33				
		VCCIO8A					P33				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		VCCIO8B					E28				
		VCCIO8B					E30				
		VCCIO8B					H30				
		VCCIO8B					K28				
		VCCIO8C					C25				
		VCCIO8C					D27				
		VCCIO8C					F25				
		VCCIO8C					G27				
		VCCIO8C					J25				
		VCCIO8C					M24				
		VCCIO8D					C21				
		VCCIO8D					D22				
		VCCIO8D					F21				
		VCCIO8D					G22				
		VCCIO8D					K22				
		VCCIO8D					L21				
		VCCPD3					AA27				
		VCCPD3					AA28				
		VCCPD3					AA29				
		VCCPD3					AB22				
		VCCPD3					AB23				
		VCCPD3					AB24				
		VCCPD3					AB30				
		VCCPD4A					AC10				
		VCCPD4A					AE10				
		VCCPD4BCD					AB12				
		VCCPD4BCD					AB13				
		VCCPD4BCD					AB16				
		VCCPD4BCD					AB18				
		VCCPD4BCD					AB19				
		VCCPD7A					P8				
		VCCPD7A					R10				
		VCCPD7BCD					T12				
		VCCPD7BCD					T13				
		VCCPD7BCD					T16				
		VCCPD7BCD					U18				
		VCCPD7BCD					U19				
		VCCPD8					R32				
		VCCPD8					T30				
		VCCPD8					U21				
		VCCPD8					U22				
		VCCPD8					U24				
		VCCPD8					U26				
		VCCPD8					U29				
		VCCPGM					N11				
		VCCPGM					AG29				
		GND					AA11				
		GND					AA13				
		GND					AA15				
		GND					AA17				
		GND					AA19				
		GND					AA23				
		GND					AA30				
		GND					AB10				
		GND					AC11				
		GND					AC14				
		GND					AC17				
		GND					AC20				
		GND					AC23				
		GND					AC26				
		GND					AC28				
		GND					AE30				
		GND					AF11				
		GND					AF14				
		GND					AF17				
		GND					AF20				
		GND					AF23				
		GND					AF26				
		GND					AF29				
		GND					AF30				
		GND					AG31				
		GND					AG9				
		GND					AJ11				
		GND					AJ14				
		GND					AJ17				
		GND					AJ20				
		GND					AJ23				
		GND					AJ26				
		GND					AJ29				
		GND					AJ32				
		GND					AJ8				
		GND					AM11				
		GND					AM14				
		GND					AM17				
		GND					AM20				
		GND					AM23				
		GND					AM26				
		GND					AM29				
		GND					AM32				
		GND					AM8				
		GND					AR11				
		GND					AR14				
		GND					AR17				
		GND					AR20				
		GND					AR23				
		GND					AR26				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					AR29				
		GND					AR32				
		GND					AR8				
		GND					AV11				
		GND					AV14				
		GND					AV17				
		GND					AV20				
		GND					AV23				
		GND					AV26				
		GND					AV29				
		GND					AV32				
		GND					AV5				
		GND					AV8				
		GND					B11				
		GND					B14				
		GND					B17				
		GND					B20				
		GND					B23				
		GND					B26				
		GND					B29				
		GND					B32				
		GND					B8				
		GND					E11				
		GND					E14				
		GND					E17				
		GND					E20				
		GND					E23				
		GND					E26				
		GND					E29				
		GND					E32				
		GND					E8				
		GND					H11				
		GND					H14				
		GND					H17				
		GND					H20				
		GND					H23				
		GND					H26				
		GND					H29				
		GND					H32				
		GND					H8				
		GND					L11				
		GND					L14				
		GND					L17				
		GND					L20				
		GND					L23				
		GND					L26				
		GND					L29				
		GND					L32				
		GND					L8				
		GND					N8				
		GND					P11				
		GND					P14				
		GND					P17				
		GND					P20				
		GND					P23				
		GND					P26				
		GND					P29				
		GND					P32				
		GND					U11				
		GND					U13				
		GND					U15				
		GND					U17				
		GND					U20				
		GND					U23				
		GND					U25				
		GND					U27				
		GND					U30				
		GND					V10				
		GND					V12				
		GND					V14				
		GND					V16				
		GND					V18				
		GND					V21				
		GND					V24				
		GND					V26				
		GND					V28				
		GND					V30				
		GND					W11				
		GND					W13				
		GND					W15				
		GND					W17				
		GND					W19				
		GND					W23				
		GND					W25				
		GND					W27				
		GND					W29				
		GND					Y10				
		GND					Y12				
		GND					Y14				
		GND					Y16				
		GND					Y18				
		GND					Y20				
		GND					Y22				
		GND					Y24				
		GND					Y26				
		GND					Y28				

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Bank Number	VREF	PinName/Function *(2)*	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY *(3)*
		GND					W21				
		VCCR_GXBR					V6				
		VCCR_GXBR					V5				
		VCCR_GXBL					W35				
		VCCR_GXBL					W34				
		VCCD_FPLL					R9				
		VCCD_FPLL					T31				
		VCCA_FPLL					U9				
		VCCA_FPLL					V31				
		VCCL_GXBR2					R6				
		VCCL_GXBR2					R5				
		VCCL_GXBL2					T35				
		VCCL_GXBL2					T34				
		VCCH_GXBR2					R7				
		VCCH_GXBL2					T33				
		VCCA_GXBR2					U7				
		VCCA_GXBL2					V33				
		GND					H38				
		GND					T8				
		GND					H39				
		GND					T9				
		DNU					G37				
		DNU					B4				
		DNU					G36				
		DNU					B3				
		GND					F38				
		GND					C1				
		GND					F39				
		GND					C2				
		DNU					E37				
		DNU					D4				
		DNU					E36				
		DNU					D3				
		GND					D38				
		GND					E1				
		GND					D39				
		GND					E2				
		DNU					C37				
		DNU					F4				
		DNU					C36				
		DNU					F3				
		GND					U31				
		GND					G1				
		GND					U32				
		GND					G2				
		GND					W31				
		DNU					H4				
		GND					W32				
		DNU					H3				
		GND					P38				
		GND					J1				
		GND					P39				
		GND					J2				
		DNU					N37				
		DNU					K4				
		DNU					N36				
		DNU					K3				
		GND					M38				
		GND					L1				
		GND					M39				
		GND					L2				
		DNU					L37				
		DNU					M4				
		DNU					L36				
		DNU					M3				
		GND					K38				
		GND					N1				
		GND					K39				
		GND					N2				
		DNU					J37				
		GND					V8				
		DNU					J36				
		GND					V9				
		VCCT_GXBR2					U5				
		VCCT_GXBR2					T6				
		VCCT_GXBL2					V35				
		VCCT_GXBL2					U34				

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) RESET pin is only applicable for DDR3 device.

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Version Number	Date	Changes Made
1.0	9/2/2011	Initial release.
1.1	11/8/2011	Updated F1517 package - R9 and T31 changed from NC to VCCD_FPLL - U9 and V31 changed from NC to VCCA_FPLL
1.2	11/30/2011	Updated pin name nPERSTL1 to nPERSTR0
1.3	1/3/2012	Split VCC to VCC and VCCP
1.4	5/11/2012	Rename the CQ pins in DQS and hard memory PHY columns
1.5	7/6/2012	- Some of the NC pins changed to power, DNU, or GND pins. - Updated for production deivce support. Added two HMC address pins (A_4D_15 and A_7D_15) for 5AGXB3 production devices, these two pins are not applicable for 5AGXB3 ES devices.
1.6	7/31/2015	Removed LPDDR2 hard memory PHY, RLDRAMII hard memory PHY, and QDRII hard memory PHY columns.

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