Index within I/O Bank	DDR3 Scheme 1: Component/UDIMM/SODIMM	DDR3 Scheme 2: Component/UDIMM/SODIMM	DDR3 Scheme 3: RDIMM	DDR3 Scheme 4: RDIMM	DDR3 Scheme 5: LRDIMM	DDR4 Scheme 1: Up to 2 CS (4 lanes) for UDIMM/RDIMM/SO-DIMM/Component	DDR4 Scheme 2: Up to 1 CS for UDIMM/RDIMM/SO-DIMM/Component	DDR4 Scheme 3: Up to 4 CS for UDIMM/RDIMM/SO-DIMM/Component; Supports Component and DIMM Ping Pong	DDR4 Scheme 4: Up to 2 CS (3 lanes) for UDIMM/RDIMM/SO-DIMM/Component	DDR4 Scheme 5: LRDIMM (4 lanes)	DDR4 Scheme 6: LRDIMM (3 lanes)	LPDDR3 Scheme 1	QDRII/II+ Scheme 1	QDRIV Scheme 1	QDRIV Scheme 2	RLDRAMII Scheme 1	RLDRAM3 Scheme 1
47			CK_N_1		CK_N_1	CK_N_1		CK_N_1		CK_N_1								
46			CK_1		CK_1	CK_1		CK_1		CK_1								
45	CK_N_3							CK_N_3		CK_N_3								
44	CK_3							CK_3		CK_3								
43	CK_N_2							CK_N_2		CK_N_2								
42	CK_2							CK_2		CK_2								
41	CKE_3		CKE_3			CKE_1		CKE_3		CKE_3								
40	CKE_2		CKE_2			ODT_1		CKE_2		CKE_2				PE_N_0				
39	ODT_3		ODT_3		RM_1	CS_N_1		ODT_3		A_19				AP_0				
38	ODT_2		ODT_2		RM_0			ODT_2		A_18				A_24				
37	CS_N_3		CS_N_3		CS_N_3			CS_N_3		CS_N_3				A_23				
36	CS_N_2		CS_N_2		CS_N_2			CS_N_2		CS_N_2				A_22				
35	BA_2	BA_2	BA_2	BA_2	BA_2	BG_0	BG_0	BG_0	BG_0	BG_0	BG_0	CK_N_3	A_22	A_21	A_21	A_22	BA_2	
34	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	BA_1	CK_3	A_21	A_20	A_20	A_21	BA_1	
33	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	BA_0	CK_N_2	A_20	A_19	A_19	A_20	BA_0	
32	CAS_N_0	CAS_N_0	CAS_N_0	CAS_N_0	CAS_N_0	A_17	A_17	A_17	A_17	A_17	A_17	CK_2	A_19	A_18	A_18	A_19	A_17	
31	RAS_N_0	RAS_N_0	RAS_N_0	RAS_N_0	RAS_N_0	A_16	A_16	A_16	A_16	A_16	A_16		A_18	A_17	A_17	A_18	A_16	
30	A_15	A_15	A_15	A_15	A_15	A_15	A_15	A_15	A_15	A_15	A_15	CKE_3	A_17	A_16	A_16	A_17	A_15	
29	A_14	A_14	A_14	A_14	A_14	A_14	A_14	A_14	A_14	A_14	A_14	CKE_2	A_16	A_15	A_15	A_16	A_14	
28	A_13	A_13	A_13	A_13	A_13	A_13	A_13	A_13	A_13	A_13	A_13	ODT_3	A_15	A_14	A_14	A_15	A_13	
27	A_12	A_12	A_12	A_12	A_12	A_12	A_12	A_12	A_12	A_12	A_12	ODT_2	A_14	A_13	A_13	A_14	A_12	
26																		
25																		
24																		
23	A_11	A_11	A_11	A_11	A_11	A_11	A_11	A_11	A_11	A_11	A_11		A_13	A_12	A_12	A_13	A_11	
22	A_10	A_10	A_10	A_10	A_10	A_10	A_10	A_10	A_10	A_10	A_10		A_12	A_11	A_11	A_12	A_10	
21	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_9	A_11	A_10	A_10	A_11	A_9	
20	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_8	A_10	A_9	A_9	A_10	A_8	
19	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_9	A_8	A_8	A_9	A_7	
18	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_8	A_7	A_7	A_8	A_6	
17	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_7	A_6	A_6	A_7	A_5	
16	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_6	A_5	A_5	A_6	A_4	
15	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_5	A_4	A_4	A_5	A_3	
14	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_4	A_3	A_3	A_4	A_2	
13	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_3	A_2	A_2	A_3	A_1	
12	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_2	A_1	A_1	A_2	A_0	
11	CK_N_1	CK_N_1	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	PAR_0	CK_N_1	A_1	A_0	A_0	A_1	REF_N_0	
10	CK_1	CK_1				C_2	C_2	CS_N_1	CS_N_1	CS_N_1	CS_N_1	CK_1	A_0	AINV_0	AINV_0	A_0		
9	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0	CK_N_0		CK_N_0	CK_N_0	CK_N_0	CK_N_0	
8	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0	CK_0		CK_0	CK_0	CK_0	CK_0	
7	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	C_1	C_1	CKE_1	CKE_1	CKE_1	CKE_1	CKE_1	RPS_N_0	RWB_N_0	RWB_N_0	REF_N_0	WE_N_0	
6	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	CKE_0	WPS_N_0	RWA_N_0	RWA_N_0	WE_N_0	A_20	
5	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	C_0	C_0	ODT_1	ODT_1	ODT_1	ODT_1	ODT_1	DOFF_N_0	LDB_N_0	LDB_N_0	CS_N_0	A_19	
4	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0	ODT_0		LDA_N_0	LDA_N_0	BA_2	A_18	
3	CS_N_1	CS_N_1	CS_N_1	CS_N_1	CS_N_1	ACT_N_0	ACT_N_0	ACT_N_0	ACT_N_0	ACT_N_0	ACT_N_0	CS_N_1		LBK1_N_0	LBK1_N_0	BA_1	CS_N_1	
2	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0	CS_N_0		LBK0_N_0	LBK0_N_0	BA_0	CS_N_0	
1	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	RESET_N_0	CS_N_3		RESET_N_0	RESET_N_0		RESET_N_0	
0	WE_N_0	WE_N_0	WE_N_0	WE_N_0	WE_N_0	BG_1	BG_1	BG_1	BG_1	BG_1	BG_1	CS_N_2		CFG_N_0	CFG_N_0		BA_3	

Date	Version	Changes Made
November 2013	2013.11.27	Initial release.
March 2014	2014.03.20	• Removed DDR4 Scheme 7: LRDIMM. • Updated DDR4 Scheme 1, DDR4 Scheme 3, DDR4 Scheme 5, DDR4 Scheme 6, and RLDRAMII Scheme 1.
November 2014	2014.11.26	• Updated the Column Header of all DDR4 Schemes and Note(1). • Removed "C_#" signals from DDR4 Scheme 1 and DDR4 Scheme 2.
July 2015	2015.07.29	• Updated CK_1, CK_N_1, ALERT_N_0, and PAR_0 in the DDR3 Scheme 5 column. • Updated CK_2, CK_N_2, CK_3, and CK_N_3 in the LPDDR3 Scheme 1 column. • Added C_2, C_0, and C_1 in DDR4 Scheme 1 and DDR4 Scheme 2 columns.
March 2017	2017.03.24	Rebranded as Intel.
December 2017	2017.12.04	Added memory format for DDR4 Scheme 1, DDR4 Scheme 2, DDR4 Scheme 3, and DDR4 Scheme 4.
May 2019	2019.05.08	Removed the note regarding the ALERT_N pin assignment for DDR4.