Pin Information for the Arria® GX EP1AGX35C/D Device
Version 1.4

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B2	VREFB2N0	IO	DIFFIO_RX28p		C28	B20		
B2	VREFB2N0	IO	DIFFIO_RX28n		C27	B19		
B2	VREFB2N0	IO	DIFFIO_TX28p		H23	D19		
B2	VREFB2N0	IO	DIFFIO_TX28n		H22	D18		
B2	VREFB2N0	IO	DIFFIO_RX27p		D28	A17		
B2	VREFB2N0	IO	DIFFIO_RX27n		D27	B17		
B2	VREFB2N0	IO	DIFFIO_TX27p		F24	C20		
B2	VREFB2N0	IO	DIFFIO_TX27n		F23	C19		
B2	VREFB2N0	IO	DIFFIO_RX26p		F27	A19		
B2	VREFB2N0	IO	DIFFIO_RX26n		F26	A18		
B2	VREFB2N0	IO	DIFFIO_TX26p		G24	D20		
B2	VREFB2N0	IO	DIFFIO_TX26n		G23	E20		
B2	VREFB2N0	IO	DIFFIO_RX25p		E28	A21		
B2	VREFB2N0	IO	DIFFIO_RX25n		F28	A20		
B2	VREFB2N0	IO	DIFFIO_TX25p		E26	F20		
B2	VREFB2N0	IO	DIFFIO_TX25n		E25	F19		
B2	VREFB2N0	VREFB2N0	VREFB2N0		T21	J18		
B2	VREFB2N0	IO	DIFFIO_RX24p		G28	B22		
B2	VREFB2N0	IO	DIFFIO_RX24n		G27	A22		
B2	VREFB2N0	IO	DIFFIO_TX24p		K24	G19		
B2	VREFB2N0	IO	DIFFIO_TX24n		J23	G18		
B2	VREFB2N0	IO	DIFFIO_RX23p		J27	C22		
B2	VREFB2N0	IO	DIFFIO_RX23n		J26	C21		
B2	VREFB2N0	IO	DIFFIO_TX23p		K22	F18		
B2	VREFB2N0	IO	DIFFIO_TX23n		K21	F17		
B2	VREFB2N0	IO	DIFFIO_RX22p		H28	D22		
B2	VREFB2N0	IO	DIFFIO_RX22n		J28	D21		
B2	VREFB2N0	IO	DIFFIO_TX22p		K23	G17		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B2	VREFB2N0	IO	DIFFIO_TX22n		L23	G16		
B2	VREFB2N0	IO	DIFFIO_RX21p		L26	E22		
B2	VREFB2N0	IO	DIFFIO_RX21n		L25	F22		
B2	VREFB2N0	IO	DIFFIO_TX21p		G26	H16		
B2	VREFB2N0	IO	DIFFIO_TX21n		G25	J16		
B2	VREFB2N1	IO	DIFFIO_RX20p		K28	F21		
B2	VREFB2N1	IO	DIFFIO_RX20n		K27	G21		
B2	VREFB2N1	IO	DIFFIO_TX20p		M22	K15		
B2	VREFB2N1	IO	DIFFIO_TX20n		M21	K14		
B2	VREFB2N1	IO	DIFFIO_RX19p		M27	G20		
B2	VREFB2N1	IO	DIFFIO_RX19n		M26	H20		
B2	VREFB2N1	IO	DIFFIO_TX19p		J25	J17		
B2	VREFB2N1	IO	DIFFIO_TX19n		J24	K16		
B2	VREFB2N1	IO	DIFFIO_RX18p		L28	G22		
B2	VREFB2N1	IO	DIFFIO_RX18n		M28	H22		
B2	VREFB2N1	IO	DIFFIO_TX18p		H26	L16		
B2	VREFB2N1	IO	DIFFIO_TX18n		H25	L15		
B2	VREFB2N1	IO	DIFFIO_RX17p		N28	J22		
B2	VREFB2N1	IO	DIFFIO_RX17n		P28	J21		
B2	VREFB2N1	IO	DIFFIO_TX17p		K26	M14		
B2	VREFB2N1	IO	DIFFIO_TX17n		K25	N14		
B2	VREFB2N1	VREFB2N1	VREFB2N1		M23	H19		
B2	VREFB2N1	IO	DIFFIO_RX16p		N26	J20		
B2	VREFB2N1	IO	DIFFIO_RX16n		N25	J19		
B2	VREFB2N1	IO	DIFFIO_TX16p		M25	M16		
B2	VREFB2N1	IO	DIFFIO_TX16n		M24	M15		
B2	VREFB2N1	IO	DIFFIO_RX15p		P27	K22		
B2	VREFB2N1	IO	DIFFIO_RX15n		P26	K21		

Pin Information for the Arria® GX EP1AGX35C/D Device
Version 1.4

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B2	VREFB2N1	IO	DIFFIO_TX15p		P25	K20		
B2	VREFB2N1	IO	DIFFIO_TX15n		P24	K19		
B2	VREFB2N1	IO	DIFFIO_RX14p		R28	L22		
B2	VREFB2N1	IO	DIFFIO_RX14n		T28	L21		
B2	VREFB2N1	IO	DIFFIO_TX14p		M20	N16		
B2	VREFB2N1	IO	DIFFIO_TX14n		N20	N15		
B2	VREFB2N1	IO	DIFFIO_RX13p		T27	L20		
B2	VREFB2N1	IO	DIFFIO_RX13n		T26	L19		
B2	VREFB2N1	IO	DIFFIO_TX13p		R21	P16		
B2	VREFB2N1	IO	DIFFIO_TX13n		R20	P15		
B2	VREFB2N1	IO	CLK0n/DIFFIO_RX_C0n		R25	M21		
B2	VREFB2N1	IO	CLK0p/DIFFIO_RX_C0p		R26	M22		
B2	VREFB2N1	CLK1n	INPUT		T24	M19		
B2	VREFB2N1	CLK1p	INPUT		T25	M20		
		VCCD_PLL1			N22	K17		
		VCCA_PLL1			N23	K18		
		GNDA_PLL1			P23	L17		
		GNDA_PLL1			P22	L18		
		GNDA_PLL2			R23	M17		
		GNDA_PLL2			R22	M18		
		VCCA_PLL2			T23	N18		
		VCCD_PLL2			T22	N17		
B1	VREFB1N0	IO	CLK2p/DIFFIO_RX_C1p		U28	N22		
B1	VREFB1N0	IO	CLK2n/DIFFIO_RX_C1n		U27	N21		
B1	VREFB1N0	CLK3p	INPUT		U26	N20		
B1	VREFB1N0	CLK3n	INPUT		U25	N19		
B1	VREFB1N0	IO	DIFFIO_RX12p		V28	P22		
B1	VREFB1N0	IO	DIFFIO_RX12n		W28	P21		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B1	VREFB1N0	IO	DIFFIO_TX12p		T19	T15		
B1	VREFB1N0	IO	DIFFIO_TX12n		U19	T14		
B1	VREFB1N0	IO	DIFFIO_RX11p		Y28	P20		
B1	VREFB1N0	IO	DIFFIO_RX11n		AA28	P19		
B1	VREFB1N0	IO	DIFFIO_TX11p		U20	T16		
B1	VREFB1N0	IO	DIFFIO_TX11n		V20	U16		
B1	VREFB1N0	VREFB1N0	VREFB1N0		Y23	R20		
B1	VREFB1N0	IO	DIFFIO_RX10p		W27	R22		
B1	VREFB1N0	IO	DIFFIO_RX10n		W26	T22		
B1	VREFB1N0	IO	DIFFIO_TX10p		Y25	P17		
B1	VREFB1N0	IO	DIFFIO_TX10n		Y24	R16		
B1	VREFB1N0	IO	DIFFIO_RX9p		Y27	T21		
B1	VREFB1N0	IO	DIFFIO_RX9n		Y26	T20		
B1	VREFB1N0	IO	DIFFIO_TX9p		U24	V17		
B1	VREFB1N0	IO	DIFFIO_TX9n		U23	W17		
B1	VREFB1N0	IO	DIFFIO_RX8p		V26	U21		
B1	VREFB1N0	IO	DIFFIO_RX8n		V25	U20		
B1	VREFB1N0	IO	DIFFIO_TX8p		AA26	U18		
B1	VREFB1N0	IO	DIFFIO_TX8n		AA25	U17		
B1	VREFB1N0	IO	DIFFIO_RX7p		AB28	U22		
B1	VREFB1N0	IO	DIFFIO_RX7n		AB27	V22		
B1	VREFB1N0	IO	DIFFIO_TX7p		V23	R17		
B1	VREFB1N0	IO	DIFFIO_TX7n		V22	T17		
B1	VREFB1N1	IO	DIFFIO_RX6p		AC28	W22		
B1	VREFB1N1	IO	DIFFIO_RX6n		AD28	W21		
B1	VREFB1N1	IO	DIFFIO_TX6p		W21	W19		
B1	VREFB1N1	IO	DIFFIO_TX6n		Y21	W18		
B1	VREFB1N1	IO	DIFFIO_RX5p		AD26	Y22		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B1	VREFB1N1	IO	DIFFIO_RX5n		AD25	Y21		
B1	VREFB1N1	IO	DIFFIO_TX5p		AC25	Y19		
B1	VREFB1N1	IO	DIFFIO_TX5n		AC24	Y18		
B1	VREFB1N1	IO	DIFFIO_RX4p		W25	AA22		
B1	VREFB1N1	IO	DIFFIO_RX4n		W24	AB22		
B1	VREFB1N1	IO	DIFFIO_TX4p		AB22	V20		
B1	VREFB1N1	IO	DIFFIO_TX4n		AB21	V19		
B1	VREFB1N1	VREFB1N1	VREFB1N1		W23	P18		
B1	VREFB1N1	IO	DIFFIO_RX3p		AC27	AB21		
B1	VREFB1N1	IO	DIFFIO_RX3n		AC26	AB20		
B1	VREFB1N1	IO	DIFFIO_TX3p		AE26	R19		
B1	VREFB1N1	IO	DIFFIO_TX3n		AE25	T19		
B1	VREFB1N1	IO	DIFFIO_RX2p		AB26	AB19		
B1	VREFB1N1	IO	DIFFIO_RX2n		AB25	AB18		
B1	VREFB1N1	IO	DIFFIO_TX2p		AB24	AB17		
B1	VREFB1N1	IO	DIFFIO_TX2n		AB23	AA17		
B1	VREFB1N1	IO	DIFFIO_RX1p		AE28	AA20		
B1	VREFB1N1	IO	DIFFIO_RX1n		AE27	AA19		
B1	VREFB1N1	IO	DIFFIO_TX1p		AC23	AA16		
B1	VREFB1N1	IO	DIFFIO_TX1n		AC22	Y17		
B1	VREFB1N1	IO	DIFFIO_RX0p		AF28	W20		
B1	VREFB1N1	IO	DIFFIO_RX0n		AF27	Y20		
B1	VREFB1N1	IO	DIFFIO_TX0p		AA23	AB16		
B1	VREFB1N1	IO	DIFFIO_TX0n		AA22	AB15		
B8	VREFB8N0	TDI		TDI	V19	AA14		
B8	VREFB8N0	TMS		TMS	W19	Y16		
B8	VREFB8N0	TCK		TCK	V17	AB13		
B8	VREFB8N0	TRST		TRST	W17	AB14		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B8	VREFB8N0	nCONFIG		nCONFIG	V16	Y15		
B8	VREFB8N0	VCCSEL		VCCSEL	W18	AB12		
B8	VREFB8N0	IO		CS	AE24	Y14		
B8	VREFB8N0	IO		CLKUSR	AC21	AA11		
B8	VREFB8N0	IO		nWS	AE22	AA13		
B8	VREFB8N0	IO		nRS	AE21	AB11		
B8	VREFB8N0	IO			AE23	W16		
B8	VREFB8N0	IO			W16			
B8	VREFB8N0	IO			AD20			
B8	VREFB8N0	IO			AB20			
B8	VREFB8N0	IO	DQ17B		AF26		DQ3B	
B8	VREFB8N0	IO			AF25		DQ3B	DQ1B
B8	VREFB8N0	VREFB8N0	VREFB8N0		AD19	V16		
B8	VREFB8N0	IO	DQ17B		AG26		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ17B		AH25		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ17B		AH26		DQ3B	DQ1B
B8	VREFB8N0	IO	DQS17B		AG25			
B8	VREFB8N0	IO			AA19			
B8	VREFB8N0	IO			AB19			
B8	VREFB8N0	IO	DQ15B		AH24		DQ3B	DQ1B
B8	VREFB8N0	IO			AF23	W15		DQ1B
B8	VREFB8N0	IO	DQ15B		AF24		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ15B		AF22		DQ3B	DQ1B
B8	VREFB8N0	IO	DQ15B		AH23		DQ3B	DQ1B
B8	VREFB8N0	IO	DQS15B		AG23	W14	DQS3B	
B8	VREFB8N0	IO			AC19			
B8	VREFB8N0	IO			AB18			
B8	VREFB8N0	IO			AE19			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B8	VREFB8N1	IO				W11		
B8	VREFB8N1	IO	DQ13B		AG22		DQ2B	DQ1B
B8	VREFB8N1	IO			AF20		DQ2B	
B8	VREFB8N1	IO	DQ13B		AH22		DQ2B	DQ1B
B8	VREFB8N1	IO	DQ13B		AH21		DQ2B	DQ1B
B8	VREFB8N1	IO	DQ13B		AF21		DQ2B	DQ1B
B8	VREFB8N1	IO	DQS13B		AG20			DQS1B
B8	VREFB8N1	IO			AA17			
B8	VREFB8N1	IO			Y17			
B8	VREFB8N1	IO	DQ11B		AH20	Y13	DQ2B	DQ1B
B8	VREFB8N1	IO			AG19	Y12		DQ1B
B8	VREFB8N1	IO	DQ11B		AF19	W12	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ11B		AF18	Y11	DQ2B	DQ1B
B8	VREFB8N1	IO	DQ11B		AH18		DQ2B	DQ1B
B8	VREFB8N1	IO	DQS11B		AH19	W13	DQS2B	
B8	VREFB8N1	VREFB8N1	VREFB8N1		AD17	V14		
B8	VREFB8N1	IO			AB17	AB9		
B8	VREFB8N1	IO			AC17			
B8	VREFB8N1	IO			W15			
B8	VREFB8N1	IO			Y15			
B8	VREFB8N1	IO		RUnLU	AC16	T13		
B8	VREFB8N1	IO		DEV_OE	AD16	U14		
B8	VREFB8N1	IO		DEV_CLRn	AE17	U13		
B8	VREFB8N1	IO		nCS	AF17	AB10		
B8	VREFB8N1	IO	CLK5n		AB15	W10		
B8	VREFB8N1	IO	CLK5p		AC15	Y9		
B8	VREFB8N1	IO	CLK4n		AG17	Y10		
B8	VREFB8N1	IO	CLK4p		AH17	AA10		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GNDA_PLL6			W14	T12		
		GNDA_PLL6			W13	U11		
		VCCA_PLL6			Y14	U12		
		VCCD_PLL6			V14	T11		
B10		VCC_PLL6_OUT			AA14	V10		
B7	VREFB7N0	IO	CLK7p		AF15	AB8		
B7	VREFB7N0	IO	CLK7n		AE15	AA8		
B7	VREFB7N0	IO	CLK6p		AH16	Y8		
B7	VREFB7N0	IO	CLK6n		AG16	W9		
B10	VREFB7N0	IO	PLL6_OUT1p		AG14	AA7		
B10	VREFB7N0	IO	PLL6_OUT1n		AF14	Y7		
B10	VREFB7N0	IO	PLL6_OUT0p		AH15	AB7		
B10	VREFB7N0	IO	PLL6_OUT0n		AH14	AB6		
B10	VREFB7N0	IO	PLL6_FBp/OUT2p		AE14	W8		
B10	VREFB7N0	IO	PLL6_FBn/OUT2n		AD14	W7		
B7	VREFB7N0	IO			Y13			
B7	VREFB7N0	IO			AB13			
B7	VREFB7N0	IO	DQ9B		AG13	U10	DQ1B	
B7	VREFB7N0	IO			AE13	Y6	DQ1B	DQ0B
B7	VREFB7N0	VREFB7N0	VREFB7N0		AB14	V11		
B7	VREFB7N0	IO	DQ9B		AC14	T8	DQ1B	DQ0B
B7	VREFB7N0	IO	DQ9B		AC13	T9	DQ1B	DQ0B
B7	VREFB7N0	IO	DQ9B		AD13	T10	DQ1B	DQ0B
B7	VREFB7N0	IO	DQS9B		AF13			
B7	VREFB7N0	IO			AB12			
B7	VREFB7N0	IO			V11			
B7	VREFB7N0	IO			AC12			
B7	VREFB7N0	IO	DQ7B		AH13	AB4	DQ1B	DQ0B

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B7	VREFB7N0	IO			AF12	AB5		DQ0B
B7	VREFB7N0	IO	DQ7B		AH12		DQ1B	DQ0B
B7	VREFB7N0	IO	DQ7B		AG11		DQ1B	DQ0B
B7	VREFB7N0	IO	DQ7B		AH11	AA4	DQ1B	DQ0B
B7	VREFB7N0	IO	DQS7B		AE12	AA5	DQS1B	
B7	VREFB7N0	IO			AA11			
B7	VREFB7N0	IO			AB11			
B7	VREFB7N1	IO			AC11			
B7	VREFB7N1	IO	DQ5B		AD11		DQ0B	DQ0B
B7	VREFB7N1	IO			AF11	V7	DQ0B	
B7	VREFB7N1	IO	DQ5B		AF10		DQ0B	DQ0B
B7	VREFB7N1	IO	DQ5B		AG10		DQ0B	DQ0B
B7	VREFB7N1	IO	DQ5B		AH10		DQ0B	DQ0B
B7	VREFB7N1	IO	DQS5B		AE11	U8		DQS0B
B7	VREFB7N1	IO			AB9			
B7	VREFB7N1	IO			AB10			
B7	VREFB7N1	IO	DQ3B		AE10		DQ0B	DQ0B
B7	VREFB7N1	IO			AF9			DQ0B
B7	VREFB7N1	IO	DQ3B		AH8	Y5	DQ0B	DQ0B
B7	VREFB7N1	IO	DQ3B		AH9		DQ0B	DQ0B
B7	VREFB7N1	IO	DQ3B		AD10		DQ0B	DQ0B
B7	VREFB7N1	IO	DQS3B		AE9		DQS0B	
B7	VREFB7N1	VREFB7N1	VREFB7N1		AC10	V8		
B7	VREFB7N1	IO			AC9			
B7	VREFB7N1	IO			Y10			
B7	VREFB7N1	IO	DQ1B		AH7			
B7	VREFB7N1	IO			AG8	Y4		
B7	VREFB7N1	IO	DQ1B		AE7			

Pin Information for the Arria® GX EP1AGX35C/D Device
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Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B7	VREFB7N1	IO	DQ1B		AF7			
B7	VREFB7N1	IO	DQ1B		AE8			
B7	VREFB7N1	IO	DQS1B		AF8			
B7	VREFB7N1	IO			W9			
B7	VREFB7N1	IO			AC8	AB3		
B7	VREFB7N1	IO			AB8	Y3		
B7	VREFB7N1	PORSEL		PORSEL	Y8	AB2		
B7	VREFB7N1	nIO_PULLUP		nIO_PULLUP	Y7	AB1		
B7	VREFB7N1	PLL_ENA		PLL_ENA	AA8	AA2		
		GND			AC7	Y2		
B7	VREFB7N1	nCEO		nCEO	AB7	Y1		
B14		GXB_RX7n			AD2	V2		
B14		GXB_RX7p			AD1	V1		
B14		GXB_TX7n			AF5	V5		
B14		GXB_TX7p			AF4	V4		
B14		GXB_RX6n			AB2	T2		
B14		GXB_RX6p			AB1	T1		
B14		GXB_TX6n			AD5	T5		
B14		GXB_TX6p			AD4	T4		
B14		RREFB14			Y4	J3		
B14		REFCLK0_B14n			Y2	N1		
B14		REFCLK0_B14p			Y1	P1		
B14		REFCLK1_B14n			AB5	J1		
B14		REFCLK1_B14p			AB4	K1		
		VCCA			V9	P6		
		VCCA			T6	M3		
		VCCA			V7	P4		
B14		GXB_RX4n			V2	G2		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B14		GXB_RX4p			V1	G1		
B14		GXB_TX4n			V5	G5		
B14		GXB_TX4p			V4	G4		
B14		GXB_RX5n			T2	E2		
B14		GXB_RX5p			T1	E1		
B14		GXB_TX5n			T5	E5		
B14		GXB_TX5p			T4	E4		
B13		GXB_RX3n			N2			
B13		GXB_RX3p			N1			
B13		GXB_TX3n			N5			
B13		GXB_TX3p			N4			
B13		GXB_RX2n			L2			
B13		GXB_RX2p			L1			
B13		GXB_TX2n			L5			
B13		GXB_TX2p			L4			
B13		RREFB13			J4			
B13		REFCLK0_B13n			J2			
B13		REFCLK0_B13p			J1			
B13		REFCLK1_B13n			G5			
B13		REFCLK1_B13p			G4			
		VCCA			P9			
		VCCA			M6			
		VCCA			P7			
B13		GXB_RX0n			G2			
B13		GXB_RX0p			G1			
B13		GXB_TX0n			E5			
B13		GXB_TX0p			E4			
B13		GXB_RX1n			E2			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B13		GXB_RX1p			E1			
B13		GXB_TX1n			C5			
B13		GXB_TX1p			C4			
NC		NC			K7	J5		
NC		NC			K8	J6		
		VCCA			K9			
		GND			F7	C3		
		GND			G7	C2		
B4	VREFB4N0	TDO		TDO	F8	C1		
B4	VREFB4N0	MSEL3		MSEL3	G8	A1		
B4	VREFB4N0	MSEL2		MSEL2	H8	A2		
B4	VREFB4N0	MSEL1		MSEL1	E8	C4		
B4	VREFB4N0	MSEL0		MSEL0	J8	C5		
B4	VREFB4N0	IO			C7	H8		
B4	VREFB4N0	IO			D7	G8		
B4	VREFB4N0	IO	DQS1T		C8			
B4	VREFB4N0	IO	DQ1T		D9			
B4	VREFB4N0	IO	DQ1T		A7	F7		
B4	VREFB4N0	IO	DQ1T		D8			
B4	VREFB4N0	IO			B8	B2		
B4	VREFB4N0	IO	DQ1T		A8			
B4	VREFB4N0	IO			K10			
B4	VREFB4N0	IO			G9			
B4	VREFB4N0	IO			J10	G9		
B4	VREFB4N0	VREFB4N0	VREFB4N0		F10	E8		
B4	VREFB4N0	IO	DQS3T		D10		DQS0T	
B4	VREFB4N0	IO	DQ3T		B10		DQ0T	DQ0T
B4	VREFB4N0	IO	DQ3T		A9		DQ0T	DQ0T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B4	VREFB4N0	IO	DQ3T		C9		DQ0T	DQ0T
B4	VREFB4N0	IO			C10			DQ0T
B4	VREFB4N0	IO	DQ3T		E11		DQ0T	DQ0T
B4	VREFB4N0	IO			E10			
B4	VREFB4N0	IO			K11	F8		
B4	VREFB4N0	IO			G10			
B4	VREFB4N0	IO	DQS5T		C11			DQS0T
B4	VREFB4N0	IO	DQ5T		C12		DQ0T	DQ0T
B4	VREFB4N0	IO	DQ5T		D11		DQ0T	DQ0T
B4	VREFB4N0	IO	DQ5T		A10		DQ0T	DQ0T
B4	VREFB4N0	IO			B11		DQ0T	
B4	VREFB4N0	IO	DQ5T		D12		DQ0T	DQ0T
B4	VREFB4N0	IO			J11			
B4	VREFB4N0	IO			H11			
B4	VREFB4N1	IO			K12			
B4	VREFB4N1	IO			L12			
B4	VREFB4N1	IO	DQS7T		D13	B4	DQS1T	
B4	VREFB4N1	IO	DQ7T		A11	A3	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		F13	D7	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		A12	C6	DQ1T	DQ0T
B4	VREFB4N1	IO			C13	B5		DQ0T
B4	VREFB4N1	IO	DQ7T		E13	A4	DQ1T	DQ0T
B4	VREFB4N1	IO			G12			
B4	VREFB4N1	IO			K13			
B4	VREFB4N1	IO			L13			
B4	VREFB4N1	IO	DQS9T		B14	H9		
B4	VREFB4N1	IO	DQ9T		E14	F11	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ9T		A13	G10	DQ1T	DQ0T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B4	VREFB4N1	IO	DQ9T		B13		DQ1T	DQ0T
B4	VREFB4N1	VREFB4N1	VREFB4N1		F12	E11		
B4	VREFB4N1	IO			C14	H10	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ9T		D14		DQ1T	
B4	VREFB4N1	IO			H13			
B4	VREFB4N1	IO			G13			
B9	VREFB4N1	IO	PLL5_FBn/OUT2n		G14	C7		
B9	VREFB4N1	IO	PLL5_FBp/OUT2p		F14	B7		
B9	VREFB4N1	IO	PLL5_OUT0n		A14	D9		
B9	VREFB4N1	IO	PLL5_OUT0p		A15	C9		
B9	VREFB4N1	IO	PLL5_OUT1n		D15	D8		
B9	VREFB4N1	IO	PLL5_OUT1p		C15	C8		
B4	VREFB4N1	IO	CLK12n		B16	B8		
B4	VREFB4N1	IO	CLK12p		A16	A7		
B4	VREFB4N1	IO	CLK13n		G15	A6		
B4	VREFB4N1	IO	CLK13p		F15	A5		
B9		VCC_PLL5_OUT			J14	E10		
		VCCD_PLL5			K16	H11		
		VCCA_PLL5			J15	G12		
		GNDA_PLL5			J16	H12		
		GNDA_PLL5			K15	G11		
B3	VREFB3N0	IO	CLK14p		A17	A8		
B3	VREFB3N0	IO	CLK14n		B17	A9		
B3	VREFB3N0	IO	CLK15p		C16	C10		
B3	VREFB3N0	IO	CLK15n		D16	D10		
B3	VREFB3N0	IO		PGM2	E16	C11		
B3	VREFB3N0	IO		PGM1	F16	D13		
B3	VREFB3N0	IO		PGM0	G16	D12		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B3	VREFB3N0	IO		ASDO	L16	F12		
B3	VREFB3N0	IO		nCSO	D17	B10		
B3	VREFB3N0	IO		CRC_ERROR	E17	A10		
B3	VREFB3N0	IO		DATA0	F17	D11		
B3	VREFB3N0	IO		DATA1	K17	F13		
B3	VREFB3N0	IO			G17			
B3	VREFB3N0	IO			D18			
B3	VREFB3N0	IO			L17			
B3	VREFB3N0	VREFB3N0	VREFB3N0		E19	E14		
B3	VREFB3N0	IO	DQS11T		A19	D14	DQS2T	
B3	VREFB3N0	IO	DQ11T		A18	C12	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		C18	C13	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		C19	B13	DQ2T	DQ1T
B3	VREFB3N0	IO			B19	C14		DQ1T
B3	VREFB3N0	IO	DQ11T		A20	B14	DQ2T	DQ1T
B3	VREFB3N0	IO			G18			
B3	VREFB3N0	IO			J18			
B3	VREFB3N0	IO			K18	G13		
B3	VREFB3N0	IO	DQS13T		B20	H13		DQS1T
B3	VREFB3N0	IO	DQ13T		A21	H14	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ13T		C21		DQ2T	DQ1T
B3	VREFB3N0	IO	DQ13T		A22	J14	DQ2T	DQ1T
B3	VREFB3N0	IO			C20	G14	DQ2T	
B3	VREFB3N0	IO	DQ13T		B22	G15	DQ2T	DQ1T
B3	VREFB3N0	IO			K19			
B3	VREFB3N1	IO			H19	F14		
B3	VREFB3N1	IO	DQS15T		B23	D15	DQS3T	
B3	VREFB3N1	IO	DQ15T		A23		DQ3T	DQ1T

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B3	VREFB3N1	IO	DQ15T		C22		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		A24		DQ3T	DQ1T
B3	VREFB3N1	IO			C23			DQ1T
B3	VREFB3N1	IO	DQ15T		C24		DQ3T	DQ1T
B3	VREFB3N1	IO			D20			
B3	VREFB3N1	IO			L19			
B3	VREFB3N1	IO			G19			
B3	VREFB3N1	IO	DQS17T		B25			
B3	VREFB3N1	IO	DQ17T		A26		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ17T		A25		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ17T		C26		DQ3T	DQ1T
B3	VREFB3N1	IO			C25		DQ3T	DQ1T
B3	VREFB3N1	IO	DQ17T		B26		DQ3T	
B3	VREFB3N1	VREFB3N1	VREFB3N1		E20	E16		
B3	VREFB3N1	IO			F20	D16		
B3	VREFB3N1	IO			K20	F16		
B3	VREFB3N1	IO			L20	C15		
B3	VREFB3N1	IO		DATA2	F21	A12		
B3	VREFB3N1	IO		DATA3	D21	A13		
B3	VREFB3N1	IO		DATA4	G21	B11		
B3	VREFB3N1	IO		DATA5	D23	D17		
B3	VREFB3N1	IO		DATA6	F22	A14		
B3	VREFB3N1	IO		DATA7	D22	C16		
B3	VREFB3N1	IO		RDYnBSY	J21	A11		
B3	VREFB3N1	IO		INIT_DONE	G22	C17		
B3	VREFB3N1	nSTATUS		nSTATUS	D26	A16		
B3	VREFB3N1	nCE		nCE	D24	A15		
B3	VREFB3N1	DCLK		DCLK	D25	B16		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
B3	VREFB3N1	CONF_DONE		CONF_DONE	E23	C18		
		VCCIO2			J22	J15		
		VCCIO2			L22	H17		
		VCCIO2			N21			
		VCCIO1			U22	R14		
		VCCIO1			V21	T18		
		VCCIO1			Y22			
		VCCIO8			AA16	U15		
		VCCIO8			Y18	V13		
		VCCIO8			Y19			
		VCCIO7			AA10	U7		
		VCCIO7			AA13	U9		
		VCCIO7			Y9			
		VCCT_B14			R8	L5		
		VCCT_B14			T8	M5		
		VCCH_B14			R9	L6		
		VCCH_B14			T9	M6		
		VCCR			R7	L4		
		VCCR			T7	M4		
		VCCA			R6	L3		
		VCCL_B14			U6	N3		
		VCCT_B13			L8			
		VCCT_B13			M8			
		VCCH_B13			L9			
		VCCH_B13			M9			
		VCCL_B13			N6			
		VCCR			L7			
		VCCR			M7			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		VCCA			L6			
		VCCP			R10	L7		
		VCCP			T10	M7		
		VCCP			L10			
		VCCP			M10			
		VCCIO4			H14	G7		
		VCCIO4			J9	F9		
		VCCIO4			J12			
		VCCIO3			H17	F15		
		VCCIO3			H20	E13		
		VCCIO3			J19			
		VCCA				J7		
		VCCINT			M12	K13		
		VCCINT			M14	K11		
		VCCINT			M16	J10		
		VCCINT			M18	K9		
		VCCINT			N11	L8		
		VCCINT			N13	M9		
		VCCINT			N15	N8		
		VCCINT			N17	P9		
		VCCINT			P12	R10		
		VCCINT			P14	P11		
		VCCINT			P16	N10		
		VCCINT			P18	L10		
		VCCINT			R11	M11		
		VCCINT			R13	L12		
		VCCINT			R15	M13		
		VCCINT			R17	N12		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		VCCINT			T12	P13		
		VCCINT			T14			
		VCCINT			T16			
		VCCINT			T18			
		VCCINT			U11			
		VCCINT			U13			
		VCCINT			U15			
		VCCINT			U17			
		GND			AA21	AA21		
		GND			AA24	AA18		
		GND			AA27	V18		
		GND			AD24	V21		
		GND			AD27	R21		
		GND			AG27	R18		
		GND			AG28	R15		
		GND			B28	H18		
		GND			E27	H15		
		GND			H21	H21		
		GND			H24	E21		
		GND			H27	E18		
		GND			L21	B18		
		GND			L24	B21		
		GND			L27			
		GND			M19			
		GND			N24			
		GND			N27			
		GND			P21			
		GND			R24			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			R27			
		GND			U21			
		GND			V24			
		GND			V27			
		GND			W20			
		GND			W22			
		GND			Y20			
		GND			W8	AA1		
		GND			W7	AA3		
		GND			V18	AA6		
		GND			V15	T7		
		GND			V12	V9		
		GND			V10	AA9		
		GND			AH27	AA12		
		GND			AG9	V12		
		GND			AG7	V15		
		GND			AG24	AA15		
		GND			AG21			
		GND			AG18			
		GND			AG15			
		GND			AG12			
		GND			AD9			
		GND			AD7			
		GND			AD21			
		GND			AD18			
		GND			AD15			
		GND			AD12			
		GND			AA9			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			AA7			
		GND			AA20			
		GND			AA18			
		GND			AA15			
		GND			AA12			
		GND			A2	D1		
		GND			A3	D2		
		GND			A4	D3		
		GND			A5	D4		
		GND			A6	D5		
		GND			AA1	D6		
		GND			AA2	E3		
		GND			AA3	E6		
		GND			AA4	F1		
		GND			AA5	F2		
		GND			AA6	F3		
		GND			AB3	F4		
		GND			AB6	F5		
		GND			AC1	F6		
		GND			AC2	G3		
		GND			AC3	G6		
		GND			AC4	H1		
		GND			AC5	H2		
		GND			AC6	H3		
		GND			AD3	H4		
		GND			AD6	H5		
		GND			AE1	J2		
		GND			AE2	J4		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			AE3	H6		
		GND			AE4	K2		
		GND			AE5	K3		
		GND			AE6	K4		
		GND			AF1	K5		
		GND			AF2	K6		
		GND			AF3	K7		
		GND			AF6	L1		
		GND			AG1	L2		
		GND			AG2	M1		
		GND			AG3	M2		
		GND			AG4	N2		
		GND			AG5	N4		
		GND			AG6	N5		
		GND			AH2	N6		
		GND			AH3	N7		
		GND			AH4	P2		
		GND			AH5	P3		
		GND			AH6	P5		
		GND			B1	P7		
		GND			B2	R1		
		GND			B3	R2		
		GND			B4	R3		
		GND			B5	R4		
		GND			B6	R5		
		GND			C1	R6		
		GND			C2	R7		
		GND			C3	T3		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			C6	T6		
		GND			D1	U1		
		GND			D2	U2		
		GND			D3	U3		
		GND			D4	U4		
		GND			D5	U5		
		GND			D6	U6		
		GND			E3	V3		
		GND			E6	V6		
		GND			F1	W1		
		GND			F2	W2		
		GND			F3	W3		
		GND			F4	W4		
		GND			F5	W5		
		GND			F6	W6		
		GND			G3			
		GND			G6			
		GND			H1			
		GND			H2			
		GND			H3			
		GND			H4			
		GND			H5			
		GND			H6			
		GND			J3			
		GND			J5			
		GND			J6			
		GND			K1			
		GND			K2			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			K3			
		GND			K4			
		GND			K5			
		GND			K6			
		GND			L3			
		GND			M1			
		GND			M2			
		GND			M3			
		GND			M4			
		GND			M5			
		GND			N3			
		GND			N7			
		GND			N8			
		GND			N9			
		GND			N10			
		GND			P1			
		GND			P2			
		GND			P3			
		GND			P4			
		GND			P5			
		GND			P6			
		GND			R1			
		GND			R2			
		GND			R3			
		GND			R4			
		GND			R5			
		GND			T3			
		GND			U1			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			U2			
		GND			U3			
		GND			U4			
		GND			U5			
		GND			U7			
		GND			U8			
		GND			U9			
		GND			U10			
		GND			V3			
		GND			V6			
		GND			W1			
		GND			W2			
		GND			W3			
		GND			W4			
		GND			W5			
		GND			W6			
		GND			Y3			
		GND			Y5			
		GND			Y6			
		GND			V8			
		GND			P8			
		GND			A27	B1		
		GND			B12	B3		
		GND			B15	B6		
		GND			B18	B9		
		GND			B21	E9		
		GND			B24	H7		
		GND			B27	E12		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			B7	B12		
		GND			B9	B15		
		GND			E12	E15		
		GND			E15			
		GND			E18			
		GND			E21			
		GND			E24			
		GND			E7			
		GND			E9			
		GND			H12			
		GND			H15			
		GND			H16			
		GND			H18			
		GND			H7			
		GND			H9			
		GND			J7			
		GND			L11			
		GND			L15			
		GND			L18			
		GND			M11	J12		
		GND			M13	K12		
		GND			M15	J11		
		GND			M17	J9		
		GND			N12	K10		
		GND			N14	K8		
		GND			N16	L9		
		GND			N18	M8		
		GND			P11	N9		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		GND			P13	P8		
		GND			P15	R9		
		GND			P17	P10		
		GND			R12	R11		
		GND			R14	R12		
		GND			R16	P12		
		GND			R18	N13		
		GND			T11	M12		
		GND			T13	L13		
		GND			T15	L11		
		GND			T17	N11		
		GND			U12	M10		
		GND			U14			
		GND			U16			
		GND			U18			
		GND			N19			
		GND			P10			
		GND			P19			
		GND			R19			
		VCCPD2			P20	L14		
		VCCPD1			T20	P14		
		VCCPD8			Y16	R13		
		VCCPD7			Y12	R8		
		VCCPD4			J13	J8		
		VCCPD3			J17	J13		
		NC			AD8	E17		
		NC			AD22	E7		
		NC			AD23	F10		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)
		NC			AE16	E19		
		NC			AF16	U19		
		NC			C17			
		NC			E22			
		NC			F9			
		NC			F25			
		NC			AE20			
		NC			AC20			
		NC			AC18			
		NC			AE18			
		NC			AB16			
		NC			V13			
		NC			W12			
		NC			W11			
		NC			Y11			
		NC			W10			
		NC			H10			
		NC			G11			
		NC			F11			
		NC			L14			
		NC			K14			
		NC			F18			
		NC			F19			
		NC			D19			
		NC			G20			
		NC			J20			

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)	Configuration Function	EP1AGX35DF780	EP1AGX35CF484	x8/x9 Mode (1)	x16/x18 Mode (1)
							DQ group for DQS mode (F780, F484)	DQ group for DQS mode (F780, F484)

Note:

1. The DQS/DQ mode shown in this column applies to the largest device package in the pin list.
   Smaller packages may not have the pins to support some of the DQS groups.
   To determine the supported DQS/DQ groups, check the pin availability for the target device package.
   For example, for the EP1AGX35CF484 package, there is only one x8 group, but no x9 group.

Pin Name	Pin Type (1st, 2nd, and 3rd Functions)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	1.2-V internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HSTL, SSTL, differential HSTL, and differential SSTL I/O standards.
VCCIO[1..4,7,8]	Power	I/O supply voltage pins for banks 1-4, 7, and 8. Each bank can support a different voltage level. Supported voltages are 1.5V, 1.8V, 2.5V, and 3.3V. VCCIO[4,7,8] also support 1.2V for 1.2V HSTL operation.For specific I/O standards supported by Arria GX FPGA refer to the Arria GX Handbook.
VCCPD[1..4,7,8]	Power	Dedicated power pins. This 3.3-V supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and the JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR.
GND	Ground	Device ground pins.
VREFB[1..4,7,8]N[2..0]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for that bank. All the VREF pins within a bank are shorted together.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p, and PLL5_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL5 in bank 9 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p, and PLL6_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL6 in bank 10 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL11_OUT	Power	External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p, and PLL11_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL11 in bank 11 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCC_PLL12_OUT	Power	External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p, and PLL12_FBn/OUT2n. This pin should be connected to the voltage level of the target device that PLL12 in bank 12 is driving. Refer to the data sheet for absolute maximum voltage rating on this pin.
VCCA_PLL[1,2,5..8,11,12]	Power	1.2-V analog power for PLL[1,2,5..8,11,12].
VCCD_PLL[1,2,5..8,11,12]	Power	1.2-V digital power for PLL[1,2,5..8,11,12].
GNDA_PLL[1,2,5..8,11,12]	Ground	Analog ground for PLL[1,2,5..8,11,12].
NC	No Connect	Do not drive any signals into this pin.

Pin Name	Pin Type (1st, 2nd, and 3rd Functions)	Pin Description
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns it on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Arria GX device. In AS mode, DCLK is an output from the Arria GX device that provides timing for the configuration interface.
MSEL[3..0]	Input	Configuration input pins that set the Arria GX device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic-high level initiates reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects a POR time of about 12 ms and a logic low selects a POR time of about 100 ms.
		Optional/Dual-Purpose Configuration Pins
nCSO	I/O, Output	Output control signal from the Arria GX FPGA to the serial configuration device in AS mode that enables the configuration device.

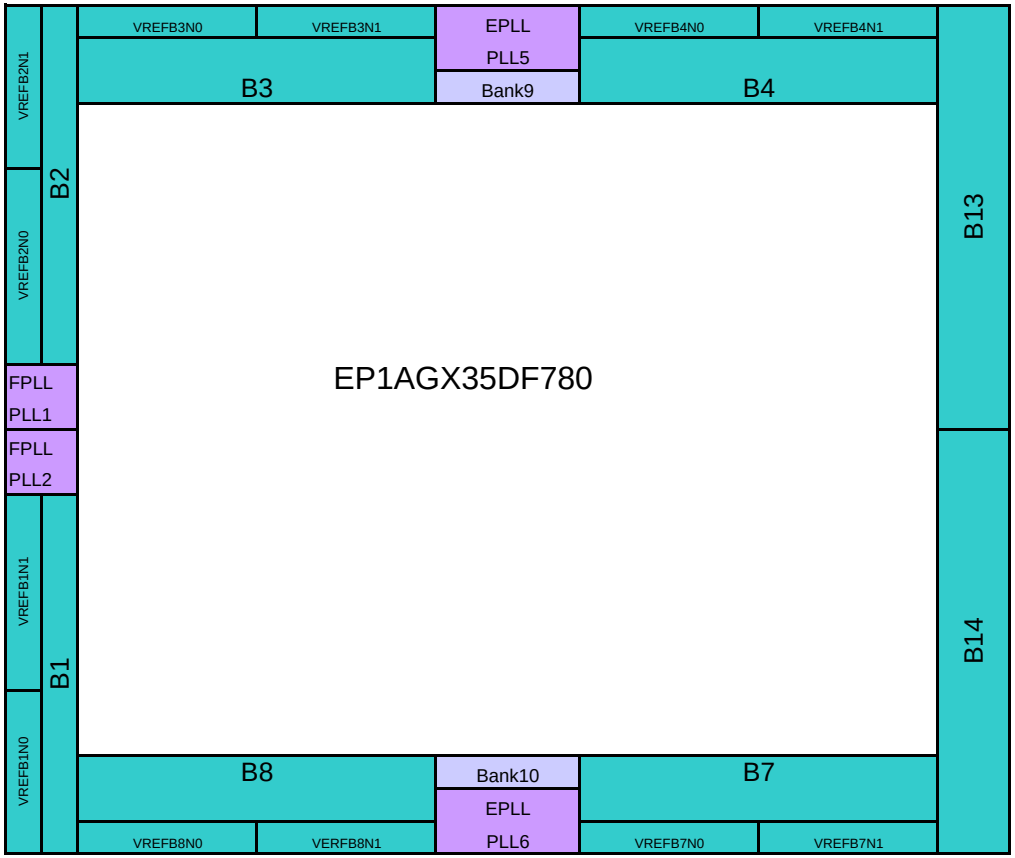
Pin Name	Pin Type (1st, 2nd, and 3rd Functions)	Pin Description
ASDO	I/O, Output	Control signal from the Arria GX FPGA to the serial configuration device in AS mode used to read out configuration data.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[6..1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[7..0] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
DATA7	I/O, Bidirectional	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal is strobed low.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
nCS, CS	I/O, Input	These are chip-select inputs that enable the Arria GX device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active-high enable, use the CS pin and drive the nCS pin low. If a design requires an active-low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.

Pin Name	Pin Type (1st, 2nd, and 3rd Functions)	Pin Description
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUnLU	I/O, Input	Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration modes, this pin is available as general-purpose user I/O pin.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
Clock and PLL Pins		
CLK[1,3]p	Clock, Input	Dedicated clock input pins 1 and 3 that can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins.
CLK[1,3]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins.
CLK[2,0]p/DIFFIO_RX_C[1,0]p	I/O, Clock	These pins can be used as I/O pins, clock input pins, or positive terminal data pins of differential receiver channels.
CLK[2,0]n/DIFFIO_RX_C[1,0]n	I/O, Clock	These pins can be used as I/O pins, negative clock input pins for differential clock input, or negative data pins of differential receiver channels.
CLK[4-7,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-7,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs.
FPLL[8..7]CLKp	Clock, Input	Dedicated positive clock inputs for fast PLLs (PLLs 7 and 8), which can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins.
FPLL[8..7]CLKn	Clock, Input	Dedicated negative clock inputs associated with the FPLL[7,8]CLKp pins, which can also be used for data inputs. These pins do not support OCT Rd and cannot be used as output pins. The programmable weak pull up resistor is not supported on these pins.
PLL5_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL5. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL5).

Pin Name	Pin Type (1st, 2nd, and 3rd Functions)	Pin Description
PLL5_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL5. If the clock outputs are single-ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL6_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL6. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL6).
PLL6_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL6. If the clock outputs are single-ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL11_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL11. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL11).
PLL11_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL11. If the clock outputs are single-ended, then each pair of pins (i.e., PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL12_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL12. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL12).
PLL12_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL12. If the clock outputs are single-ended, then each pair of pins (i.e., PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.
PLL[6..5]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or external clock outputs for PLL[6,5].
PLL[6..5]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[6,5]_FBp, or negative terminal clock output pins for differential clock output.
PLL[12..11]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or positive external clock outputs for PLL[12..11].
PLL[12..11]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[12..11]_FBp, or negative external clock output pins for differential clock output.
Dual-Purpose Differential and External Memory Interface Pins		
DIFFIO_RX[50..1]p	IO, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_RX[50..1]n	IO, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.

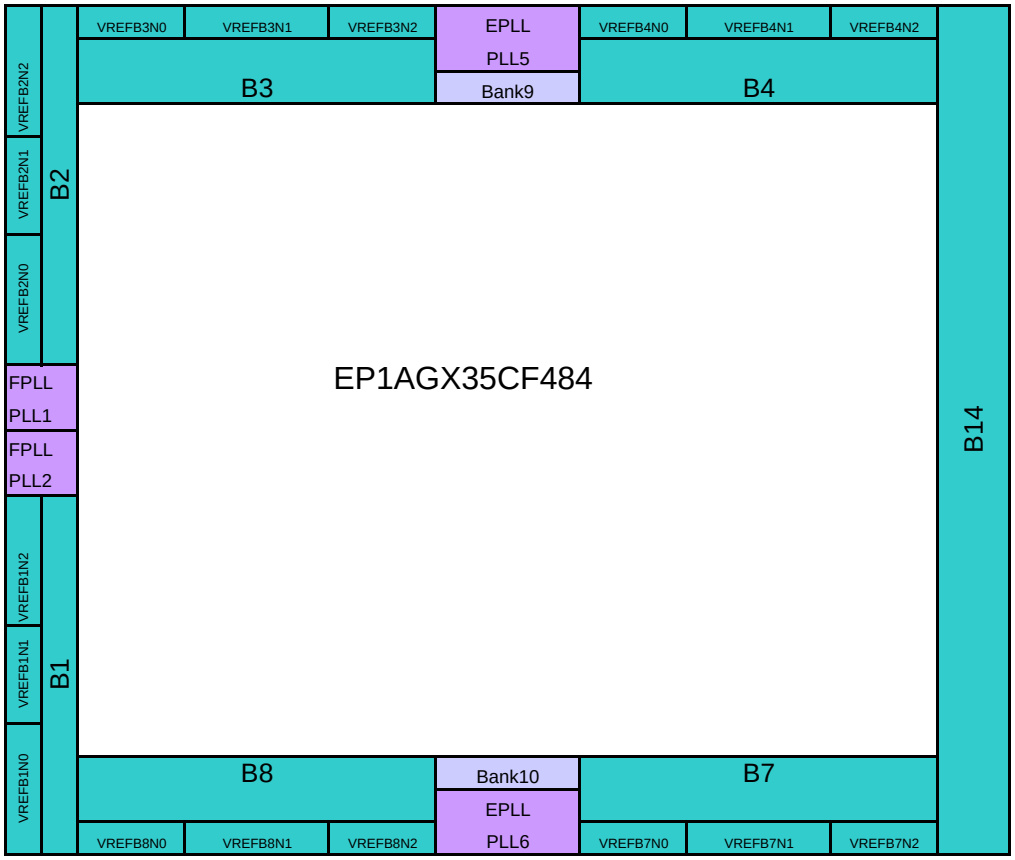
Pin Name	Pin Type (1st, 2nd, and 3rd Functions)	Pin Description
DIFFIO_TX[51..0]p	IO, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[51..0]n	IO, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[17..0][T,B]	DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQ[17..0][T,B]	DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
Transceiver (I/O Banks) Pins		
VCCP	Power	GX bank [15..13] PCS power. This power is connected to 1.2 V.
VCCR	Power	GX bank [15..13] receiver analog power. This power is connected to 1.2 V.
VCCT_B[15..13]	Power	GX bank [15..13] transmitter analog power. This power is connected to 1.2 V.
VCCA	Power	GX bank [15..13] analog power. This power is connected to 3.3 V.
VCCH_B[15..13]	Power	GX bank [15..13] transmitter driver analog power. This power is connected to 1.2 V or 1.5 V.
VCCL_B[15..13]	Power	GX bank [15..13] VCO analog power. This power is connected to 1.2 V.
GXB_RX[11..0]p	I, Input	High-speed positive differential receiver channels.
GXB_RX[11..0]n	I, Input	High-speed negative differential receiver channels.
GXB_TX[11..0]p	O, Output	High-speed positive differential transmitter channel.
GXB_TX[11..0]n	O, Output	High-speed negative differential transmitter channels.
REFCLK[0,1]_B[15..13]p	I, Input	High-speed differential I/O reference clock positive. This pin is powered by 1.2-V VCCT_B[15..13].
REFCLK[0,1]_B[15..13]n	I, Input	High-speed differential I/O reference clock negative. This pin is powered by 1.2-V VCCT_B[15..13].
RREFB[15..13]	I, Input	Reference resistor for GX side banks.

Note:
1) These descriptions are created based on the Arria GX device with the largest density, EP1AGX90E.



Notes:

1. This is a top view of the silicon die. For flip-chip packages, the die is mounted upside-down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus ® II software for exact locations.



Notes:

1. This is a top view of the silicon die. For flip-chip packages, the die is mounted upside-down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus II software for exact locations.

Version	Date	Changes Made
1.0	6/22/2007	Initial release
1.1	7/27/2007	Added F484 package
1.2	12/21/2007	Updated pin descriptions for VCCINT, VCCIO, TEMPDIODEp, and TEMPDIODEn
		Removed Bank 7 reference for GND pin AC7 (F780)/ Y2 (F484) in Pin List
1.3	9/8/2008	Removed RUP4,RUP7,RDN4,RDN7 from Pin List and Pin Definitions
1.4	5/21/2009	Removed TEMPDIODEp and TEMPDIODEn from Pin List and Pin Definitions