ALTERA®

think AND not OR

Altera @ 40 nm

What if you could design with the highest performance AND the lowest power? With the benefits of both FPGAs AND ASICs? With design software delivering the highest logic utilization AND the fastest compile times? You can, with Altera's new 40-nm Stratix® IV FPGAs and HardCopy® IV ASICs. Our devices deliver new levels of integration, freeing you to innovate without compromise.

So go ahead—think AND, not OR.

Innovation without compromise

We're proud to introduce the market's first 40-nm devices—our Stratix IV FPGA family and HardCopy IV ASIC family. Both device families, available with and without transceivers, deliver performance and power advantages that are ideal for large system-on-a-chip (SOC) designs. Along with our leading-edge Quartus® II design software, our newest programmable solutions deliver:

- The highest density, highest performance, AND lowest power
- Unprecedented system bandwidth AND superior signal integrity
- The benefits of FPGAs AND ASICs
- The highest performance, highest logic utilization, AND fastest compile times
- Earliest access to 40-nm technology AND a low-risk path to production

That's why Altera at 40 nm gives you the freedom to think AND, not OR.

Migrate your Stratix III designs to higher density Stratix IV FPGAs using Quartus II software.

Stratix IV E device package plan

Stratix FPGA series	Device	780-pin FBGA* (29 mm)	1,152-pin FBGA* (35 mm)	1,517-pin FBGA* (40 mm)	1,760-pin FBGA* (43 mm)
Stratix III E FPGA	EP3SL200			864, 88	
	EP3SE260			960, 112	
	EP3SL340			960, 112	1,104, 132
Stratix IV E FPGA	EP4SE110	480, 56			
	EP4SE230	480, 56			
	EP4SE290	480, 56	736, 88	864, 88	
	EP4SE360	480, 56	736, 88	864, 88	
	EP4SE530		736, 88	960, 112	960, 112
	EP4SE680		736, 88	960, 112	1,104, 132

480, 56 — Number indicates available user I/O pins, LVDS pairs

Vertical migration (same V_{CC}, GND, in-system programmability (ISP), and input pins)

All Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages.

*FBGA: FineLine BGA (flip chip)

Two variants per family, both resource rich

- Stratix IV E and GX FPGAs and HardCopy IV E and GX ASICs provide rich logic, memory, and digital signal processing (DSP) resources for diverse, high-end applications. Multiple Stratix IV E FPGA family members are pin-compatible with Stratix III FPGAs in the same package, so you can start your design with Stratix III FPGAs and later port to our newer and larger devices.
- Stratix IV GX FPGAs and HardCopy IV GX ASICs include the advantages of the same integrated transceiver block for high-bandwidth serial interface applications.

Highest density, highest performance, AND lowest power

Building on the advanced, proven Stratix III FPGA architecture, and through the advantages of 40-nm process technology, Stratix IV FPGAs give you the highest density, highest performance, and lowest power consumption.

Highest density and highest performance—

- Up to 680K high-performance logic elements (LEs)
- DSP blocks—with a parallel architecture and up to 1,360 embedded 18x18 multipliers running at 550 MHz, Stratix IV FPGAs deliver up to 748 GMACS of DSP performance, a level unmatched by competing devices
- TriMatrix memory—three memory block sizes with up to 22.4 Mbits of embedded memory running at 600 MHz
- An FPGA fabric that is two speed grades, or 35 percent, faster than that of the nearest competitor

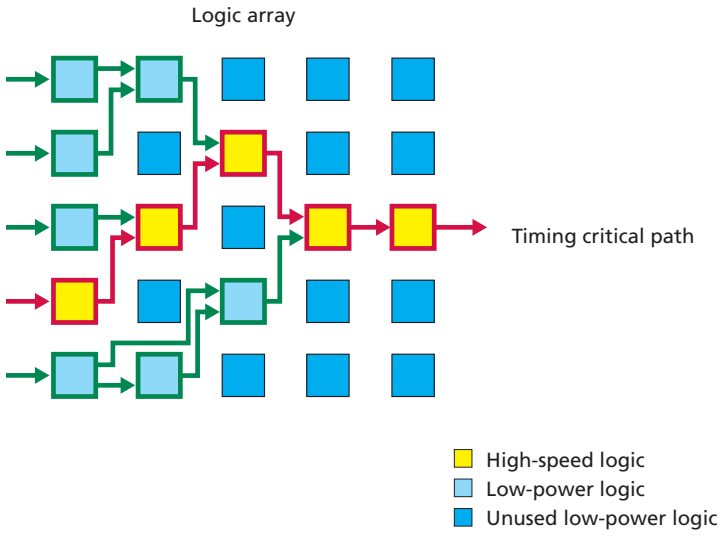
Lowest power—

- Programmable Power Technology automatically optimizes logic, DSP, and memory blocks for the lowest power at the required performance
- 50 percent less power consumption compared to competing devices
- Additional power consumption reduction of more than 50 percent, when you migrate your design from Stratix IV devices to HardCopy IV ASICs

Strengthening DSP performance

With peak performance rated at 748 GMACS, Stratix IV FPGAs achieve the highest DSP performance among FPGAs. Along with raw multiplier resources, the Stratix IV architecture also includes abundant logic, registers (about 400 registers per multiplier), and embedded memory bandwidth (more than 3,000 36-bit memory ports). This combination provides a critical advantage when implementing the highest performance DSP applications.

Stratix IV FPGA Programmable Power Technology



With Programmable Power Technology, power mapping is fully automated by Quartus II software, based on timing constraints. As a result, you get high performance where you need it, and lowest power everywhere else.

Stratix IV device family plan

Variant	Device	LEs	Transceivers (up to 8.5 Gbps[1])	Memory (Mbits)	Multipliers (18x18)
Stratix IV GX FPGA	EP4SGX70	70K	8	6.3	384
	EP4SGX110	110K	16	8.1	512
	EP4SGX230	230K	36	13.9	1,288
	EP4SGX290	290K	36	13.3	832
	EP4SGX360	360K	36	17.7	1,040
	EP4SGX530	530K	48	20.3	1,024
Stratix IV E FPGA	EP4SE110	110K	–	8.1	512
	EP4SE230	230K	–	13.9	1,288
	EP4SE290	290K	–	13.3	832
	EP4SE360	360K	–	17.7	1,040
	EP4SE530	530K	–	20.3	1,024
	EP4SE680	680K	–	22.4	1,360

Notes:
[1] Full-duplex serial transceivers

Unprecedented system bandwidth AND superior signal integrity

Transceiver-based Stratix IV GX FPGAs give you the resources to achieve a new level of system bandwidth. The device's high-performance core features up to 530K LEs, as well as high levels of transceiver and memory bandwidth:

- Up to 48 high-speed transceivers supporting data rates of up to 8.5 Gbps, including hard intellectual property (IP) protocols and signal integrity optimization blocks
- Up to four hard IP blocks for PCI Express (PCIe) compliant with PCIe Base Specification 2.0, 1.1, or 1.0, supporting x1, x2, x4, and x8 configurations. You'll also have support for end-port and root-port applications.
- LVDS support up to 1.6 Gbps
- Up to four 72-bit high-speed DDR3 interfaces at 1,067 Mbps (533 MHz)

The enhanced transceiver block in Stratix IV GX FPGAs supports key protocols including PCIe, Ethernet, Serial RapidIO®, GPON, CPRI, OBSAI, HyperTransport™ 3.0, SERDES Framer Interface Level 5 (SFI-5), and Interlaken. The block includes dynamically reconfigurable transceivers for selecting different protocols, data rates, and physical medium attachment (PMA) settings without interrupting adjacent transceiver channels.

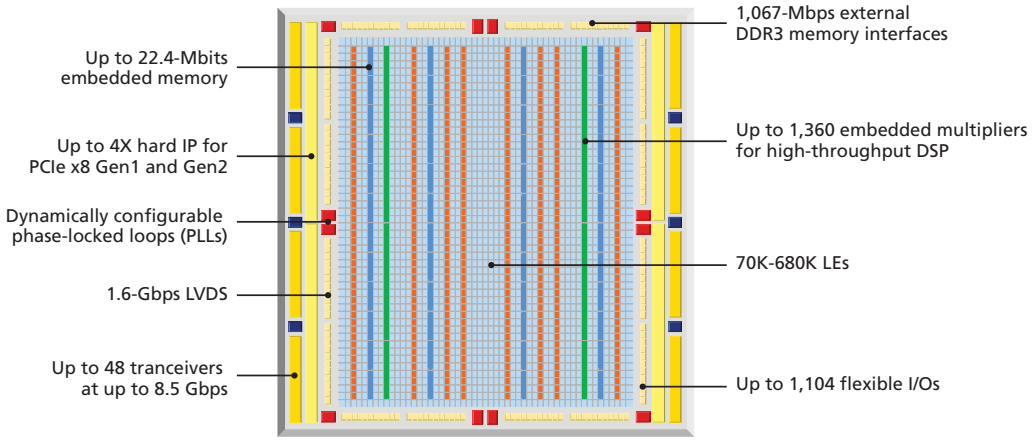
Stratix IV GX FPGAs feature transceiver and memory interfaces designed to deliver superior signal integrity:

- Dynamically reconfigurable transmit pre-emphasis and receiver equalization allow you to drive a 50-inch backplane on FR-4 at 6.375 Gbps
- Plug & Play Signal Integrity allows you to change the position of backplane cards on the fly, without having to manually reconfigure your backplane equalization settings, through two key functions:
  - Hot socketing, the ability to hot swap transceiver cards
  - Adaptive dispersion compensation engine (ADCE), which monitors and adjusts the receiver equalizer for the best eye opening
- Dedicated memory interface circuitry supports the latest high-performance memory interfaces; low simultaneous switching noise (SSN) and superior eye quality, through chip- and package-level enhancements, enable 1067-Mbps DDR3 interfaces

With these capabilities, you can design backplane systems with truly universal cards that can fit into multiple card positions. You also gain flexibility for a wide range of FPGA applications and configurations while enjoying low bit-error rate (BER) operation.

Stratix IV FPGAs deliver 2X the density and a two-speed-grade advantage over FPGAs from the nearest competitor, making them ideal for large designs in a variety of industries, from telecommunications to military to broadcast.

Stratix IV architectural elements



The benefits of FPGAs AND ASICs

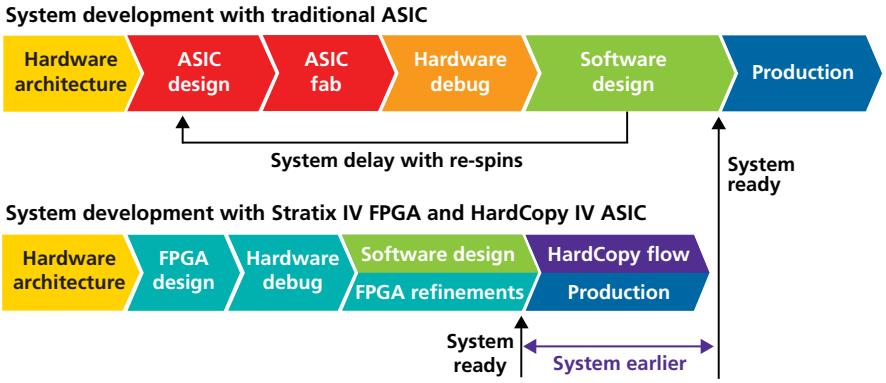
With an equivalent transceiver block and package- and pin-compatibility to Stratix IV GX FPGAs, HardCopy IV GX ASICs help you achieve the lowest risk and lowest total cost in ASIC designs with embedded transceivers. Experience the benefits of FPGAs with in-system, at-speed seamless prototyping using Stratix IV FPGAs, and completely prepare your system for production prior to ASIC handoff.

Altera uses a proven turnkey process to create low-cost, low-power, functionally equivalent, pin-compatible HardCopy IV ASICs in just 9 to 14 weeks. Our turnkey process includes full test insertion, so your design teams can focus on your innovative technology.

In short, HardCopy IV ASICs offer:

- More than 50 percent power consumption reduction, on average, over their FPGA prototypes
- Up to 100 percent increase in core performance
- 9 to 12 months saved in system time to market, through FPGA-based design and verification methodology
- Total development cost reduced to one-fifth that of standard-cell ASICs, through decreased design verification time and resources, EDA tooling costs, and NRE mask costs
- Increased single event upset (SEU) immunity and design security
- Significantly smaller die-sizes than the FPGA prototypes, lowering manufacturing costs

HardCopy design flow



HardCopy IV device family plan

Device	FPGA prototype	6.5+Gbps[1] SERDES	Memory (Mbits)	ASIC gates[2]
HardCopy IV GX ASIC	HC4GX1	8	6.3	2.8M
	HC4GX2	16	8.1	3.9M
	HC4GX3	24	12.2	9.2M
	HC4GX4	24	12.7	7.6M
	HC4GX5	24	13.3	9.5M
	HC4GX6	24	13.3	12.0M
HardCopy IV E ASIC	HC4E2	–	8.1	3.9M
	HC4E3	–	10.7	9.2M
	HC4E4	–	13.3	7.6M
	HC4E5	–	16.8	9.5M
	HC4E6	–	16.8	12.0M
	HC4E7	–	16.8	13.3M

Notes:

[1] Not all modes supported on all channels

[2] ASIC gates calculated as 12 gates per LE; 5,000 gates per 18x18 multiplier

Highest performance, highest logic utilization, AND fastest compile times

With a higher density device, you'll need a higher productivity design tool for faster design completion. Look to Quartus II software, the only design environment you'll need. Choose from soft and hard IP cores, and create two device implementations from a single design—one for Stratix IV FPGAs and one for HardCopy IV ASICs. With true hardware and software co-design and co-verification, you'll eliminate re-spins and avoid system delays to get to market faster.

Number one in performance and productivity for high-density FPGAs, Quartus II software v8.0 is the first FPGA vendor software to support 40-nm devices. The software offers many advantages:

- Performance optimization techniques, along with the Stratix IV FPGA routing architecture, result in optimal device performance—on average, a full two-speed-grade advantage over the nearest competitor.
- Advanced place-and-route algorithms, coupled with the logic architecture, enable you to achieve the highest logic utilization.
- Advanced place-and-route algorithms, with multiprocessor support, deliver compilation times that are three times faster than those of the nearest competitor. Further reduce compilation times by up to 70 percent with the software's incremental compilation feature, which compiles only the changed partitions in your design. Incremental compilation also supports a team-based design flow.

Quartus II software also includes industry-leading productivity features such as PowerPlay power optimization, TimeQuest timing analyzer, and SOPC Builder. These features automatically minimize power consumption, and enable faster timing closure and faster design development.

TSMC and Altera: 40-nm technology AND low-risk path to production

A leader in R&D, silicon volume, and quality, TSMC has been our manufacturing partner since 1993. As a team, we are redefining the foundry model, from design through tape-out and throughout manufacturing process development. Rather than working autonomously, as IC suppliers and foundries often do, we collaborate on both of our respective competencies. For example, as part of our standard operating procedure, we developed test chips on TSMC's 40-nm process technology. These test chips validated functionality of key IC components, minimizing product risks related to process and circuit design uncertainties.

Our 40-nm devices, built on TSMC's 40-nm process, provide the market's earliest access to leading-edge technology and the lowest-risk path to production. TSMC's 40-nm process technology features 193-nm immersion lithography, extreme low-k dielectrics, and strained silicon to enhance device performance and power efficiency.

Together, we're achieving faster, better results, and an unequalled track record of node-to-node success.

More reasons to think AND, not OR

Because true design success calls for a comprehensive set of resources, we complement our silicon and design software with embedded processors, embedded software development tools, pre-verified and configurable IP cores, development kits, and reference designs. Newly updated design resources to support our 40-nm devices include Nios® II embedded processors v8.0 and MegaCore® IP Library v8.0.

Nios II embedded processors v8.0 extend the embedded software capabilities of our 40-nm devices. With our latest version, you can add a memory protection unit to address the needs of safety-critical applications, or a memory management unit to provide both memory protection and virtual memory support. You can also:

- Accelerate time-critical software subroutines automatically by converting ANSI C code into hardware accelerators with the Nios II C-to-Hardware (C2H) Acceleration Compiler
- Add dozens of 300-MIPS processors in a single high-density device
- Add hardware accelerators to boost system performance and/or reduce system power consumption

Our MegaCore IP Library v8.0 introduces new hard IP for PCIe, compliant with PCIe Base Specification 2.0, 1.1, or 1.0 for Stratix IV GX FPGAs, supporting x1, x2, x4, and x8 configurations. Select and configure both hard and soft IP from a single GUI. This release also includes more video and image processing cores and adds many new features to existing IP functions.

Altera understands the requirements of end-market solutions that drive silicon and IP development. That's why we've created building blocks that ease integration of various functions, and continue to provide a robust ecosystem to source a variety of these IP cores.

Where Stratix IV FPGAs and HardCopy IV ASICs can help

Industry	Application
Wireline	20G/40G MSAN/MSPP, 4- and 8-port GPON OLT
Wireless	Basestations, high-end RF cards
Military	Radar and electronic warfare
Broadcast	Studio and head end
Storage	SAN controllers and switches
Medical imaging	Diagnostic imaging and therapy systems
Computing	High-performance computing
Automotive	Infotainment, gateway control
Aerospace	Commercial airliners

Ready to learn more?

With Altera at 40 nm, it's not about sacrificing one benefit to gain another. So if you're ready to think AND, not OR, contact your local Altera® sales representative or FAE, or visit our website for white papers, webcasts, and more on Stratix IV FPGAs and HardCopy IV ASICs.

www.altera.com/thinkANDnotOR

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