

Design Guidelines for Intel® FPGA DisplayPort Interface

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The design guidelines help you implement the Intel® FPGA DisplayPort IP core using Intel FPGA devices. These guidelines facilitate board designs for the Intel FPGA DisplayPort IP video interfaces.

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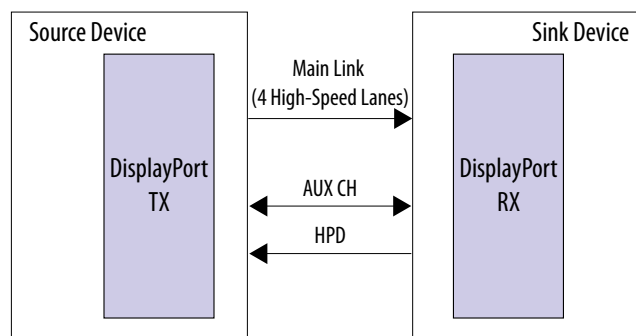
Intel FPGA DisplayPort Design Guidelines

The Intel FPGA DisplayPort interface consists of a Main link, an auxiliary channel (AUX CH), and a Hot-Plug Detect (HPD) signal.

- **Main Link**—Main Link is a unidirectional, high-bandwidth channel that transports video and audio over 1, 2, or 4 lanes at 8.1, 5.4, 2.7, and 1.62 Gigabits per second (Gbps) per lane. All lanes carry data. The clock is embedded in 8b/10b encoded serial data.
- **AUX CH**—The AUX CH is 1 Megabits per second (Mbps) half-duplex bidirectional channel used for link management and device control.
- **HPD**—The Intel FPGA DisplayPort sink device uses HPD to detect its presence. The HPD signal serves as an interrupt request by the DisplayPort sink device.

Figure 1: Intel FPGA DisplayPort Transport Channels

This figure shows the Intel FPGA DisplayPort link between a source and a sink device.



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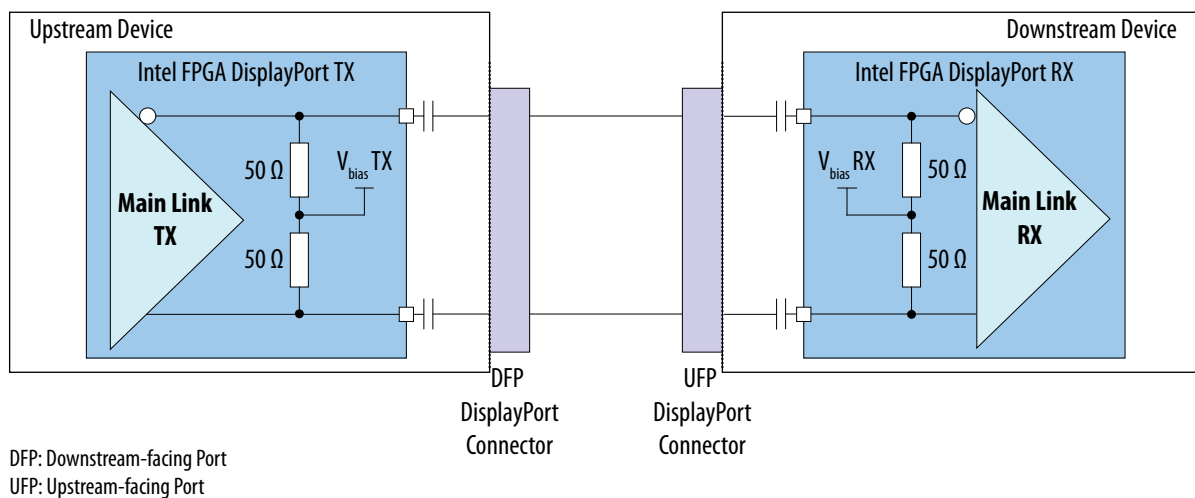
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Main Link

The Intel FPGA DisplayPort Main Link is a unidirectional, high-bandwidth channel used to transport video and audio data.

Figure 2: Main Link Differential Pair with FPGA Transceiver PHY

This figure shows a Main Link differential pair. The Intel FPGA DisplayPort source must have AC-coupling capacitors. AC-coupling for Intel FPGA DisplayPort sink is optional.



Main Link TX

The Main Link TX drives doubly-terminated AC-coupled differential pairs.

The FPGA Transceiver PHY TX includes on-chip 100 ohm differential termination and bias voltage generation. You may add a repeater such as a retimer or a redriver in between the FPGA and the external DisplayPort connector to compensate for loss.

Table 1: FPGA Transceiver PHY TX Operation Guidelines

FPGA Transceiver PHY Operations	Description
<p>Transceiver PHY TX Reference Clock Connection</p>	<p>A free-running 135 MHz differential clock (e.g. LVDS) is AC-coupled to a dedicated reference clock input of the transceiver bank. The reference clock input supports on-chip termination (OCT).</p> <p>Enable OCT using a QSF assignment:</p> <ul style="list-style-type: none"> • Intel Arria® 10 devices <pre>set_instance_assignment -name XCVR_A10_REFCLK_TERM_TRISTATE TRISTATE_OFF -to <dedicated refclk pin name></pre> • Intel Cyclone® 10 GX devices <pre>set_instance_assignment -name XCVR_C10_REFCLK_TERM_TRISTATE TRISTATE_OFF -to <dedicated refclk pin name></pre> • Arria V, Cyclone V, and Stratix V devices <pre>set_instance_assignment -name XCVR_REFCLK_PIN_TERMINATION AC_COUPLING -to <dedicated refclk pin name></pre> <p>Note: Your design does not require external termination if OCT is enabled.</p>
<p>Transceiver TX On-Chip Termination</p>	<p>By default, the Intel Quartus® Prime software enables differential 100 ohm OCT and bias voltage generation. Your design does not require external 50 ohm termination and bias voltage (v_{bias_TX}).</p>
<p>Transceiver TX Channel Bonding</p>	<p>Bonding TX channels reduces on-chip channel-to-channel skew, which allows more skew margin at the board or system level to meet the Intel FPGA DisplayPort Source inter-lane skew requirement.</p> <p>Refer to Table 2 for more information.</p>

FPGA Transceiver PHY Operations	Description
Transceiver TX Voltage Swing and Pre-emphasis	<p>DisplayPort TX specification for the Main Link allows four differential peak-to-peak voltage swing levels, and four pre-emphasis (Post Cursor1) levels. Certain combinations of voltage swing levels and pre-emphasis levels that result in differential peak-to-peak swing outside the allowable range (1.38 V) are not allowed.</p> <p>The reconfiguration management module available in the Intel Quartus Prime design example includes a sub-module that translates the DisplayPort voltage swing and pre-emphasis levels to the FPGA transceiver setting. Refer to Table 3 for more information.</p> <p>Use the reconfiguration management file and a sub-module of the Intel Quartus Prime design examples that maps the DisplayPort levels to the transceiver analog parameter setting.</p> <ul style="list-style-type: none"> • Intel Arria 10 devices <ul style="list-style-type: none"> Reconfiguration management module : <code>bitec_reconfig_alt_a10.v</code> Sub-module: <code>tx_analog</code> mappings • Intel Cyclone 10 GX devices <ul style="list-style-type: none"> Reconfiguration management module : <code>bitec_reconfig_alt_c10.v</code> Sub-module: <code>tx_analog</code> mappings • Arria V devices <ul style="list-style-type: none"> Reconfiguration management module : <code>bitec_reconfig_alt_av.v</code> Sub-module: <code>dp_analog</code> mappings • Cyclone V devices <ul style="list-style-type: none"> Reconfiguration management module : <code>reconfig_mgmt_hw_ctrl.v</code> Sub-module: <code>dp_analog</code> mappings • Stratix V devices <ul style="list-style-type: none"> Reconfiguration management module : <code>bitec_reconfig_alt_sv.v</code> Sub-module: <code>dp_analog</code> mappings

FPGA Transceiver PHY Operations	Description
<p>TX Repeater (Redriver or Retimer)</p>	<p>To mitigate system signal losses, you may place a redriver or retimer between the FPGA and the external DisplayPort connector for a box-to-box connection. In such designs, place the repeater close to the external DisplayPort connector and generate the DisplayPort signals at the voltage and pre-emphasis levels determined during link training, instead of the FPGA.</p> <p>In this case, you can turn off the Support analog reconfiguration option in the Intel FPGA DisplayPort parameter editor and set the FPGA voltage swing in the QSF assignments. The selection of the appropriate signaling level between the FPGA and the repeater depend on the PCB loss and the equalization of the redriver/retimer input. The typical setting for the transmitter is 400 mV voltage swing without pre-emphasis.</p> <p>Refer to Table 4 for more information.</p>

Bonded TX channels placed in a single transceiver bank results in lower channel-to-channel skew, allowing more skew budget at the board level. For information about the maximum channel-to-channel skew, refer to the *Device Datasheet*.

You have the option to select bonding mode through the Transceiver PHY parameter editor.

Table 2: Bonding Mode Selection Guidelines

Device Family	Transceiver PHY Bonding Mode	Notes
<p>Intel Arria 10/Intel Cyclone 10 GX</p>	<p>PMA and PCS bonding</p>	<ul style="list-style-type: none"> Requires bonded TX channels to be placed contiguously Channel 0 is selected as a bonding master Uses x6/xN clock network driven by Master Clock Generation Block (MCGB). MCGB is enabled in the TX PLL (e.g. fPLL) parameter editor. <p>Note: The digital reset signal (<code>tx_digitalreset</code>) to all TX channels within a bonded group must meet a maximum skew tolerance of one-half the TX parallel clock cycle (<code>tx_clkout</code>). Refer to the <i>Timing Constraints for Bonded PCS and PMA Channels</i> section of the respective <i>Transceiver PHY User Guides</i> for more information.</p>

Device Family	Transceiver PHY Bonding Mode	Notes
Arria V	xN	–
Stratix V	x6/xN	–

Table 3: Recommended Combinations of Voltage Swing and Pre-Emphasis Levels

This table lists the 4 levels of voltage swing level defined in the *Video Electronics Standards Association (VESA) DisplayPort Standard*. The combination of these levels is independent of the devices. Intel FPGA devices support all 4 levels. The mapping between the DisplayPort levels and the actual PMA values is provided in the Intel FPGA DisplayPort design examples.

Voltage Swing Level	Pre-Emphasis Level			
	0	1	2	3
0	Supported	Supported	Supported	Supported
1	Supported	Supported	Supported	Not allowed
2	Supported	Supported	Not allowed	Not allowed
3	Supported	Not allowed	Not allowed	Not allowed

Table 4: Guidelines on the Usage of the TX Repeater Device

Device Family	DisplayPort version 1.2 Rates (RBR, HBR, HBR2)	DisplayPort version 1.4 Rate (HBR3)	Example Repeater
Intel Arria 10	Not Required	Not Required	–
Intel Cyclone 10 GX	Not Required	Not Required	–
Arria V	Recommended	Not Applicable ⁽¹⁾	TI SN75DP130 (Redriver)
Cyclone V	Recommended	Not Applicable ⁽¹⁾	TI SN75DP130 (Redriver)
Stratix V	Not Required	Not Applicable ⁽¹⁾	–

Main Link TX Electrical Specifications

Use the listed Main Link transmitter electrical parameters for reference. Refer to the *VESA DisplayPort Standard* for other transmitter electrical parameters.

Table 5: TP2 (TX External Connector)

Note: The Lane-to-Lane Output Skew specification at TP2 in *VESA DisplayPort Standard* version 1.2a differs from version 1.4.

⁽¹⁾ This device does not support HBR3 data rate.

Parameter	Minimum	Typical	Maximum	Notes
Maximum Output Voltage Level	–	–	1.38 V	Maximum differential peak-to-peak swing for all output level and pre-emphasis combinations
Lane-to-Lane Output Skew	–	–	1250 ps	VESA DisplayPort Standard version 1.4 for all data rates
Lane-to-Lane Output Skew (HBR, RBR)	–	–	2 UI	VESA DisplayPort Standard version 1.2a for HBR and RBR
Lane-to-Lane Output Skew (HBR2)	–	–	4 UI + 500 ps	VESA DisplayPort Standard version 1.2a for HBR2

Table 6: TP3_EQ (Compliance Cable Model with Reference Receiver Equalizer)

Parameter	Minimum	Typical	Maximum	Notes
Maximum TX Total Jitter	–	–	0.65 UI	For HBR3, TPS4 pattern, at 1E-9
	–	–	0.62 UI	For HBR2, CP2520 pattern, at 1E-9
	–	–	0.40 UI	For HBR2, D10.2 pattern, at 1E-9
TX Differential Peak-to-Peak EYE Voltage at HBR3	75 mV	–	–	For HBR3, TPS4 pattern, at 1E-9
TX Differential Peak-to-Peak EYE Voltage at HBR2	90 mV	–	–	For HBR2, CP2520 pattern, at 1E-9

Note: For more information about TP2 and TP3_EQ compliance measurement points and reference receiver equalizer, refer to the *VESA DisplayPort Standard*.

Main Link RX

The FPGA Transceiver PHY RX includes on-chip 100 ohm differential termination and bias voltage generation.

You may add an RX repeater such as a retimer or a redriver in between the FPGA and the external DisplayPort connector to clean up jitter and compensate for losses. AC-coupling is optional for Main Link RX.

Table 7: FPGA Transceiver PHY RX Operation Guidelines

FPGA Transceiver PHY Operations	Description
Transceiver RX On-Chip Termination	By default, the Intel Quartus Prime software enables differential 100 ohm OCT and bias voltage generation. Your design does not require external 50 ohm termination and bias voltage (<code>v_{bias_RX}</code>).

FPGA Transceiver PHY Operations	Description
RX Repeater (Redriver or Retimer)	<p>To clean up jitter and compensate for signal losses, a sink device uses a redriver or retimer between the external DisplayPort connector and the FPGA RX. In such systems, the device places the repeater close to the external DisplayPort connector and regenerates the received DisplayPort signals.</p> <ul style="list-style-type: none"> The retimer includes the clock and data recovery (CDR) circuit that cleans up the jitter. The redriver does not have a CDR circuit. <p>Refer to Table 8 for more information.</p>

Table 8: Guidelines on the Usage of the RX Repeater Device

Device Family	VESA DisplayPort Standard version 1.2a Rates (RBR, HBR, HBR2)	VESA DisplayPort Standard version 1.4 Rate (HBR3)	Example Repeater
Intel Arria 10/Intel Cyclone 10 GX	Not Required	Required	Parade Technologies PS8460 (Retimer) ⁽²⁾
Arria V	Recommended	Not Applicable ⁽³⁾	TI SN75DP130 (Redriver)
Cyclone V	Recommended	Not Applicable ⁽³⁾	TI SN75DP130 (Redriver)
Stratix V	Not Required	Not Applicable ⁽³⁾	–

Main Link RX Electrical Specifications

Use the listed Main Link receiver electrical parameters for reference. Refer to the *VESA DisplayPort Standard* for other receiver electrical parameters.

Table 9: TP3_EQ

Parameter	Minimum	Typical	Maximum	Notes
Minimum Receiver EYE Width at HBR3	0.35 UI	–	–	For HBR3, TPS4 pattern
RX Differential Peak-to-Peak EYE Voltage at HBR3	75 mV	–	–	

⁽²⁾ The *VESA DisplayPort PHY Compliance Test Specification (CTS) version 1.4* passed in Intel Arria 10 device using Parade Technologies PS8460 Retimer in RX. For other vendors' device recommendation, please contact your nearest Intel sales representative.

⁽³⁾ This device does not support HBR3 data rate.

Parameter	Minimum	Typical	Maximum	Notes
Minimum Receiver EYE Width at HBR2	0.38 UI	–	–	
RX Differential Peak-to-Peak EYE Voltage at HBR2	70 mV	–	–	For HBR2, CP2520 pattern

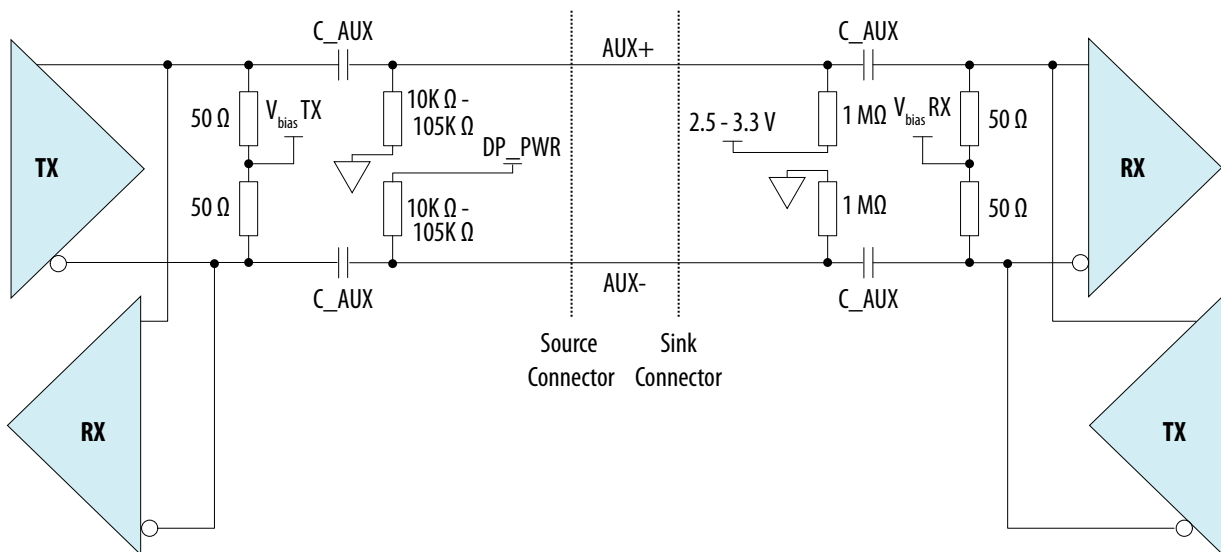
Note: For more information about TP3_EQ compliance measurement point and reference receiver equalizer, refer to the *VESA DisplayPort Standard*.

AUX Channel

The DisplayPort AUX channel is a half-duplex, bidirectional channel running at 1 Mbps rate.

Figure 3: AUX Channel Differential Pair

The AUX channel is a differential pair doubly-terminated with 50 ohm resistors and AC-coupled at both source and sink devices.

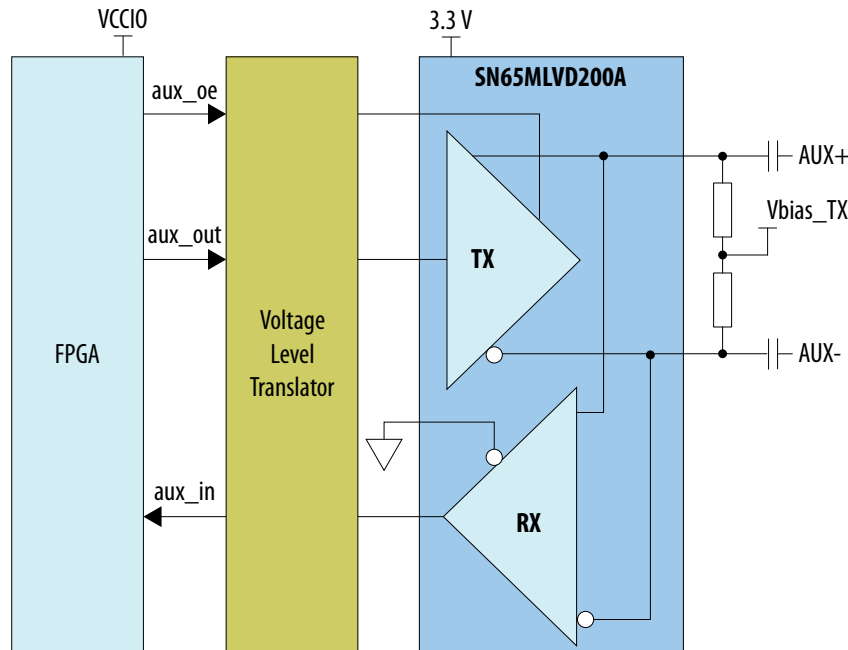


Implementing Bidirectional LVDS

You can implement half-duplex, bidirectional LVDS using either an external LVDS line driver/receiver or on-chip Bus LVDS interface.

Figure 4: External LVDS Line Driver/Receiver

The figure shows an example of an external LVDS driver/receiver, TI SN65MLVD200A used in Bitec HSMC DisplayPort daughter card.



The interface to the device is straightforward. For example, TI SN65MLVD200A requires three LVTTL general purpose I/O pins (`aux_oe`, `aux_out`, `aux_in`). If the FPGA bank I/Os are not tolerant with LVTTL, a level shifter is required, as shown in the figure above.

There may be crosstalk from the single-ended LVTTL signals to the Main-Link high speed signals if the traces are routed close to each other. During board signal integrity (SI) design, pay special attention to routing.

Note: The Intel FPGA DisplayPort design examples are developed based on the Bitec DisplayPort daughter card using TI SN65MLVD200A.

For more information about the BLVDS driver, TI SN65MLVD200A, refer to the [SN65MLVD20xx Multipoint-LVDS Line Driver and Receiver datasheet](#).

Detection of DisplayPort Upstream Source Device

The DisplayPort sink device senses the AUX+ and AUX- signal logic level to detect the upstream source.

The weak pullup and pulldown resistors form a voltage divider that allows the sink device to detect the presence of the upstream source device.

Between the AC-coupling capacitor and the DisplayPort connector:

- The source device weakly pulls down the AUX+ line to GND and weakly pulls up the AUX- line to DP_PWR (typically 3.3 V) with nominal 100K ohm resistors.
- The sink device weakly pulls up the AUX+ line to 3.3 V and weakly pulls down the AUX- line to GND with nominal 1M ohm resistors.

The AUX+ and AUX- lines connect to the FPGA through 10K ohm resistors (e.g. `RX_SENSE_P` and `RX_SENSE_N` signals in the Bitec DisplayPort daughter card). The Intel FPGA DisplayPort sink senses the logic level of the AUX+ and AUX- lines using the `rx_cable_detect` and `rx_pwr_detect` inputs and triggers the HPD signal when the powered upstream source device is detected.

The sense signals require level translation if they are connected to an FPGA I/O that is not 3.3V tolerant, for example, Intel Arria 10 device bank with `VCCIO = 1.8 V`.

DisplayPort Hot Plug Detect (HPD)

The DisplayPort sink device drives the HPD signal using 3.3V TTL signal level. The upstream DisplayPort source device monitors the HPD signal.

To prevent the HPD signal from floating when not connected, tie to GND with a >100K ohm resistor in both the Intel FPGA DisplayPort source and sink devices.

Note: The voltage level of the HPD pin uses 3.3 V TTL. FPGA I/Os that are not tolerant with 3.3V TTL require a level shifter.

DisplayPort Power

For Box-to-Box DisplayPort connection, the DisplayPort source and sink devices provide a power pin and a return current pin on the connector.

This power is provided by the DisplayPort source and sink to power up attached devices such as a Branch device or an Active Cable Assembly.

As per the *VESA DisplayPort Standard*, the maximum current drawn by an attached device is 0.5 A at 3.3V setting.

Bitec DisplayPort Daughter Card Revisions

The schematic diagrams of the Bitec HSMC and FMC DisplayPort daughter cards show the connectivity for Intel FPGA development boards.

Table 10: Bitec DisplayPort FMC Daughter Card Revisions

Revision	Release Date	Change	Note
Rev. 10	TBD	Added Parade Technologies Retimer (PS8460) on RX	<i>VESA DisplayPort PHY CTS version 1.4</i> passed in Intel Arria 10 device
Rev. 5	January 2015		<ul style="list-style-type: none"> TX lane polarity inverted TX lane order reversed No redriver/retimer used Used for developing the Intel FPGA DisplayPort design example in version 17.0 of the Intel Quartus Prime software.

Related Information

- [Schematic Diagram for HSMC DisplayPort Daughter Card Revision 11](#)
- [Schematic Diagram for FMC DisplayPort Daughter Card Revision 8](#)

Document Revision History for AN 745: Design Guidelines for Intel FPGA DisplayPort Interface

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Date	Version	Changes
January 2018	2018.01.22	<ul style="list-style-type: none">Removed all information about the Intel FPGA HDMI interface to <i>AN 837: Design Guidelines for Intel FPGA HDMI</i>.Changed the title of this document to <i>AN 745: Design Guidelines for Intel FPGA DisplayPort Interface</i>.Added specific guidelines for Main Link RX and TX.Added information about receiver electrical parameters.Added guidelines for DisplayPort Power.Removed the schematic diagrams and provided links to the diagrams on the Bitec product page.
November 2015	2015.11.02	Initial release.

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