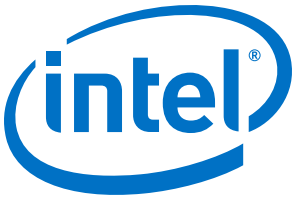


AN 916: JESD204C Intel® FPGA IP and ADI AD9081/AD9082 MxFE* Interoperability Report for Intel® Stratix® 10 E-Tile Devices

AN-916 | 2020.06.22
Latest document on the web: PDF | HTML

Contents

1. JESD204C Intel® FPGA IP and ADI AD9081/AD9082 MxFE* Hardware Checkout Report for Intel® Stratix® 10 E-Tile Devices

The JESD204C Intel® FPGA IP is a high-speed point-to-point serial interface intellectual property (IP).

TheJESD204C Intel FPGA IP has been hardware-tested with selected JESD204C-compliant analog-to-digital converter (ADC) and digital-to-analog converter (DAC) device.

This report highlights the interoperability of the JESD204C Intel FPGA IP with the AD9081 MxFE evaluation board AD9081-FMCA-EBZ from Analog Devices. The following sections describe the hardware checkout methodology and test results. The AD9082 MxFE evaluation board is also supported.

The AD9081 MxFE evaluation board is provided by Analog Devices with bring up and configuration support from Analog Devices.

The AD9081 and AD9082 are high integration devices with the following features:

- AD9081:
  - 16-bit, 12 GSPS maximum sample rate radio frequency (RF) DAC core.
  - 12-bit, 4 GSPS rate RF ADC core.
  - 16-lane, 24.75 Gbps JESD204C or 15.5 Gbps JESD204B data transceiver port.
  - On-chip clock multiplier.
  - Digital signal processing capability targeted at single- and dual-band direct-to-RF radio applications.
- AD9082:
  - 16-bit, 12 GSPS maximum RF DAC core.
  - 12-bit, 6 GSPS rate RF ADC core.
  - 16-lane, 24.75 Gbps JESD204C or 15.5 Gbps JESD204B data transceiver port.
  - On-chip clock multiplier.
  - Digital signal processing capability targeted at multiband direct-to-RF radio applications.

For more information about the AD9081 and AD9082, refer to *AD9081 Datasheet and Product Info* and *AD9082 Datasheet and Product Info*.

Related Information

- JESD204C Intel FPGA IP User Guide
- AD9081 Datasheet and Product Info

- AD9082 Datasheet and Product Info

1.1. Hardware Requirements

The hardware checkout test requires the following hardware and software tools:

- Intel Stratix® 10 TX Signal Integrity (SI) Development Kit (Production Rev B Edition) with Intel Stratix 10 1ST280EY2F55E1VG (transceiver E-tile) device
- Analog Devices AD9081 MxFE AD9081-FMCA-EBZ
- Mini-USB cable
- SMA cables
- Pulse generator

Related Information

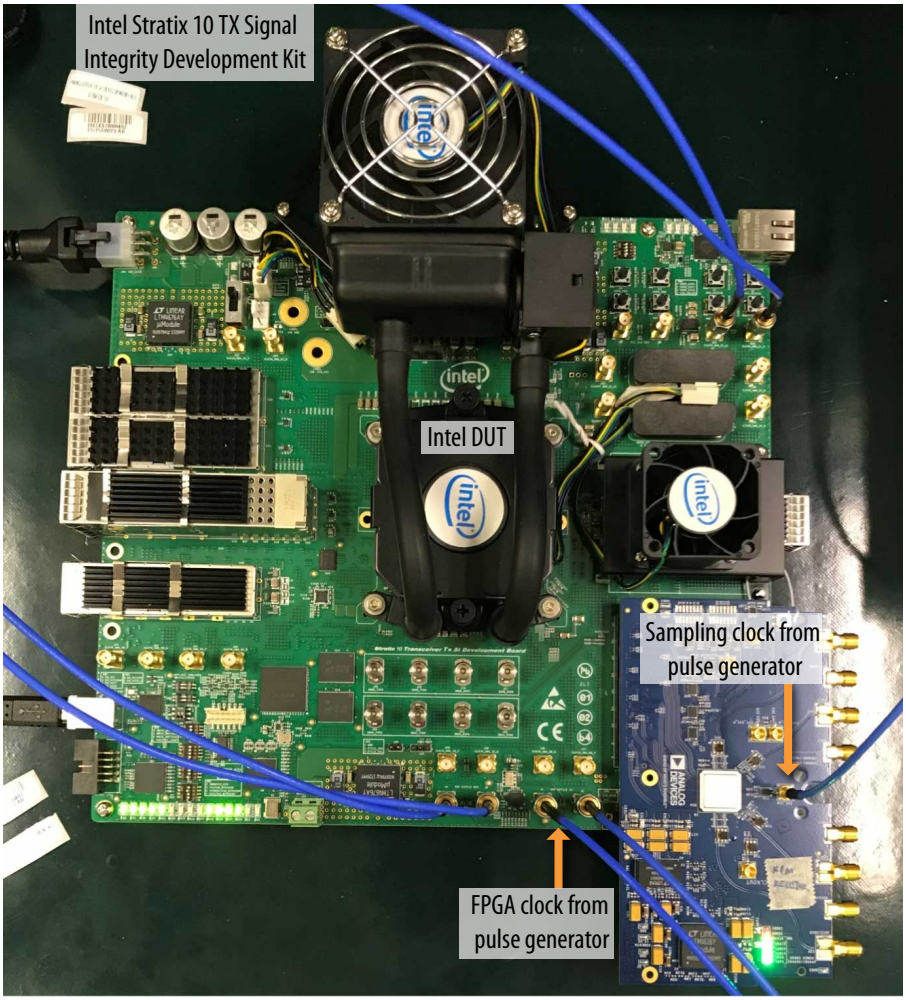
Intel Stratix 10 TX Signal Integrity Development Kit

1.2. Hardware Setup

An Intel Stratix 10 TX SI Development Kit (Production Rev B Edition) is used with the Analog Devices AD9081 daughter card module installed to the FMC+ connector of the development board.

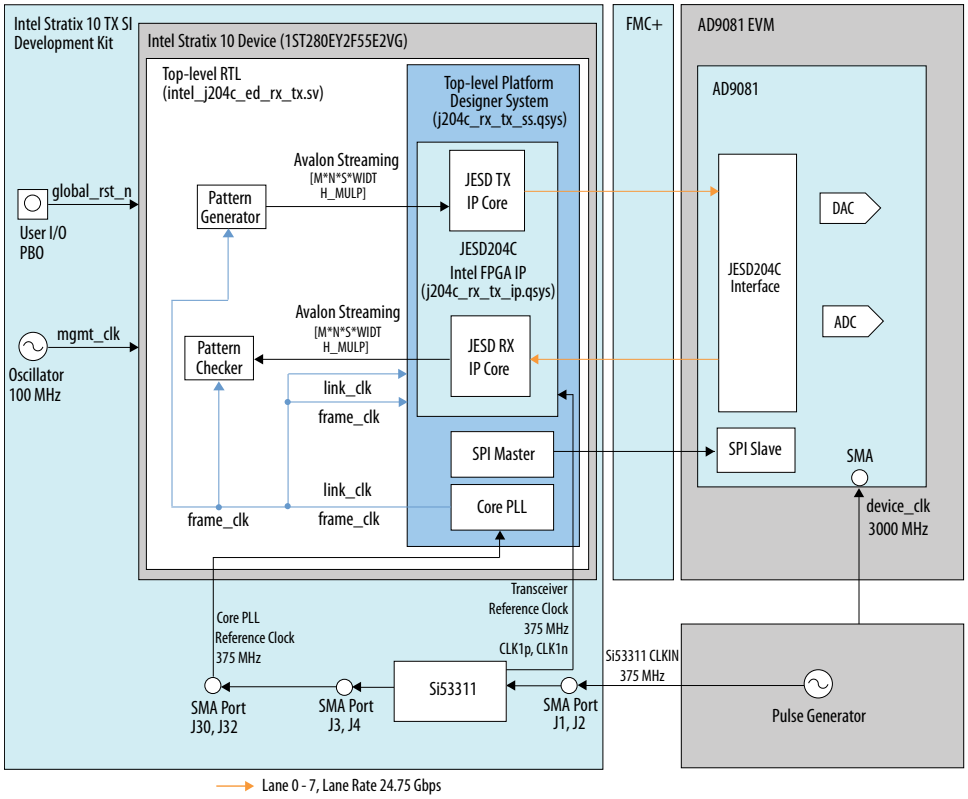
- The AD9081 EVM derives power from the FMC+ pins.
- The FPGA reference clock is supplied by a pulse generator through an SMA cable.
- The pulse generator provides device clock to the MxFE on the AD9081 EVB through an SMA cable.

Figure 1. Hardware Setup



The following system-level diagram shows how the different modules connect in this design.

Figure 2. System Diagram



In this setup, where LMF = 882, the data rate of the transceiver lanes is 24.75 Gbps. The pulse generator is used to provide reference clock to the clock generator Si53311. The core PLL reference clock and the transceiver reference clock is generated by the clock generator Si53311.

For FCLK_MULP=2, the core PLL generates 187.5 MHz link clock and 375 MHz frame clock. The pulse generator also provides the AD9081 device clock of 3000 MHz. The SPI master in the FPGA programs the AD9081 registers through the 4 wire SPI interfaces via FMC pins. The converters operate in a single JESD link in all configurations with a maximum of 8 lanes.

1.3. JESD204C Intel FPGA IP and ADC Hardware Checkout

1.3.1. ADC Hardware Checkout Methodology

The following section describes the test objectives, procedure, and the passing criteria. The test covers the following areas:

- Receiver data link layer
- Receiver transport layer

1.3.1.1. Receiver Data Link Layer

This test area covers the test cases for sync header alignment (SHA) and extended multiblock alignment (EMBA).

The JESD204C RX IP will start link operation after `rx_rst_n` is deasserted. In a typical user application, all run-time registers should be configured when the Avalon® memory-mapped configuration space is out of reset, and before the link and transport layers are out of reset. Upon `rx_rst_n` deassertion, the JESD204C RX IP will perform SHA and EMB alignment.

1.3.1.1.1. Sync Header Alignment

Table 1. SHA Test Cases

Test Case	Objective	Description	Passing Criteria
SHA.1	Check if Sync Header Lock is asserted after the completion of reset sequence.	The following signals in `<ip_variant_name>_base.v` are tapped: • `j204c_rx_rst_n` • `j204c_rx_sh_lock` • `j204c_rx_int` The `rxlink_clk` is used as the sampling clock for the Signal Tap.	• The `j204c_rx_sh_lock` is asserted after the deassertion of `j204c_rx_rst_n`. • The `j204c_rx_int` signal should stay low if there is no error.
SHA.2	Check Sync Header Lock status after sync header lock is achieved (or during the EMBA phase) and stable.	The following signals in `<ip_variant_name>_base.v` are tapped: • `j204c_rx_sh_lock` • `j204c_rx_int` The `rxlink_clk` is used as the sampling clock for the Signal Tap.	• The `j204c_rx_sh_lock` should remain asserted.(1) • The `j204c_rx_int` signal should stay low if there is no error.(2)

1.3.1.1.2. Extended Multiblock Alignment (EMBA)

Table 2. EMBA Test Cases

Test Case	Objective	Description	Passing Criteria
EMBA.1	Check if extended multiblock lock is asserted only after the assertion of sync header lock.	The following signals in `<ip_variant_name>_base.v` are tapped: • `j204c_rx_emb_lock` • `j204c_rx_int`	• The `j204c_rx_emb_lock` is asserted after assertion of `j204c_rx_sh_lock`. • The `j204c_rx_int` signal should stay low if there is no error.
EMBA.2	Check if extended multiblock lock status is stable (after extended multiblock lock or until elastic	The following signals in `<ip_variant_name>_base.v` are tapped: • `j204c_rx_emb_lock` • `j204c_rx_int` The `rxlink_clk` is used as the sampling clock for the Signal Tap.	• The `j204c_rx_emb_lock` should remain asserted.(3) • The `j204c_rx_int` signal should stay low if there is no error.

continued...

(1) The `j204c_rx_sh_lock` signal should remain asserted after 12 hours.

(2) The `j204c_rx_int` signal should not be asserted after 12 hours.

(3) The `j204c_rx_emb_lock` signal should remain asserted after 12 hours.

Test Case	Objective	Description	Passing Criteria
	buffer is released) along with no invalid multiblock.		
EMBA.3	Check the lane alignment.	The following signals in <*ip_variant_name*>_base.v are tapped: • j204c_rx_dev_lane_align • j204c_rx_int The rxlink_clk is used as the sampling clock for the Signal Tap.	• The j204c_rx_dev_lane_align is asserted after the assertion of j204c_rx_emb_lock and next LEMC event. • The j204c_rx_int signal should stay low if there is no error.

1.3.1.2. Receiver Transport Layer

To check the data integrity of the data stream through the JESD204C receiver IP core and transport layer, the ADC is configured to output the ramp test data pattern. The ADC is also set to operate with the same configuration as set in the JESD204C IP core. The ramp checker in the FPGA fabric checks data integrity for 12 hours.

This figure shows the conceptual test setup for data integrity checking.

Figure 3. Data Integrity Check Using RAMP Pattern Checker

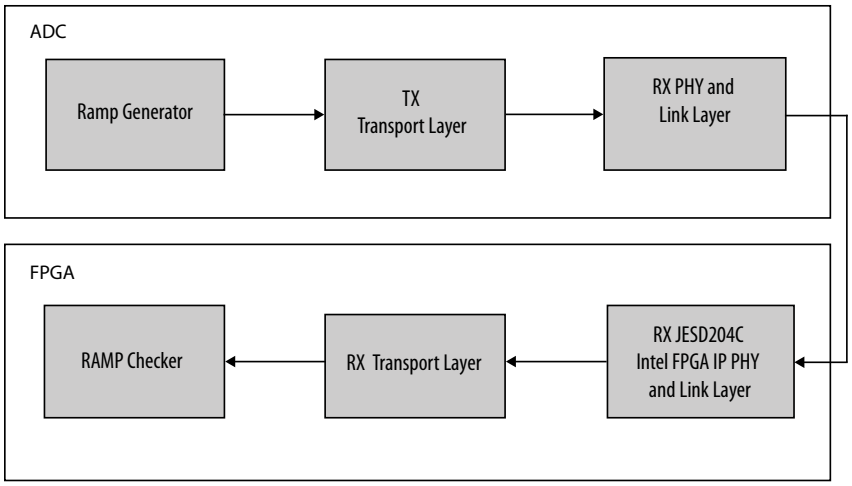


Table 3. RX Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
RXTL.1	Check the transport layer mapping of the data channel using ramp test pattern.	The following signals in <*ip_variant_name*>_base.v are tapped: • j204c_rx_avst_valid • j204c_rx_avst_ready • j204c_rx_avst_data [(M*S*WIDTH_MULP*N)-1:0][4][5][6][7] • rx_patchk_data_error_int	• The j204c_rx_avst_valid is asserted. • The j204c_rx_avst_ready is asserted. • The rx_patchk_data_error_int should stay low if there is no error.

(4) M is the number of converters.

Test Case	Objective	Description	Passing Criteria
		The `rxframe_clk` is used as the sampling clock for the Signal Tap. The `rx_patchk_data_error_int` signal indicates a pass or fail for the ramp checker.	

1.3.2. JESD204C Intel FPGA IP and ADC Configurations

The JESD204C Intel FPGA IP parameters (L, M, and F) in this hardware checkout are natively supported by the AD9081 device configuration registers. The transceiver data rate, sampling clock frequency, and other JESD204C parameters comply with the AD9081 operating conditions.

The hardware checkout testing implements the JESD204C Intel FPGA IP with the following parameter configurations.

Global setting for below configuration:

- E = 1
- CF = 0
- FCLK_MULP = 2
- WIDTH_MULP = 4
- Subclass = 0
- SH_CONFIG = CRC-12
- FPGA Management Clock (MHz) = 100

Table 4. Parameter Configuration

Mode	LMF	N/N'	S	E	Decimation Mode	ADC Rate (Msps)	Data Rate (Msps) (8)	Lane Rate (Mbps) (9)	FPGA Device Clock (MHz)(10)	FPGA Link Clock (MHz) (11)	FPGA Frame Clock (MHz) (11)	Data Pattern
1	882	16	1	1	2x1	3000	1500	24750	375	187.5	375	Ramp

1.3.3. ADC Test Results

The following table contains the possible results and their definition.

(5) S is the number of transmitted samples per converter per frame.

(6) WIDTH_MULP is the data width multiplier between the application and transport layers.

(7) N is the number of conversion bits per converter.

(8) Data rate = ADC rate x decimation factor.

(9) Lane rate = (M/L) x N' x (66/64) x data rate.

(10) The FPGA device clock is used to clock the core PLL and the transceiver.

(11) The link clock and the frame clock are derived from the device clock using the core PLL.

Table 5. Results Definition

Result	Definition
PASS	The device under test (DUT) was observed to exhibit conformant behavior.
PASS with comments	The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included (example: due to time limitations, only a portion of the testing was performed).
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Refer to comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases SHA.1, SHA.2, EMBA.1, EMBA.2, EMBA.3, and RXTL.1 with subclass 0, and FCLK_MULP = 2.

Table 6. Result for Test Cases SHA.1, SHA.2, EMBA.1, EMBA.2, EMBA.3, and RXTL.1

Test No.	L	M	F	E	Lane Rate (Mbps)	ADC Rate (Msps)	Link Clock (MHz)	Result
1	8	8	2	1	24750	3000	187.5	PASS

The following figure shows the Signal Tap waveform of the ramp pattern data received at output of FPGA receiver transport layer.

Figure 4. Ramp Data Pattern Diagram

The following figure shows the result of the ramp pattern checker at output data of FPGA receiver transport layer.

Figure 5. Ramp Pattern Checker Result

1.3.4. ADC Test Result Comment

In receiver test case, the JESD204C receiver IP core successfully locked at sync header alignment phase and EMB alignment phase, no data integrity issue is observed by the ramp checker.

1.4. JESD204C Intel FPGA IP and DAC Hardware Checkout

1.4.1. DAC Hardware Checkout Methodology

This section describes the test objectives, procedures, and passing criteria. The test covers the following areas:

- Transmitter data link layer
- Transmitter transport layer

1.4.1.1. Transmitter Data Link Layer

This test area covers the test cases for `tx_rst_n`. The JESD204C TX IP will start link operation after `tx_rst_n` is deasserted. In a typical user application, all run-time registers should be configured when the Avalon memory-mapped configuration space is out of reset, and before the `txlink_clk` and `txframe_clk` are out of reset.

1.4.1.1.1. TX_RST

Table 7. TXRST Test Case

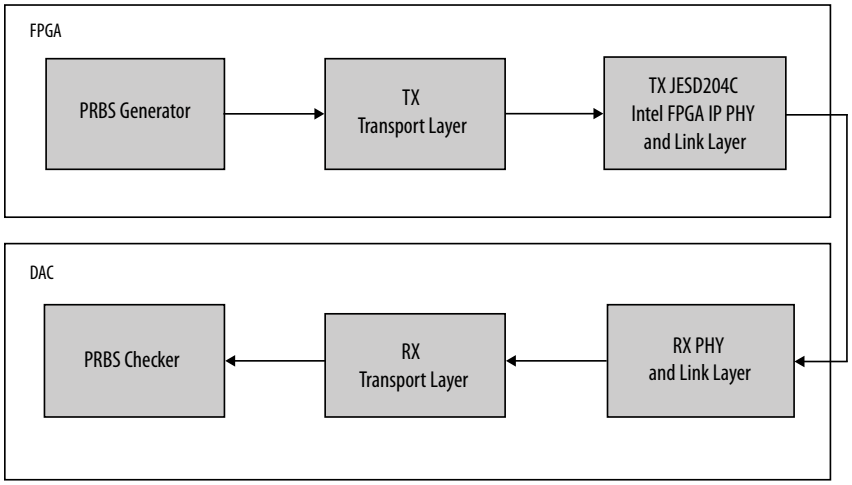
Test Case	Objective	Description	Passing Criteria
TXRST.1	Check if `j204c_tx_rst_n` is deasserted after the completion of reset sequence.	The following signals in *<ip_variant_name>*`_base.v` are tapped: • `j204c_tx_rst_n` • `j204c_tx_int` The `txlink_clk` is used as the sampling clock for the Signal Tap.	• The `j204c_tx_rst_n` is deasserted after power on. • The `j204c_tx_int` signal should stay low if there is no error. • AD9081 0x55E[6:4] status register returns 0x6 (Lock State) when the register is read.

1.4.1.2. Transmitter Transport Layer

To verify the data integrity of the data stream through the transmitter (TX) JESD204C Intel FPGA IP and transport layer, the DAC JESD core is configured to check the PRBS test pattern that is transmitted from the test pattern generator of the FPGA. PRBS pattern checker is used to check the data integrity of DAC transport layer.

This figure shows the conceptual test setup for data integrity checking.

Figure 6. Data Integrity Check Using PRBS Pattern Checker



The Signal Tap logic analyzer monitors the operation of the TX transport layer.

Table 8. TX Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
TXTL.1	Check the transport layer mapping of the data channel using PRBS test pattern.	The following signals in <*ip_variant_name*>_base.v are tapped: • j204c_tx_avst_valid • j204c_tx_avst_ready • j204c_tx_avst_data [(M*S*WIDTH_MULP*N)-1:0] The txframe_clk is used as the sampling clock for the Signal Tap. Check the following in the DAC: • PRBS test status	• The j204c_tx_avst_valid and j204c_tx_avst_ready signals are asserted. • The PRBS test status in DAC register 0x2064 and 0x2065 does not show an error.

1.4.2. JESD204C Intel FPGA IP and DAC Configurations

The JESD204C Intel FPGA IP parameters (L, M, and F) in this hardware checkout are natively supported by the AD9081 device configuration registers. The transceiver data rate, sampling clock frequency, and other JESD204C parameters comply with the AD9081 operating conditions.

The hardware checkout testing implements the JESD204C Intel FPGA IP with the following parameter configurations.

Global setting for below configuration:

- E = 1
- CF = 0
- FCLK_MULP = 2
- WIDTH_MULP = 4

- Subclass = 0
- SH_CONFIG = CRC-12
- FPGA Management Clock (MHz) = 100

Table 9. Parameter Configuration

Mode	LMF	N/N'	S	E	Interpolation Mode	DAC Rate (Msps)	Data Rate (Msps) (12)	Lane Rate (Mbps) (13)	FPGA Device Clock (MHz) (14)	FPGA Link Clock (MHz) (15)	FPGA Frame Clock (MHz)	Data Pattern
1	882	16	1	1	2x1	1939.39394	969.69697	16000	242.424242	121.212121	242.424242	PRBS23

1.4.3. DAC Test Results

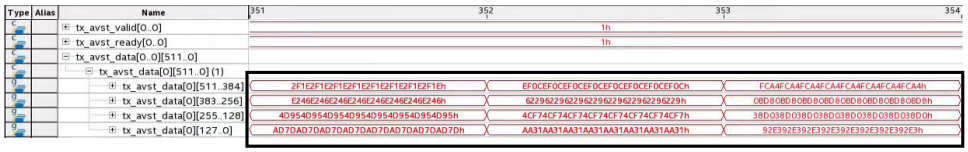
The following table shows the results for test cases TXRST.1 and TXTL.1 with subclass 0 and FCLK_MULP = 2.

Table 10. Result for Test Cases TXRST.1 and TXTL.1

Test No.	L	M	F	E	Lane Rate (Mbps)	DAC Rate (Msps)	Link Clock (MHz)	Result
1	8	8	2	1	16000	1939.39394	121.212121	PASS

The following figure shows the Signal Tap waveform of the PRBS pattern data transmitted to FPGA transmitter transport layer.

Figure 7. PRBS Data Pattern Diagram



The following figure shows the result of the pattern checker at output data of DAC transport layer.

(12) Data rate = DAC rate x interpolation factor.

(13) Lane rate = (M/L) x N' x (66/64) x data rate.

(14) The FPGA device clock is used to clock the core PLL and the transceiver.

(15) The link clock and frame clock are derived from the device clock using the core PLL.

Figure 8. DAC PRBS Checker Result

1.4.4. DAC Test Result Comment

In transmitter test case, the JESD204C transmitter IP successfully sends PRBS data through the transport, link and physical layers. The value of register `0x55E[6:4]` is 6, which means JESD204C link in DAC is locked, and no data integrity issue is observed by the DAC PRBS checker.

1.5. Document Revision History for AN 916: JESD204C Intel FPGA IP and ADI AD9081/AD9082 MxFE* Interoperability Report for Intel Stratix 10 E-Tile Devices

Document Version	Changes
2020.06.22	Initial release.

1.6. Appendix

Device Used and Quartus Tool Version

The Intel Stratix 10 1ST280EY2F55E1VG device (transceiver speed grade -1 device) is used.

Intel Quartus® Prime Pro Edition software version 19.3.0 Build 219 is used for compilation of designs.

Supported Device Data rate

The MxFE version of the DAC provided was specified to a maximum data rate of 16 Gbps while ADC was 24.75 Gbps.

Summary

This report shows validation of the Intel FPGA JESD204C IP core and PHY electrical interface with the AD9081 or AD9082 devices up to 16 Gbps for DAC and 24.75 Gbps for ADC. The complete configuration and hardware setup are shown to provide confidence in interoperability and performance of the two devices.