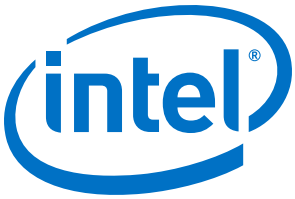


AN 910: Intel Agilex Power Distribution Network Design Guidelines

AN-910 | 2020.12.18
Latest document on the web: PDF | HTML

Contents

1. Intel® Agilex™ Power Distribution Network Design Guidelines Overview

This application note provides information for the Intel® Agilex™ device family power distribution network (PDN) design guidelines. A solid design guidelines for the Intel Agilex device family PDN including fixed decoupling caps on board and minimum simulation is proposed.

In the previous FPGA families (for example, the Intel Stratix® 10 and Intel Arria® 10 devices), the PDN tool was used along with power consumption data from the Early Power Estimator (EPE) and the pin connection guidelines to design and optimize board-level PDN. However, due to achieving non-feasible PDN design tool (decoupling caps) specifically for core, and with pessimistic results, the PDN tool is not used and supported for the Intel Agilex device family.

2. Power Sequencing Guidelines

This section describes the recommended power sequencing guidelines of the Intel Agilex device family.

2.1. Power Rail Sequence Grouping in Power-Up Sequence (PUS)

In order to simplify the power sequencing of the FPGA, the voltage rails are divided into 3 groups as shown in the Table 1 on page 4. The voltage rails of the lowest group comes up first in the PUS and go down last in the power-down sequence (PDS). Voltage rails in Group 1 comes up first, followed by Group 2, and then Group 3 in the PUS. Voltage rails in Group 3 comes down first, followed by Group 2, and then Group 1 in the PDS. All the voltage rails within each group are enabled and disabled at the same time.

Table 1 on page 4 shows the Intel Agilex device family power rail grouping and the required PUS covering for both ES and production devices.

Table 1. Intel Agilex Device Power Rail Grouping for the PUS Purpose

Power Group	FPGA Core and Hard Processor System (HPS)	Additional Voltage Rails			
		E-Tile	P-Tile	F-Tile	R-Tile
Group 1	V_{CC} V_{CCP} V_{CCH} V_{CCL_SDM} V_{CCH_SDM} $V_{CCPLLDIG\_SDM}$ V_{CCL_HPS} $V_{CCPLLDIG\_HPS}$	V_{CCRT_GXE} $V_{CC\_HSSI\_GXE}$ $V_{CCRTPLL\_GXE}$	$V_{CC\_HSSI\_GXP}$ V_{CCRT_GXP} V_{CCFUSE_GXP}	$V_{CC\_HSSI\_GXF}$ $V_{CCFUSECORE\_GXF}$ $V_{CCERT\_UX\_GXF}$ $V_{CCERT1\_BRK\_GXF}$ $V_{CCERT2\_BRK\_GXF}$	$V_{CC\_HSSI\_GXR}$ $V_{CCE\_PLL\_REF\_GXR}$ V_{CCERT_GXR}
Group 2	V_{CCPT} V_{CCPLL_SDM} V_{CCADC} V_{CCPLL_HPS} V_{CCA_PLL} (1)	V_{CCH_GXE} V_{CCCLK_GXE}	V_{CCH_GXP} V_{CCCLK_GXP}	$V_{CCFUSEWR\_GXF}$ V_{CCCLK_GXF} $V_{CCH\_UX\_GXF}$ $V_{CCEHT\_BRK\_GXF}$	V_{CCED_GXR} V_{CCCLK_GXR} $V_{CCH\_FUSE\_GXR}$ V_{CCEHT_GXR}
Group 3	V_{CCA_PLL} (2) V_{CCR_CORE} $V_{CCIO\_PIO\_SDM}$ V_{CCBAT} V_{CCIO_PIO} $V_{CCFUSEWR\_SDM}$	—	—	—	—

continued...

(1) For AGF014 2486A Early Silicon.

(2) For AGF014 2486A production silicon.

Power Group	FPGA Core and Hard Processor System (HPS)	Additional Voltage Rails			
		E-Tile	P-Tile	F-Tile	R-Tile
	V_{CCIO_SDM} V_{CCIO_HPS}				

The following lists the summary of the Intel Agilex device family required PUS:

- PUS is a requirement, not a recommendation
- PUS must be a controlled event (Group 1 > Group 2 > Group 3)
- HBM PUS and PDS is defined by the JEDEC specification
- VCCBAT_SDM can be powered up at any time
- Configuration via Protocol (CvP) or autonomous hard IPs (HIPs) must be within 10 ms from the first power supply ramp up to the last power supply ramp up
- All voltage rails must ramp up monotonically
- All voltage rails must ramp up to the full t_{RAMP} specification (as stated in the device data sheet)
- Do not drive I/O pins during a PUS

For more information, refer to the *Power-Up Sequence Requirements* section in the Intel Agilex Power Management User Guide.

2.2. Power-Down Sequencing (PDS)

Power-down sequencing (PDS) is the reverse of power-up sequencing (PUS). Power down has two cases—controlled power down (you do intend to perform power down, reset, or shutdown on the PCB) and uncontrolled power down (you do not intend to power down the PCB but because of malfunction or system failure, this happens).

PDS is always required and recommended in normal operation and controlled power down for the Intel Agilex device family. To perform the PDS in an controlled power-down event, you must follow the reverse for PUS. For more information, refer to the Intel Agilex Device Family Pin Connection Guidelines.

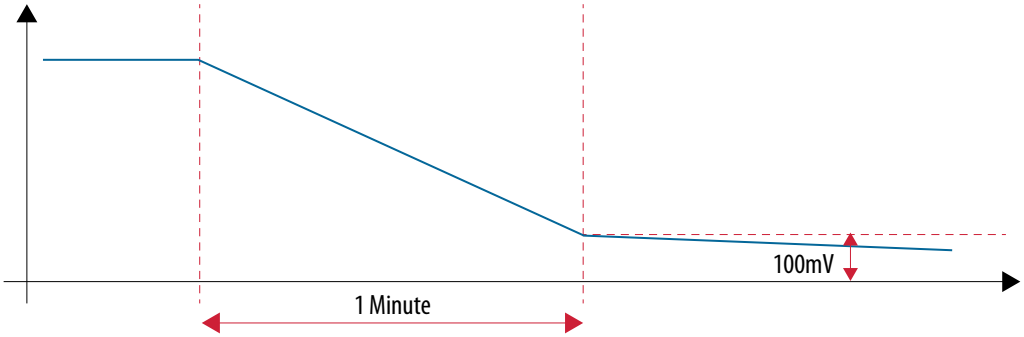
Intel Agilex device family has no uncontrolled PDS requirement for the core or fabric.

No uncontrolled PDS is required for the E-tile power rails if they are connected to VCCH with recommended filtering as shown in Figure 1 on page 8 and Figure 2 on page 9. The values of the inductors and capacitors in the filtering topology are chosen to provide the appropriate bandwidth to filter high frequency noise and isolate the IP from the external noise. If the E-tile power rails are separated and not connected to VCCH, PDS is required in an uncontrolled power-down event. PDS is required for H-tile (Intel Agilex AGF014 1785A device) in an uncontrolled power-down event. For more information on the recommended power-down circuitry for both E-tile and H-tile in an uncontrolled power-down event, refer to AN 692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria 10, Intel Stratix 10, and Intel Agilex Devices.

P-tile and R-tile are free of PDS in an uncontrolled power-down event.

The following lists the summary of the Intel Agilex recommended PDS:

- PDS is required for a controlled power-down event. Follow the reverse of the PUS procedure.
- PDS is not required but recommended for an uncontrolled power-down event unless it is stated.
  - Both E-tile and H-tile require PDS for an uncontrolled power-down event.
- All voltage rails must be <100 mV within 1 minute (this applies to a power loss condition as well).
- If the above condition (<100 mV within 1 minute) is met, then the device reliability is guaranteed, and there will be no device damage or performance degradation.



- Partial power down is not permitted.

3. Power Delivery Overview

This section covers the maximum power consumption budget specifically for the Intel Agilex device family. It also covers the recommended power tree or merged power rails on board to achieve minimum number of voltage regulators on board and reduce cost. The power rail names at the package-level along with their on-board (package pin) specification, rail tolerance, and the recommended step loads for the PDN time domain simulations are also covered in this section.

3.1. Power Architecture

3.1.1. Power Budget

Intel recommends you to use the Power Thermal Calculator (PTC) to determine the power for your applications. You must scale the recommended decoupling caps based on the scaling factor of the exact power consumption to the maximum power consumption.

Ensure that the recommended voltage regulator current in the board design must be larger than the total current for the merged power rails.

3.1.2. Power Tree

This section describes the recommended power tree for the Intel Agilex device family.

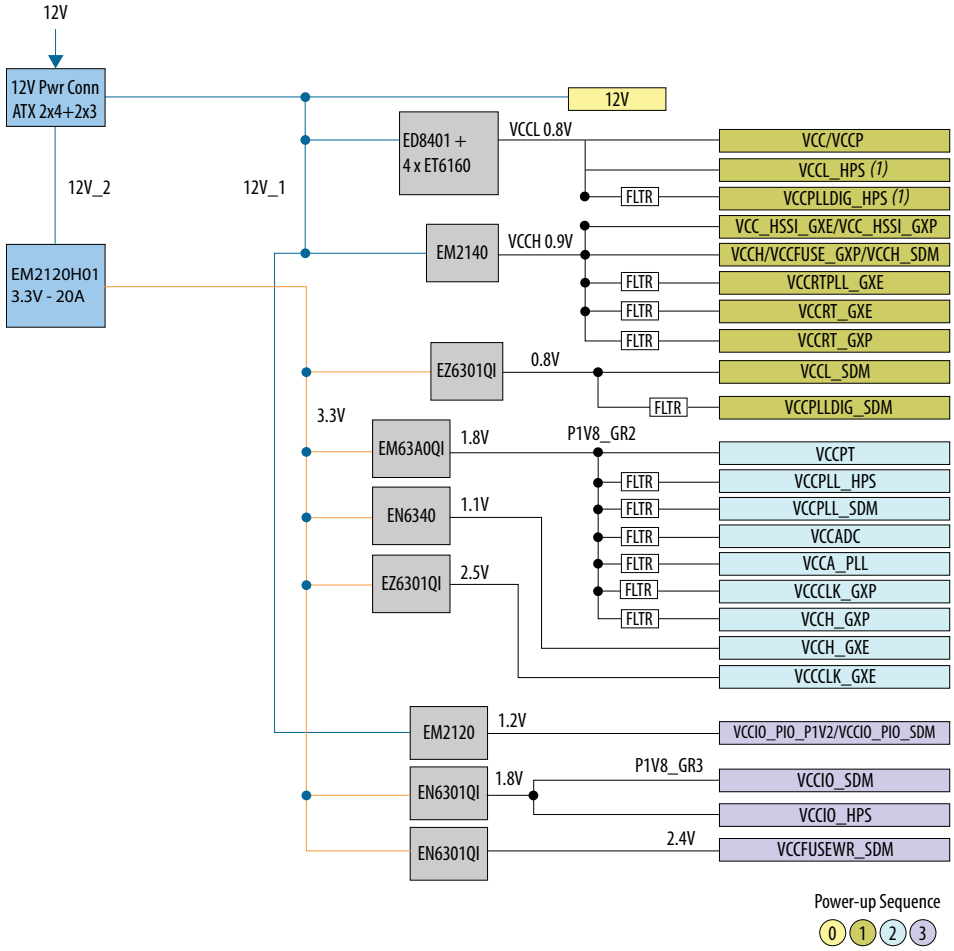
3.1.2.1. Recommended Power Tree for the Intel Agilex F-Series (2486A, 2581A: P-Tile and E Tile) Device Packages

The connection diagram in Figure 1 on page 8 and Figure 2 on page 9 show both recommended connections and required connections of the power rails on board. Required connections are mandatory for functionality. Not adhering to the required connection might produce unpredictable behavior. The recommended merged power rails and connections are aimed to reduce and optimize cost, area, and power in the platform design.

Figure 1 on page 8 and Figure 2 on page 9 show the recommended rail merger implemented in system with VCCIO of 1.2V. If a system is designed for VCCIO at 1.5V, a separate voltage regulator with a 1.5V output voltage within the same group must be assigned and designed for those I/O banks.

Figure 1. Recommended F-Series 2486A Power Tree for Early Silicon

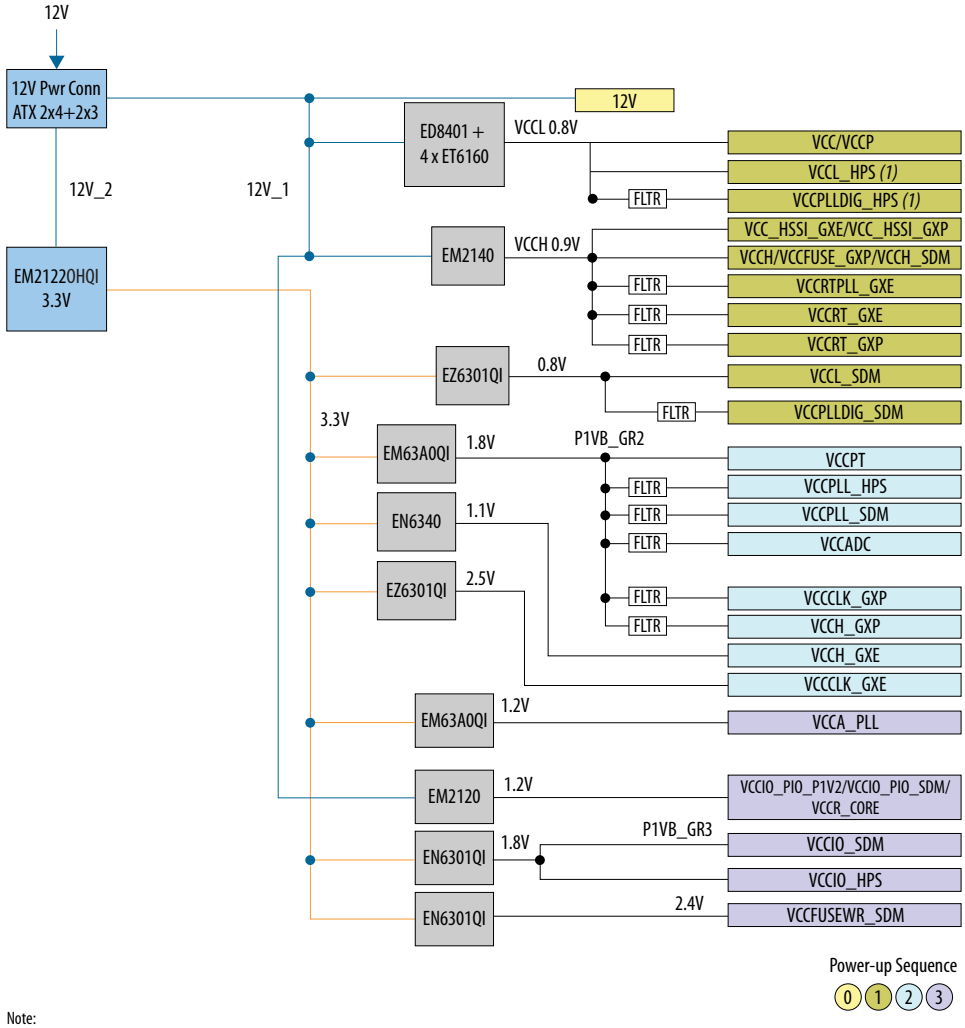
This power tree demonstrates the recommended FPGA PCB power rails grouping. You can use any recommended voltage regulators listed in FPGA Core Fabric VCCL Voltage Regulator Selection on page 21 as long as they meet the power rail specifications listed in Table 6 on page 13.



Note:
(1) VCCPLLDIG_HPS is always connected to VCCL_HPS via a filter in the power tree no matter of the device speed.
VCCL_HPS and VCCPLLDIG_HPS are always in Group 1 for power sequence no matter of the device speed.
•For -1 device speed: VCCL_HPS can be selected as either 0.9V or 0.95V for the turbo-mode performance. If 0.9V is selected for the turbo mode, VCCL_HPS and VCCPLLDIG_HPS are moved to VCCH 0.9V group rail in the power tree. If 0.95V is selected for the turbo mode, VCCL_HPS and VCCPLLDIG_HPS are fed separately by an additional voltage regulator=0.95V in Group 1.
•For -2 or -3 device speed: the power tree is as shown in this figure (VCCL_HPS and VCCPLLDIG_HPS are connected to VCCL 0.8V group rail).
•For -4 device speed: VCCL_HPS and VCCPLLDIG_HPS are connected to 0.8V group rail along with VCCL_SDM (0.8V) and VCCPLLDIG_SDM.
For more information, refer to the Intel Agilex Device Data Sheet.

Figure 2. Recommended F-Series 2486A and 2581A Power Tree for Production Silicon

This power tree demonstrates the recommended FPGA PCB power rails grouping. You can use any recommended voltage regulators listed in FPGA Core Fabric VCCL Voltage Regulator Selection on page 21 as long as they meet the power rail specifications listed in Table 6 on page 13.



Note:
(1) VCCPLLDIG_HPS is always connected to VCCL_HPS via a filter in the power tree no matter of the device speed.
VCCL_HPS and VCCPLLDIG_HPS are always in Group 1 for power sequence no matter of the device speed.
•For -1 device speed: VCCL_HPS can be selected as either 0.9V or 0.95V for the turbo-mode performance. If 0.9V is selected for the turbo mode, VCCL_HPS and VCCPLLDIG_HPS are moved to VCCH 0.9V group rail in the power tree. If 0.95V is selected for the turbo mode, VCCL_HPS and VCCPLLDIG_HPS are fed separately by an additional voltage regulator=0.95V in Group 1.
•For -2 or -3 device speed: the power tree is as shown in this figure (VCCL_HPS and VCCPLLDIG_HPS are connected to VCCL 0.8V group rail).
•For -4 device speed: VCCL_HPS and VCCPLLDIG_HPS are connected to 0.8V group rail along with VCCL_SDM (0.8V) and VCCPLLDIG_SDM.
For more information, refer to the *Intel Agilex Device Data Sheet*.

VREF_ADC

VREF_ADC (not mentioned in the power tree above) is treated as differential signal since it is input to the I/O buffer of ADC at FPGA. The in and out signals into FPGA is called VREF_ADCp and VREF_ADCn. The actual voltage of differential signal VREF_ADC is 1.25V. This voltage 1.25V comes from 1.8V in Group 2 with the use of a diode to convert 1.8V to 1.25V. This applies to both ES and production silicons. There is no

restriction on VREF_ADC voltage level in the Intel Agilex device family compared to the Intel Stratix 10 device family that states VREF_ADC to be equal or lower voltage than VCCA_PLL.

VCCPT and VCCR_CORE: Differences between Intel Agilex AGF014 2486A ES and Production Silicons

To reduce power, there has been an effort to change the rail powering CRAM from 1.8V to 1.2V. Early silicon has 1.8V supply for VCCPT (VCCPT covers VCCR_CORE in package). However, in production silicon, this will change to separate VCCPT and VCCR_CORE power rails in package, with 1.2V power supply assigned for VCCR_CORE and 1.8V power supply assigned for VCCPT. There will also be a production package which is pin compatible to ES package and contains additional 1.2V balls to account for the additional supply. To avoid impact to boards which are already in PCB design phase, the ES package ballout already contains balls with VCCR_CORE of 1.2V in the Intel Agilex AGF014 ES packages. Therefore, ES to production silicon change should be transparent to board designers. Decap table provided decaps separately for 1.2V VCCR_CORE supply. In production silicon, VCC_CORE is pin-out at package separately from VCCPT. However, in early silicon, both VCC_CORE and VCCPT power nets are combined at package and pin-out at package as VCCPT pins.

VCCA_PLL: Difference between Intel Agilex AGF014 2486A ES and Production Silicons

The power tree in Figure 1 on page 8 stands for early silicon design where VCCA_PLL is 1.8V. For production silicon design, VCCA_PLL will drop to 1.2V (for lower power consumption), and a separate voltage regulator is required for VCCA_PLL on board to support this power rail individually. This VCCA_PLL power rail which is in Group 2 cannot be merged with 1.2V power rail in Group 3 due to different voltage specification and tolerance at silicon.

Power Tree Updates for Intel Agilex AGF014 2486A Production Silicon

To address the power rail changes in the production silicon, the power tree in Figure 1 on page 8 will slightly change compared to the power tree in Figure 2 on page 9. The changes are summarized below:

- Separate VCCR_CORE from VCCPT.
- Merge VCCR_CORE with VCCIO 1.2V power rail in Group 3 (VCCIO_PIO_P1V2).
- Disconnect VCCA_PLL power rails from 1.8V power net in Group 2. The maximum supported current by voltage regulator for the updated power net 1.8V in Group 2 changes to 5A.
- Add a new voltage regulator (maximum current 6A) into power tree in Group 2 to cover a 1.2V power net in Group 2. This new 1.2V power net in Group 2 is connected to VCCA_PLL (maximum current 5.68A).
- VCCA_PLL shall be merged with VCCIO_1P2V power rail in Group 3, but an LC filter is added to isolate this power net from other power nets connected to the same rail. If you merge VCCA_PLL to VCCIO_1P2V in Group 3, the voltage noise tolerance for this VCCIO_1P2V power rail in Group 3 would change from ±5% to ±3% in Table 6 on page 13.

3.2. Rail Merger Requirements

IP voltage rails of same nominal values within the same sequencing group can be merged assuming that the power delivery network to each package balls for each IP is designed with care to meet the tolerance specifications of that IP. Therefore, proper analysis and/or simulations should be done to ensure voltage drop and cross regulations are under control.

Other connections not mentioned in the Table 2 on page 11 are recommended (not mandatory to follow) to optimize design cost and size.

Table 2. Required Rail Connections

	Rail 1	Rail 2	Notes
1	VCCH	VCC_HSSI_GXE	Connect directly. Filter is optional.
2	VCCH	VCCRT_GXE	Required to eliminate the need of PDS pull-down circuits. Connect via an LC filter. Use an inductor instead of ferrite bead to reduce voltage drop.
3	VCCH	VCCRTPLL_GXE	Required to eliminate the PDS circuits. Connect via a ferrite bead LC filter.
4	VCCH	VCC_HSSI_GXP	Connect directly. Filter is optional.
5	VCCH	VCCRT_GXP	VCC_HSSI_GXP and VCCRT_GXP should be connected to the same voltage regulator. Connect via an LC filter.

As many power rails are merged on the motherboard, the requirement for an LC filter is necessary to ensure systems functionality especially for rail connections to sensitive circuits such as the phase-locked loop (PLL) and clock. Intel recommends you to follow the LC filter requirements.

VCCH_AIB for the E-tile and P-tile are not connected on package. You can separate them if they stay in the same power sequence group. However, VCCH_SDM should be connected to both to provide proper functionality.

3.3. Power Rails Specification

3.3.1. Power Nets

This section describes the Intel Agilex device family power nets and their subsystem details along with their board-level connection based on the recommended power trees described in the Power Tree on page 7.

3.3.1.1. Intel Agilex Package Power Nets and Subsystems Details

Table 3 on page 12 shows the Intel Agilex F-Series FPGA Core/Fabric power nets and their subsystem details based on the recommended power tree in Figure 1 on page 8 and Figure 2 on page 9.

Table 3. Intel Agilex F-Series 2486A and 2581A FPGA Package Power Rail Nets and Subsystem Details

System	Ball Rail Name	PTC Rail Name	Board Connections	System Connections
FPGA	VCCL	VCC	VCCL	Fabric core
FPGA/HPS	VCCL_HPS	VCCL_HPS		HPS core
FPGA/HPS	VCCPLLDIG_HPS	VCCPLLDIG_HPS		HPS digital PLL
FPGA/PIO	VCC	VCCP		I/O 96 PHY
FPGA	VCCH_AIB	VCCH	VCCH	Rail for AIB-G
FPGA/SDM	VCCH_SDM	VCCH_SDM		SDM POR monitoring ball for VCCH
FPGA/SDM	VCCL_SDM	VCCL_SDM	VCCL_SDM	SDM core
FPGA/SDM	VCCPLLDIG_SDM	VCCPLLDIG_SDM		SDM digital PLL
FPGA	VCCR	VCCPT	P1V8_GR2	CRAM
FPGA/PIO	VCCA	VCCA_PLL(3)		Main DDR PLL
FPGA/SDM	VCCADC_SDM	VCCADC		ADC
FPGA/SDM	VCCPLL_SDM	VCCPLL_SDM		SDM analog PLL
FPGA/HPS	VCCPLL_HPS	VCCPLL_HPS		HPS analog PLL
FPGA/SDM	VCCN_PIO_SDM	VCCIO_PIO_SDM	VCCIO_PIO_P1V2	SDM POR monitor for VCCN_PIO
FPGA/PIO	VCCN_PIO	VCCIO_PIO		I/O 96 I/O buffer
FPGA	VCCR_CORE	VCCR-CORE		Share with VCCIO only when I/O is DDR4/1.2V
FPGA/SDM	VCCN_SDM	VCCIO_SDM	P1V8_GR3	SDM 1.8V I/O supply
FPGA/HPS	VCCN_HPS	VCCIO_HPS		HPS I/O supply
FPGA/SDM	VCCFUSEWR_SDM	VCCFUSEWR_SDM	VCCFUSEWR_SDM	SDM fuse

Table 4. Intel Agilex E-Tile Power Rail Nets and Subsystem Details

Ball Rail Name	PTC Rail Name	Board Connections	System Connections
VCCERT_E-TILE	VCCRT_GXE	VCCH	E-Tile TX/RX transceiver analog
VCCERT_PLL_E-TILE	VCCRTPLL_GXE		E-Tile TX/RX transceiver analog
VCC_HSSI_E-TILE	VCC_HSSI_GXE		E-Tile TX/RX transceiver analog
VCCEHT_E-TILE	VCCH_GXE	VCCH_GXE	E-Tile TX/RX transceiver analog
VCCN2P5IO	VCCCLK_GXE	VCCCLK_GXE	E-Tile 2.5V I/O supply

(3) For early silicon. For production silicon, this power rail is 1.2V.

Table 5. Intel Agilex P-Tile Power Rail Nets and Subsystem Details

Ball Rail Name	PTC Rail Name	Board Connections	System Connections
VCC_HSSI_P-TILE	VCC_HSSI_GXP	VCCH	P-tile TX/RX transceiver digital
VCCFUSE_P-TILE	VCCFUSE_GXP		P-tile fuse
VCCERT_P-TILE	VCCRT_GXP		P-tile TX/RX transceiver analog
VCCEHT_P-TILE	VCCH_GXP	P1V8_GR2	P-tile TX/RX analog
VCCN1P8V_IO	VCCCLK_GXP		1.8 GPIO in P-tile

3.3.2. Power Rails Tolerance

This section describes the power rails tolerance and budget (AC + DC) on board for the Intel Agilex device family. The rail tolerance must be met at the FPGA package ball. You must consider the following instructions to measure the rail tolerance:

- VCCL (core power net) measurement is taken at the FPGA remote differential sense lines (there is assigned differential sense pins at FPGA package) with the scope set to bandwidth limited at 20MHz.
- Other power rails (except for VCCL (core power)), the rail tolerance must be met at the board vias on the bottom layer directly connected to the package power balls.
- For other rails, place the voltage regulator sense point (if it has) in the FPGA pin field (in the package shadow), as close as possible to the corresponding package power balls. For these rails, measure the output voltage at this remote sense location.

Table 6. Intel Agilex Device Rail Tolerance

	Vnom (Required)	DC Setpoint (Recommended)	VR Ripple (Recommended)	AC (Transient) (Recommended)	AC + DC (Required) (4)
VCCL (core)	VID (0.68, 0.8, 0.85)	0.5%	2.5%		±3%
VCCH	0.9	0.5%	2.5%		±3%
VCCL_SDM	0.8	0.5%	2.5%		±3%
VCCH_GXE	1.1	0.5%	0.5%	2%	±3%
VCCCLK_GXE	2.5	0.5%	0.5%	3.5%	±5%
P1V8_GR2	1.8	0.5%	0.5%	2%	3%
VCCIO_PIO_P1V2	1.2	0.5%	1%	3.5%	5%
P1V8_GR3	1.8	0.5%	1%	3.5%	5%
VCCFUSEWR_SDM	2.4	0.5%	1%	3.5%	5%

Table 6 on page 13 shows the power rail tolerance (AC + DC) based on the recommended power grouping in Table 1 on page 4 and power tree in Figure 1 on page 8 and Figure 2 on page 9.

(4) The specification stands for DC + AC rail tolerance and must be measured and met at package pin/ball.

If a different power tree in Figure 1 on page 8 and Figure 2 on page 9 is used, the rail tolerance of each power net must fall into their recommended grouping category in Table 6 on page 13.

3.3.3. Power Nets and Transient Specifications

Rail transient provided in the Table 7 on page 14 is used to design and simulate the board level. Choose the recommended load slew rates and step load at FPGA package ball below for PCB-level PDN system simulations and design. Table 7 on page 14 shows the maximum tolerable step load at FPGA package pin. The recommended step load in Table 7 on page 14 is connected to FPGA package ball along with the PCB post-layout model (with decoupling caps and voltage regulator model excluding package and silicon/die model) in an EDA tool for time domain simulation to meet rail tolerance of respective power net in Table 6 on page 13 at FPGA package ball.

Table 7 on page 14 shows for the recommended step load at package ball and step load's slew rate.

Table 7. Intel Agilex Device Family Transient and Step Load Specifications at Package Pin

	At Package Balls (Step Load)	DI/dt at Package Balls (for Board Design)-Slew Rate	Notes
	DI (A)-Step Load	DI/dt (A/µs)-Slew Rate	
VCCL	17	200	This is the most stringent based on simulation models.
VCC	1.56	6.8	Current at ball is per side (4 I/O banks together).
VCCR	2.4	12	PDN should meet both specifications.
VCCN	0.645	10.8	Current specification is per I/O bank. Each I/O bank consists of 96 x I/Os. More I/O banks can join the same voltage regulator but current specification stays per I/O bank.
VCCH_AIB	1.12	4.8	Current at ball is per AIB.
VCCERT_GXE	2	20	Per E-tile.
VCC_HSSI_GXP	1.6	20	Current step load is per VCC_HSSI_GXP supply.
VCCERT_GXP	2.02	13.5	Slowest step load but largest current amplitude.
	0.5	10	Fastest step load but slowest current amplitude.

3.4. Decoupling Caps Recommendation

Solid and recommended FPGA decoupling caps requirement on board-level PCB are listed in this section in the table format for all power nets and based on the maximum FPGA power consumption and the recommended power trees. The table does not include recommended decoupling/bulk caps at voltage regulators. You must select the

voltage regulator bulk caps (decoupling caps) from the voltage regulator data sheet based on maximum voltage regulator ripple specification and maximum current (DC +AC) support for the specific power rail (or combined power rails).

You must follow the recommended decoupling caps along with the power rail grouping and recommended voltage regulator on PCB to ensure meeting the power tail tolerance and specification at package ball. For boards/PCBs that consume less power than maximum power consumption, you must scale the decoupling caps by ratio of board power consumption to maximum power consumption per power rail. However, transient PDN simulation must be performed to ensure meeting the power rail tolerance at package ball.

3.4.1. Intel Agilex F-Series 2486A and 2581A FPGA Packages Board-Level Decoupling Caps Summary

Table 8 on page 15 shows PCB recommended FPGA decoupling caps requirement for the Intel Agilex F-Series 2486A and 2581A device packages.

Table 8. Intel Agilex F-Series 2486A and 2581A FPGA Decoupling Caps Summary

System	Ball Rail Name	Intel Agilex Power and Thermal Calculator (PTC) Rail Name	Bottom-side Caps		FPGA Periphery Caps(5)		Notes
			Thick PCB (>65 mil thickness)	Thin PCB (≤65 mil thickness)	Thick PCB (>65 mil thickness)	Thin PCB (≤65 mil thickness)	
FPGA	VCCL	VCC	9x 47uF 0805	5x 47uF 0805	6x 47uF 0805	3x 47uF 0805	Place thick 0805 (47uF) caps inside bottom-side cavity. Use 47uF 0805 periphery caps at top-layer near FPGA.
FPGA/PIO	VCC	VCCP					
FPGA/HPS	VCCPLLDIG_HPS	VCCPLLDIG_HPS	1x 1uF 0201	1x 1uF 0201	N/A	N/A	—
FPGA/HPS	VCCL_HPS	VCCL_HPS	2x 10uF 0402 or 3x 4.7uF 0201	2x 10uF 0402 or 3x 4.7uF 0201	1x 22uF 0603	1x 22uF 0603	For SoC-centric designs.
FPGA	VCCH_AIB	VCCH	4x 22uF 0603	4x 22uF 0603	2x 47uF 0805	2x 47uF 0805	Place thick 0603 (22uF) caps inside bottom-side cavity.
FPGA/SDM	VCCH_SDM	VCCH_SDM	1x 1uF 0201	1x 1uF 0201	Same as VCCH	Same as VCCH	—
FPGA/SDM	VCCL_SDM	VCCL_SDM	2x 1uF 0201	2x 1uF 0201	N/A	N/A	—
FPGA/SDM	VCCPLLDIG_SDM	VCCPLLDIG_SDM	1x 1uF 0201	1x 1uF 0201	LC filter caps	LC filter caps	—

continued...

(5) Periphery caps are optional and recommended only for systems where the voltage regulator is placed reasonably far from the FPGA package. Once placed, they should be part of the complete voltage regulator cap solution.

System	Ball Rail Name	Intel Agilex Power and Thermal Calculator (PTC) Rail Name	Bottom-side Caps		FPGA Periphery Caps[5]		Notes
			Thick PCB (>65 mil thickness)	Thin PCB (≤65 mil thickness)	Thick PCB (>65 mil thickness)	Thin PCB (≤65 mil thickness)	
FPGA	VCCR	VCCPT	2x 4.7uF 0201	2x 4.7uF 0201	1x 10uF 0402	1x 10uF 0402	—
FPGA	VCCR_CORE	VCCR_CORE	1x 1uF 0201	1x 1uF 0201	N/A	N/A	Intel Agilex AGF014 2486A production device.
FPGA/PIO	VCCA	VCCA_PLL	2x 10uF 0402	2x 10uF 0402	LC filter caps	LC filter caps	—
FPGA/SDM	VCCADC_SDM	VCCADC	1x 1uF 0201	1x 1uF 0201	LC filter caps	LC filter caps	—
FPGA/SDM	VCCPLL_SDM	VCCPLL_SDM	1x 1uF 0201	1x 1uF 0201	LC filter caps	LC filter caps	—
FPGA/HPS	VCCPLL_HPS	VCCPLL_HPS	1x 1uF 0201	1x 1uF 0201	LC filter caps	LC filter caps	—
FPGA/SDM	VCCN_PIO_SDM	VCCIO_PIO_SDM	N/A	N/A	N/A	N/A	—
FPGA/PIO	VCCN_PIO	VCCIO_PIO	2x 4.7uF 0402	2x 4.7uF 0402	1x 10uF 0402	1x 10uF 0402	Per channel
FPGA/SDM	VCCN_SDM	VCCIO_SDM	1x 1uF 0201	1x 1uF 0201	N/A	N/A	—
FPGA/HPS	VCCN_HPS	VCCIO_HPS	1x 1uF 0201	1x 1uF 0201	N/A	N/A	—
FPGA/SDM	VCCFUSEWR_SDM	VCCFUSEWR_SDM	1x 1uF 0201	1x 1uF 0201	N/A	N/A	—

3.4.2. Intel Agilex E-Tile Board-Level Decoupling Caps Summary

Table 9. Intel Agilex E-Tile Decoupling Caps Summary

Ball Rail Name	Intel Agilex PTC Rail Name	Bottom-side Caps		FPGA Periphery Caps		Notes
		Thick PCB (≥65 mil thickness)	Thin PCB (≤65 mil thickness)	Thick PCB (≥65 mil thickness)	Thin PCB (≤65 mil thickness)	
VCCERT_E-TILE	VCCRT_GXE	6x 4.7uF 0201	6x 4.7uF 0201	LC filter caps 2x 10uF 0402	LC filter caps 2x 10uF 0402	—
VCCERT_PLL_E-TILE	VCCRTPLL_GXE	2x 0201 1uF	2x 0201 1uF	LC filter caps	LC filter caps	—
VCC_HSSI_E-TILE	VCC_HSSI_GXE	3x 10uF 0402 or 10x 4.7uF 0201	3x 10uF 0402 or 10x 4.7uF 0201	N/A	N/A	—
VCCEHT_E-TILE	VCCH_GXE	2x 4.7uF 0201	2x 4.7uF 0201	2x 10uF 0402	2x 10uF 0402	—
VCCN2P5IO	VCCCLK_GXE	1x 1uF 0201	1x 1uF 0201	N/A	N/A	—

(5) Periphery caps are optional and recommended only for systems where the voltage regulator is placed reasonably far from the FPGA package. Once placed, they should be part of the complete voltage regulator cap solution.

3.4.3. Intel Agilex P-Tile Board-Level Decoupling Caps Summary

Table 10. Intel Agilex P-Tile Decoupling Caps Summary

Ball Rail Name	Intel Agilex PTC Rail Name	Bottom-side Caps		FPGA Periphery Caps		Notes
		Thick PCB (≥65 mil thickness)	Thin PCB (≤65 mil thickness)	Thick PCB (≥65 mil thickness)	Thin PCB (≤65 mil thickness)	
VCC_HSSI_P-TILE	VCC_HSSI_GXP	1x 10uF 0402	1x 10uF 0402	N/A	N/A	—
VCCFUSE_P-TILE	VCCFUSE_GXP	1x 1uF 0201	1x 1uF 0201	N/A	N/A	For multiple P-tile packages, use 1x 0402 4.7uF per 2 P-tile.
VCCERT_P-TILE	VCCRT_GXP	6x 4.7uF 0201	6x 4.7uF 0201	LC filter caps	LC filter caps	Can use 11x 1uF 0201.
VCCEHT_P-TILE	VCCH_GXP	1x 1uF 0201	1x 1uF 0201	LC filter caps	LC filter caps	—
VCCN1P8V_IO	VCCCLK_GXP	1x 1uF 0201	1x 1uF 0201	LC filter caps	LC filter caps	—

4. Board Power Delivery Network Recommendations

This section describes other recommended power delivery network designs including the voltage regulator selection and filtering circuitry for power rails that are fed by a common voltage regulator. The design example in this section shows the development kits designed in-house.

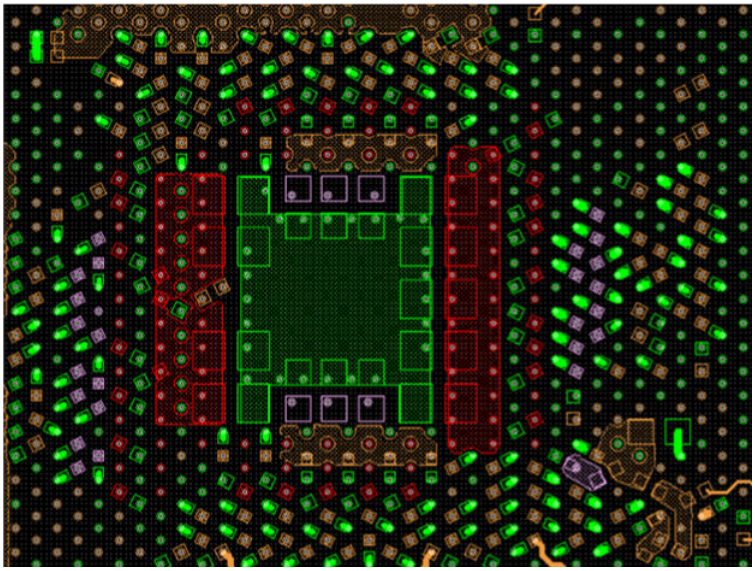
This section also describes board decoupling caps placement example on board.

4.1. Board Decoupling Caps Guide

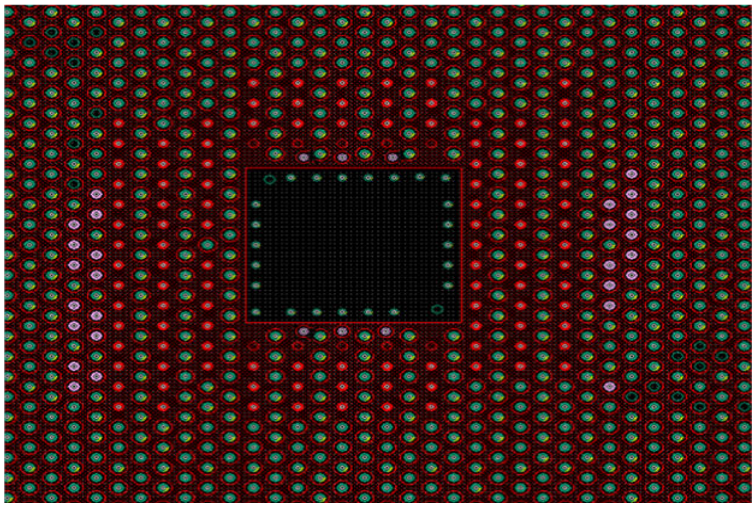
In addition to OPD (as LSC and DSC), the Intel Agilex device family also offers a cavity site or state to place back large size back side caps as close as possible to the die or package to improve transient regulation and reduce second or third voltage droop. A total of 15 decoupling caps (refer to Table 8 on page 15, the bottom side caps for VCC core and VCCH) can be added into the board cavity including 9x 0805 47uF (for VCC core) and 6x 0603 22uF (for VCCH) as shown in Figure 3 on page 19.

Figure 3 on page 19 is an example of decoupling caps scheme or connection within cavity on the top-layer for a PCB designed for the Intel Agilex FPGA without socket and the use of micro via. The top layer in Figure 3 on page 19 is assigned for VCC core power and the GND pins on top layer within the decap mounting are connected to the second layer (ground) through a micro via.

Figure 3. Back-side Board Cavity with Large Size Decaps for PCB without Socket, Thin Stackup, and the Use of Micro Via



(a) Bottom-side Decoupling Caps within Cavity Area

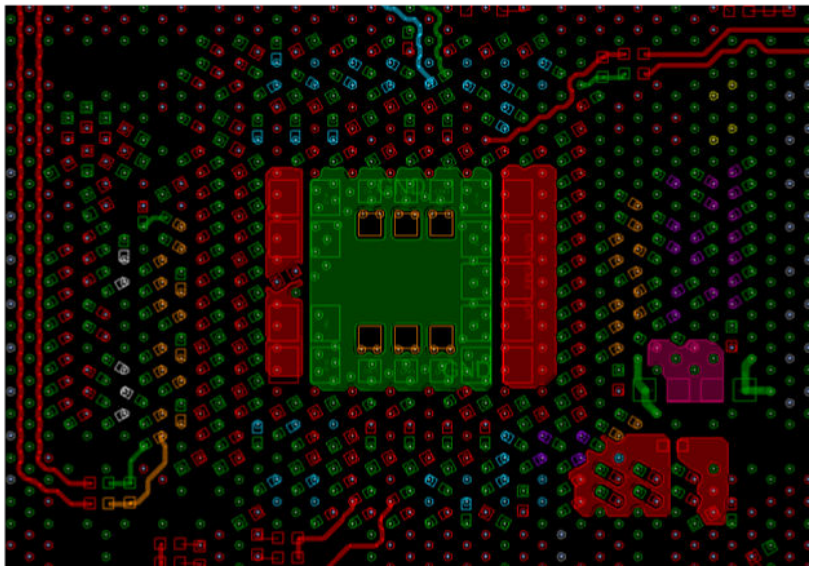


(b) Top-side of PCB within Cavity Area

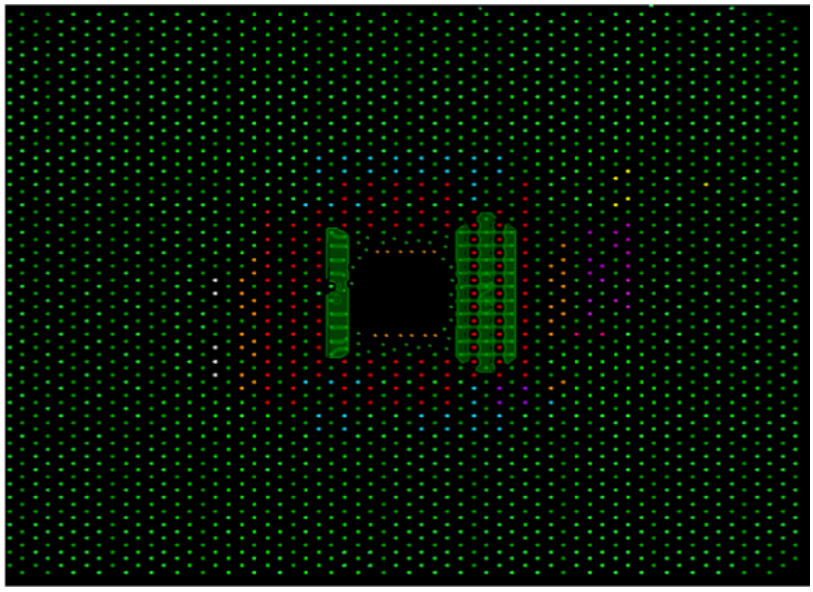
Because of the location of the cavity caps on the bottom side, several GND balls can't have vias in pad, for stackup without the use of micro via. To ensure that we do not reduce the package current capability, and that we have a low-return inductance path, add a ground island on the top layer connecting those floating balls to adjacent GND vias, as illustrated in Figure 4 on page 20.

Figure 4 on page 20 is an example of decoupling caps scheme or connection within the cavity on the top layer for a PCB designed of Intel Agilex F-Series 2486A and 2581A FPGA without socket and the use of only through via for GND pins.

Figure 4. Back-side Board Cavity with Large Size Decaps, Thick Stackup, and the Use of Through Via



(a) Bottom-side Decoupling Caps within Cavity area



(b) Top-side of PCB within Cavity area

In addition, other recommended 0201 and 0402 decoupling caps can be placed in the via field (FPGA pin field) on bottom layer inside the package shadow. The board side decaps (FPGA periphery) recommendation for all rails can be placed either on top layer or bottom layer close to the edge of FPGA device.

This is a summary of the recommended decaps placement within cavity for the Intel Agilex device family:

- VCCL cavity decaps on bottom side:
  - Thick PCB: 9x 0805 47µF
  - Thin PCB: 5x 0805 47µF
- VCCH cavity decaps on bottom side: 4x 0603 22µF
  - Option for VCCH: Some 0603 caps can be allocated to VCCL or VCCN/VCCR depending on power consumption.

  Note: The power tree and number of decoupling caps within the cavity on the Intel Agilex development kit boards may be slightly different than what has been recommended in this application note due to early release of silicon and guideline. The recommended power tree, guideline, and decoupling caps in this application note has been well established and validated by measurement for the final device production.

It is due to reliability to have the cavity area on top layer to be free of components due to OPD in package. However, pads or other coppers are allowed in this area on top layer. This means you can place as much caps if they fit into the cavity area on the bottom layer connecting caps to top layer through via.

4.2. FPGA Core Fabric VCCL Voltage Regulator Selection

Intel recommends you to use the industry standard common footprints for power stages. This provides you the flexibility to choose between six different vendors during the validation phases. This also allows you to choose the vendor that best fit your PCB performance and cost targets without impacting the program schedule. The vendors that offer power stages for core in the industry standard common footprints are:

- Intel Enpirion®
- MPS
- Infineon
- Fairchild
- TI
- Intersil
- ADI
- LTC

The following controllers have been validated for operation and communication with the Intel Agilex Power Management Controller Tool and added to the existing list of supported controllers and power stages.

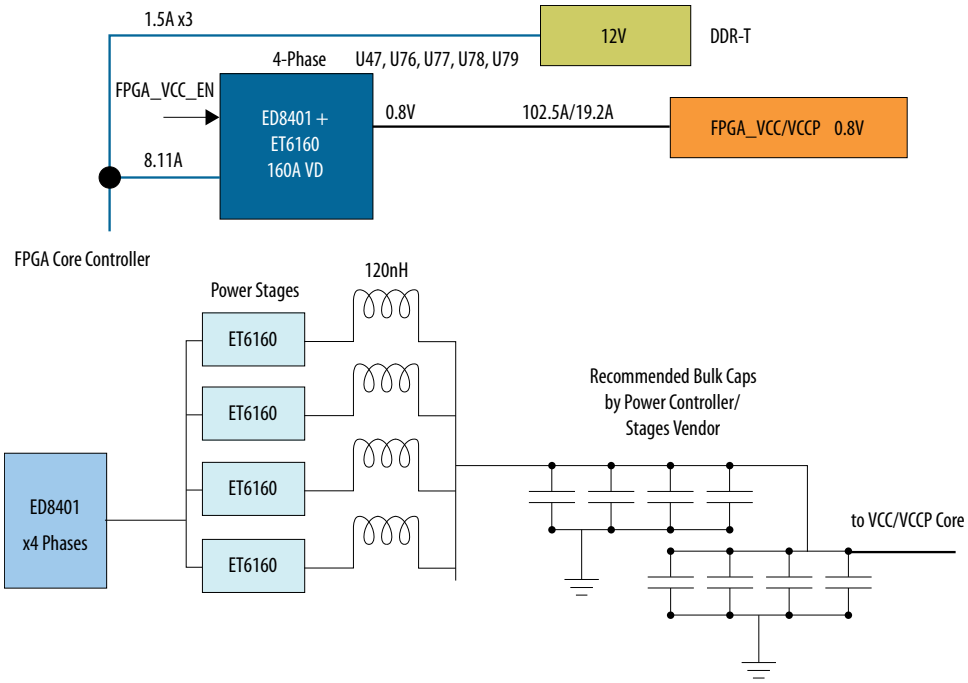
Table 11. List of Supported Controllers and Power Stages

Vendor	Controller	Power Stage	Number of Phase
Intel Enpirion/Intel	ED8401	ET6160 (60A)	4
MPS	MPS2975/2972	MP86956A (60A)	5
Intersil/Renesas	ISL68236	ISL99227 (60A)	5
ADI	LTC3888-1	LTC7051 (60A)	4

Validated VR controllers from the Intel Stratix 10 device are still supported too.

The following power tree is being tested on internal boards (development kits). Hence, Intel recommends you to follow this VCCL (core) voltage regulator diagram.

Figure 5. VCC/VCCP Core Voltage Regulator Design Implemented on the Intel Agilex AGF014 2486A FPGA Development Kits



4.3. Remote Sense Connections

Die sense pins are provided for the core fabric voltage regulator. The voltage regulator sense line for VCCL must be connected to the differential pair sense lines or pins provided on the package. The voltage regulator feedback inputs shall be connected to this FPGA die remote sense lines.

For all other voltage regulators related to other power rails or groups, the remote sense shall be placed inside the via or pin field under the die shadow as close as physically possible to the geometrical center of the corresponding power balls. Note that the voltage rail specification provided in Table 6 on page 13 are valid only when sensing at this remote sense location, for example, on the board back side, on the vias connected to the package power balls.

You are required to use sense lines for Intel Agilex core, including the VID and multi-voltage designs.

Note: If you uniformly distribute current in core, all package IR drop can be compensated (this package IR drop is about 13mV). However, if you distribute the current unevenly in core, only 50% of package IR drop can be compensated (about 6mV).

4.4. Load Line Requirements

Load line is optional for Intel Agilex AGF014 device family packages. The load line requirements will be updated for future Intel Agilex device family.

4.5. VCCL Core Board Current Slew Rate

The VCCL core fabric has a very high current slew rate. But some of that is filtered out by the metal-insulator-metal (MIM) caps as they provide the lowest impedance to the load because of their proximity. With addition of OPDs, most of the remaining fast edges are filtered out, leaving the board cavity caps and voltage regulator caps to handle only a fraction of the die level current.

You must ensure the PDN can deliver the current specified at the package balls. Board LC Recommended Filters for Noise Reduction in Combined Power Delivery Rails on page 24 describes the recommended PCB system-level simulation to ensure the voltage tolerance or specification at package balls are met through the design.

5. Board LC Recommended Filters for Noise Reduction in Combined Power Delivery Rails

5.1. P-Tile Rail LC Filter Board Scheme and Connection

The filtering topology in Figure 6 on page 24, Figure 7 on page 24, and Figure 8 on page 25 are recommended for the P-tile voltage rails (VCCCLK_GXP, VCCHT_GXP, VCCRT_GXP) in the Power Tree on page 7 for noise filtering purpose. The filter can be placed as close to FPGA as periphery caps in the recommended decoupling caps table in the Decoupling Caps Recommendation on page 14. In addition to the LC filter, you must also add the bottom or backside caps recommended in the decoupling caps table in the Decoupling Caps Recommendation on page 14 within pin or via field on the bottom layer.

Figure 6. Filter Recommendation for VCCCLK_GXP

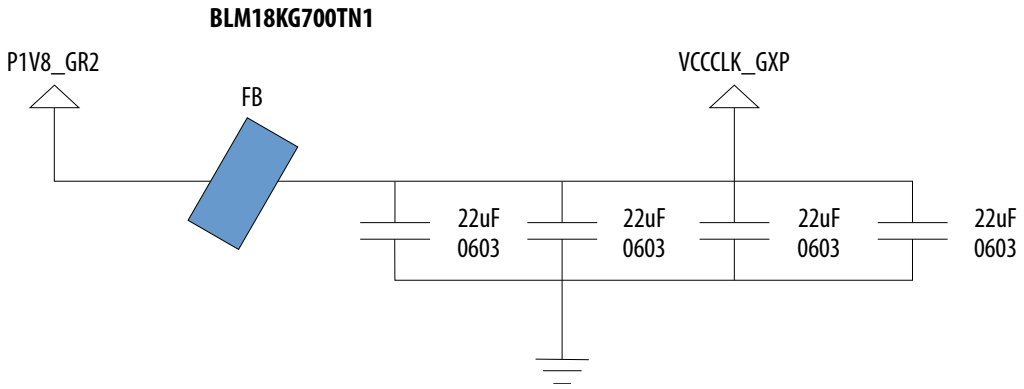


Figure 7. Filter Recommendation for VCCHT_GXP

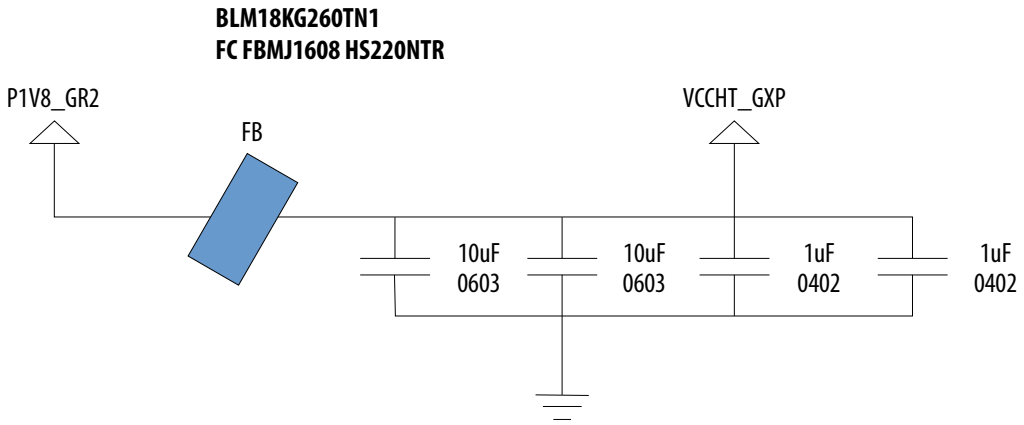
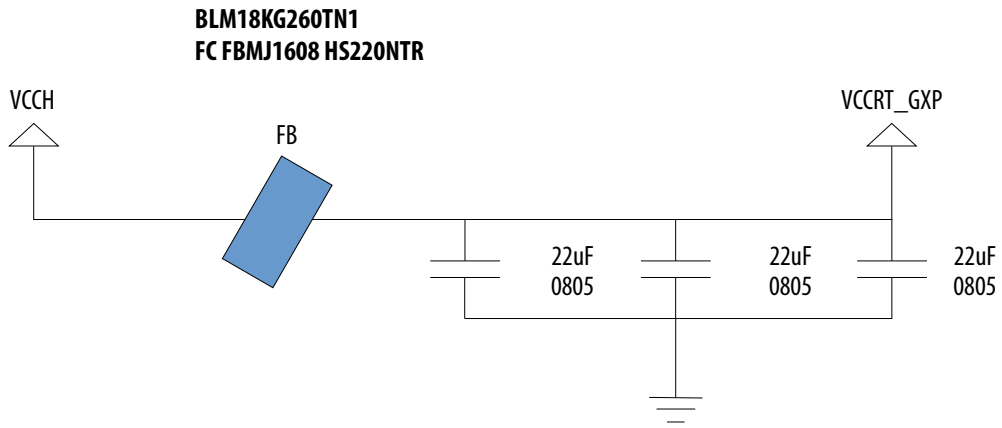


Figure 8. Filter Recommendation for VCCRT_GXP



5.2. E-Tile Rail LC Filter Board Scheme and Connection

The E-tile has a strict connection requirement to eliminate the need for PDS control circuits. With the connections in Figure 9 on page 25 and Figure 10 on page 26, the E-tile eliminates the PDS requirement existing in the Intel Stratix 10 device family—no pull-down discharge FETs or resistors on voltage rails are required. The filter can be placed as close to FPGA as periphery caps in Table 8 on page 15.

Figure 9. Connection Requirement and Filter Recommendation for VCCRT_GXE

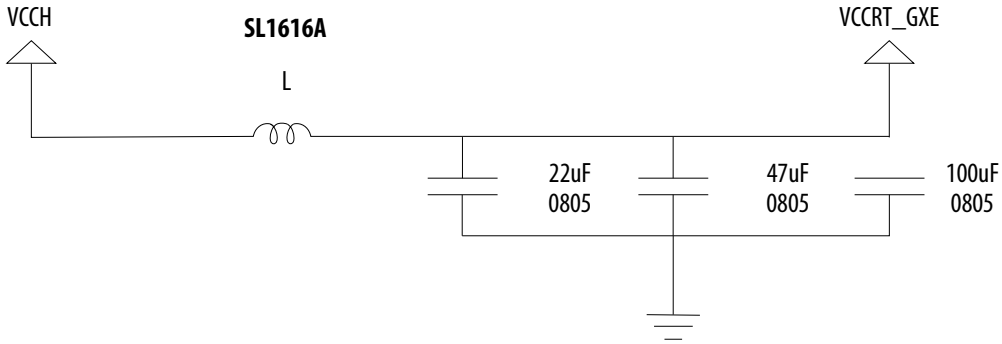
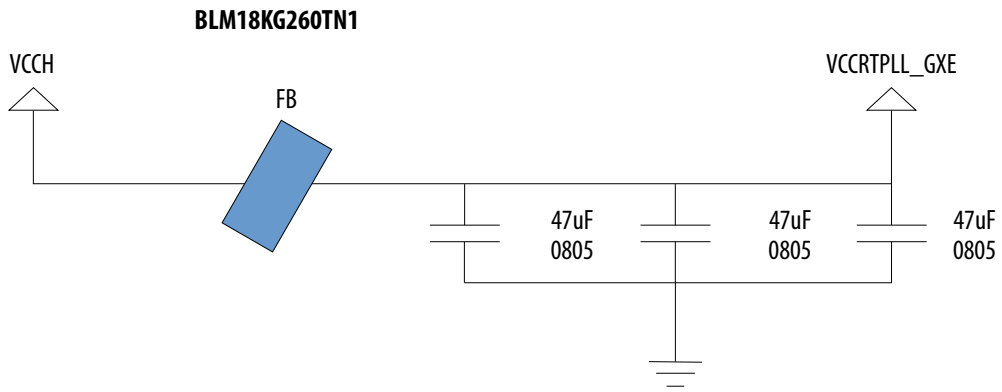


Figure 10. Connection Requirement and Filter Recommendation for VCCRTPLL_GXE



6. PCB Voltage Regulator Recommendation for Other Power Rails

Intel recommends that all Intel Agilex PCB-based designs to use the Intel Enpirion voltage regulators because of its capability, efficiency, and performance which have been validated on various Intel Agilex device family boards. Although you can use other voltage regulators, you are advised to use tested and trusted power solutions to remove the burden of validating other vendor solutions. This is to ensure that you can focus your bandwidth on validating and optimizing the FPGA intrinsic performances.

VCCIO_PIO_P1V2

The recommended voltage regulator solution for VCCIO_PIO_P1V2 is the *Intel Enpirion Power Solutions EM2120x01QI 20A PowerSoC*. For more information, refer to the Intel Enpirion Power Solutions EM2120x01QI 20A PowerSoC Datasheet.

VCCH

The recommended voltage regulator solution for VCCH is the *Intel Enpirion Power Solutions EM2140P0QI 40A PowerSoC*. For more information, refer to the Intel Enpirion Power Solutions EM2140P0QI 40A PowerSoC Datasheet.

VCCH_GXE

The recommended voltage regulator solution for VCCH_GXE is the *Intel Enpirion EN6340QI 4A PowerSoC*. For more information, refer to the Intel Enpirion EN6340QI 4A PowerSoC Datasheet.

VCCCLK_GXE

The recommended voltage regulator solution for VCCCLK_GXE is the *Intel Enpirion EZ6301QI Triple Output Module*. For more information, refer to the Intel Enpirion EZ6301QI Triple Output Module Datasheet.

VCCL_SDM

The recommended voltage regulator solution for VCCL_SDM is the *Intel Enpirion EZ6301QI Triple Output Module*. For more information, refer to the Intel Enpirion EZ6301QI Triple Output Module Datasheet.

P1V8_GR2

The recommended voltage regulator solution for P1V8_GR2 is the *Intel Enpirion EN63A0QI 12A PowerSoC*. For more information, refer to the Intel Enpirion EN63A0QI 12A PowerSoC Datasheet.

P1V8_GR3

The recommended voltage regulator solution for P1V8_GR3 is the *Intel Enpirion EZ6301QI Triple Output Module*. For more information, refer to the Intel Enpirion EZ6301QI Triple Output Module Datasheet.

VCCFUSEWR_SDM

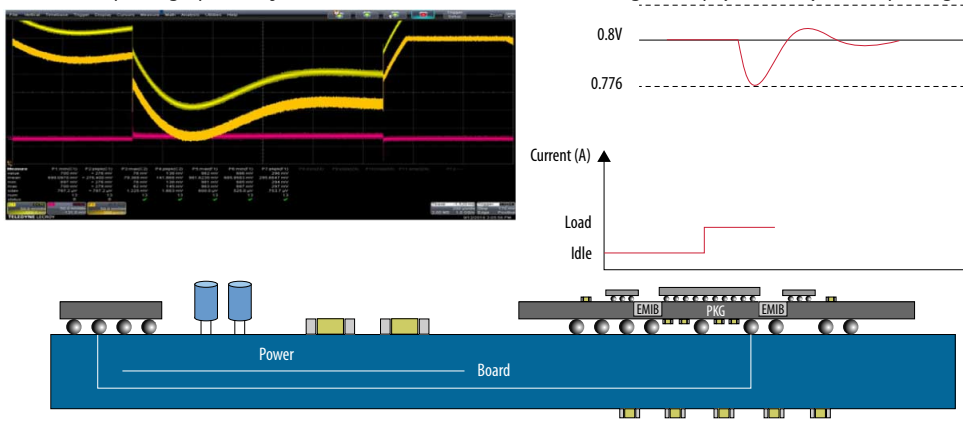
The recommended voltage regulator solution for VCCFUSEWR_SDM is the *Intel Enpirion EZ6301QI Triple Output Module*. For more information, refer to the Intel Enpirion EZ6301QI Triple Output Module Datasheet.

7. Board Power Delivery Network Simulations

In this section, the PDN post-layout simulation is shown in Figure 11 on page 29 for any Intel Agilex device family board design and system-level PDN simulation.

Figure 11. Methodology for Device PDN and Transient Noise Analysis

Step load at the package pin is injected to the PCB model to meet voltage droop (DC + AC) at the package pin.



Intel recommends you to follow the above-mentioned guidelines to design all power rails on the PCB with the recommended decoupling caps, voltage regulators, and LC filtering. In the post-layout phase, it is recommended to do the IR drop and transient (time domain) PDN analysis for PCB only. This means, unconventionally, we do not recommend impedance target and frequency target analysis (frequency domain simulation) for the Intel Agilex device.

To ensure the PDN design performance is within the required tolerance or specification in Table 6 on page 13, time domain post-layout PDN simulation for some critical power nets such as VCCL core, VCC, VCCR, VCCN, VCCH_AIB, VCC_HSSI_P-Tile, and VCCERT_P-Tile must be performed.

PDN time domain simulation is only performed on PCB from voltage regulator to package ball. Therefore, package, OPDs, and on-chip models are not required for the PDN time domain simulation.

The following steps show the time domain PDN simulation (as shown in Figure 12 on page 30):

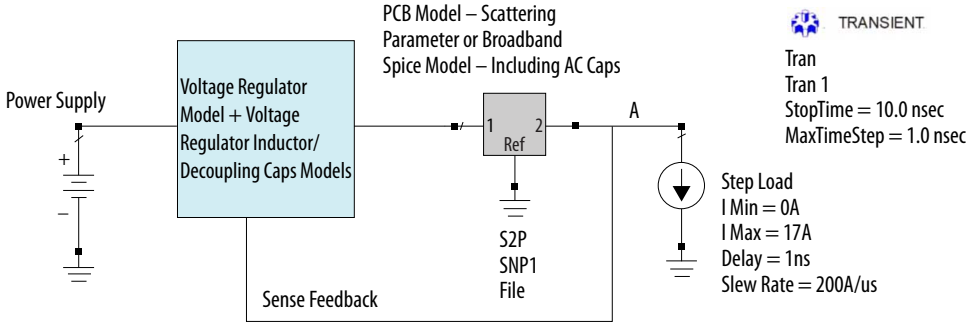
1. Obtain the implemented VRM model for the target power rail SPICE model.
2. Extract post-layout PCB model (HSPICE or scattering parameters by using tools such as PowerSI) of the PCB with decoupling caps and LC filtering from the voltage regulator (including VRM recommended bulk decaps by vendor) to package pin (if use of scattering parameters, the PCB model shall be extracted

from DC up to 1GHz). Intel recommends you to convert scattering parameters to circuit model by use of any broadband Spice or IDEM tool to avoid problematic simulation.

3. Build a schematic in any possible EDA tool (Keysight ADS or Cadence or LTspice) with the voltage regulator model (possible HSPICE model) and PCB model extracted from previous step.
   - This schematic represents the voltage regulator plus the PCB or decoupling caps model up to package pins.
   - Package, OPDs, or die model are not built into this schematic (Step load at package pin covers frequencies for only PCB, which means high current frequency components are eliminated through package and on-die).
   - Connect the sense pins from the package pin feedback to the voltage regulator sense pins.
4. Connect the maximum step load current at the package pins shown in Table 7 on page 14 (for example, for core, 200A/µs slew rate and step load of 17A).
5. Probe voltage drop at the package pin to see if the power rail specification in Table 6 on page 13 is met (for example, for VCCL core, the DC+AC voltage tolerance is ±3%).
   - If not meeting the package power rail tolerance or specification in Table 6 on page 13, you must check the PCB and adjust the decoupling caps or locations.

Figure 12. Time Domain PDN Test Bench Example for VCCL Core

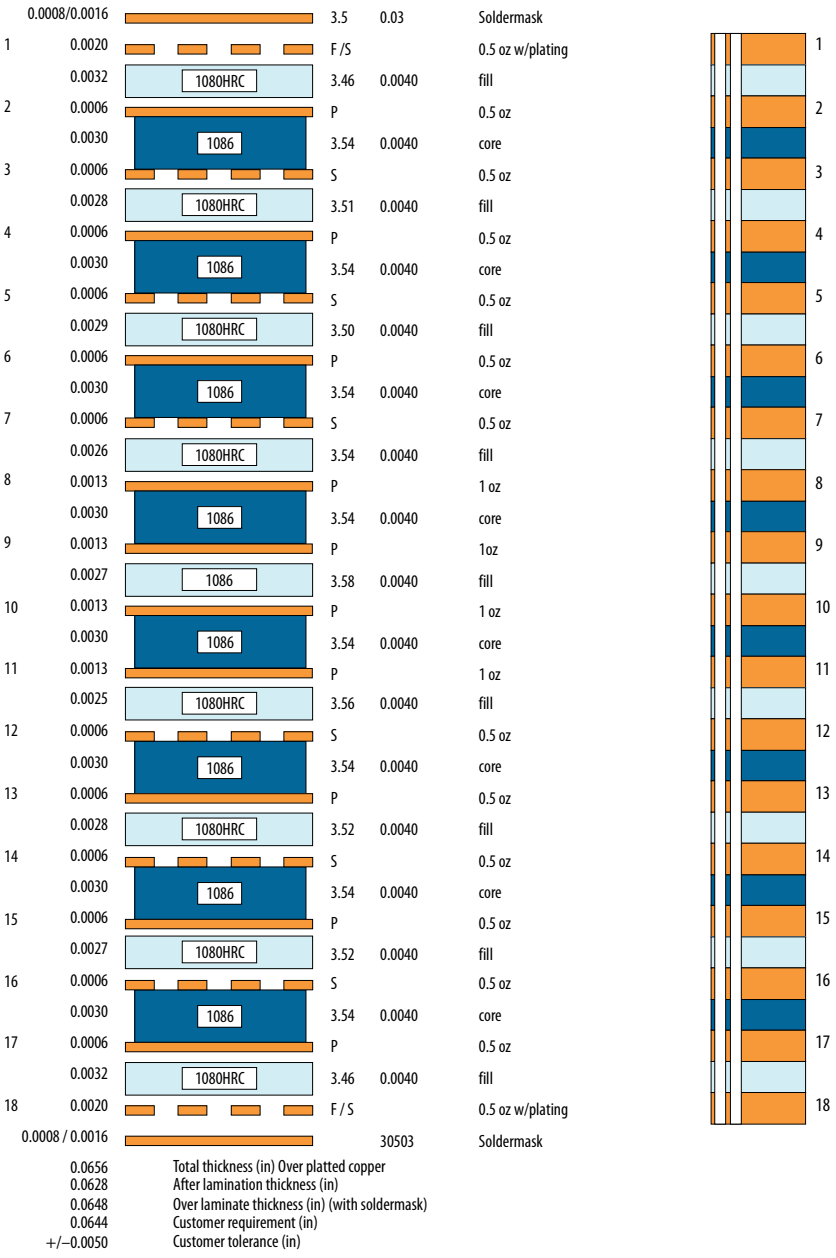
"A" is the VCCL node at the package ball (all VCCL pins at the package are connected to A). Voltage at "A" must be evaluated based on the voltage tolerance.



The PDN IR drop analysis is a DC simulation and must be performed on all power rails on the PCB up to package pins to meet the DC specification in Table 6 on page 13.

Figure 13 on page 31 shows the reference stackup used in the PDN design guideline and FPGA decoupling caps extraction. However, the FPGA PDN performance is also validated with a thicker PCB such the DK-SI-AGF014E3ES board designed in-house.

Figure 13. Reference Stackup



8. Intel Agilex Device Family PDN Design Summary

The summary of the Intel Agilex device family PDN design guidelines are as follow:

1. Current PDN design guidelines stand for the maximum power consumption—the worst use case.
   - If for any reason (various applications, configurations, or the PTC power data is lower than the maximum power used for the PDN design guideline), you must scale the recommended decoupling caps based on the ratio of design current to the maximum current. Use of ratio is an estimate and time domain simulation are mandatory to ensure meeting package ball voltage specification.
2. Apply the recommended power-up or power-down sequence grouping on the PCB. For more information, refer to AN 692: Intel Cyclone 10 GX, Intel Arria 10, Intel Stratix 10, and Intel Agilex Devices and Intel Agilex Power Management User Guide.
3. Use the recommended power tree presented in the Power Tree on page 7 for each Intel Agilex device with the suggested merged power nets.
   - Minimum 9 x voltage regulator is required on the PCB for the Intel Agilex AGF014 2486A Package Early Silicon and minimum 10 x voltage regulator is required on the PCB for Intel Agilex AGF014 production silicon. The recommended voltage regulators are only for FPGA and do not cover other devices on the board.
   - The minimum recommended number of voltage regulators on PCB is due to cost, area, and power-effective solution strategies. However, you can separate all power rails by the use of separate voltage regulators.
4. Use the recommended voltage regulators in the power tree or design your own voltage regulator based on the required maximum ripple or total current support per power rail on the PCB-VRM inductors or bulk caps must be designed separately. Tables in the Decoupling Caps Recommendation on page 14 show the FPGA decoupling caps and do not include the voltage regulator bulk caps.
5. Use the recommended bottom-side or FPGA periphery decoupling caps for each power net.
6. Use the recommended LC filters for power nets.
7. Use of sense line for IR drop compensation.
8. Configure the FPGA to follow the maximum recommended step load allowed at the package pin.

9. Do post-layout simulation for the IR drop analysis to see if this is within the DC specification at the package pin in Table 6 on page 13.
10. Do post-layout time domain PCB simulation up to the package pin for critical power nets such as the VCCL core to meet the AC voltage tolerance or specification at the package pin in Table 6 on page 13.
11. If not meeting the voltage tolerance (DC or AC) at the FPGA package pin, you must check the PCB and update the decoupling caps and redo the simulations.

9. Document Revision History for AN 910: Intel Agilex Power Distribution Network Design Guidelines

Document Version	Changes
2020.12.18	Updated Figure: *Recommended F-Series 2486A and 2581A Power Tree for Production Silicon* to correct VCCCLX_GXP to VCCCLK_GXP.
2020.12.16	Updated Figure: *Recommended F-Series 2486A and 2581A Power Tree for Production Silicon* to correct the power group for VCCA_PLL from 2 to 3.
2020.12.05	• Updated references to "ES silicon" to "early silicon" throughout the document. • Updated Figure: *Recommended F-Series 2486A Power Tree for Early Silicon*. • Updated Figure: *Recommended F-Series 2486A and 2581A Power Tree for Production Silicon*. • Updated the *Board Decoupling Caps Guide* topic: — Updated the VCCH cavity decaps on bottom side from 6x 0603 22µ to 4x 0603 22µ. — Added a note to clarify that the power tree and number of decoupling caps within cavity on Intel Agilex development kit boards may be slightly different than what has been recommended due to early release of silicon and guideline. • Updated Table: *Intel Agilex F-Series 2486A and 2581A FPGA Decoupling Caps Summary*. • Updated Table: *Required Rail Connections*.
2020.08.25	• Updated Figure: *Recommended F-Series 2486A Power Tree for ES Silicon*. • Updated note (1) in Figure: *Recommended F-Series 2486A and 2581A Power Tree for Production Silicon*.
2020.08.19	Initial release.