



# **AN 906: Intel® Stratix® 10 GX 400, SX 400, and TX 400 Routing and Designing Floorplan Guidelines**



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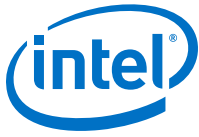


## 1. AN 906: Intel® Stratix® 10 GX 400, SX 400, and TX 400 Routing and Designing Floorplan Guidelines

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This document describes the routing and guidelines for the Intel® Stratix® 10 GX 400 (1SG040), SX 400 (1SX040), and TX 400 (1ST040) devices. The objective of these guidelines is to enable you to get the best possible timing performance of the Intel Stratix 10 GX 400, SX 400, and TX 400 devices.

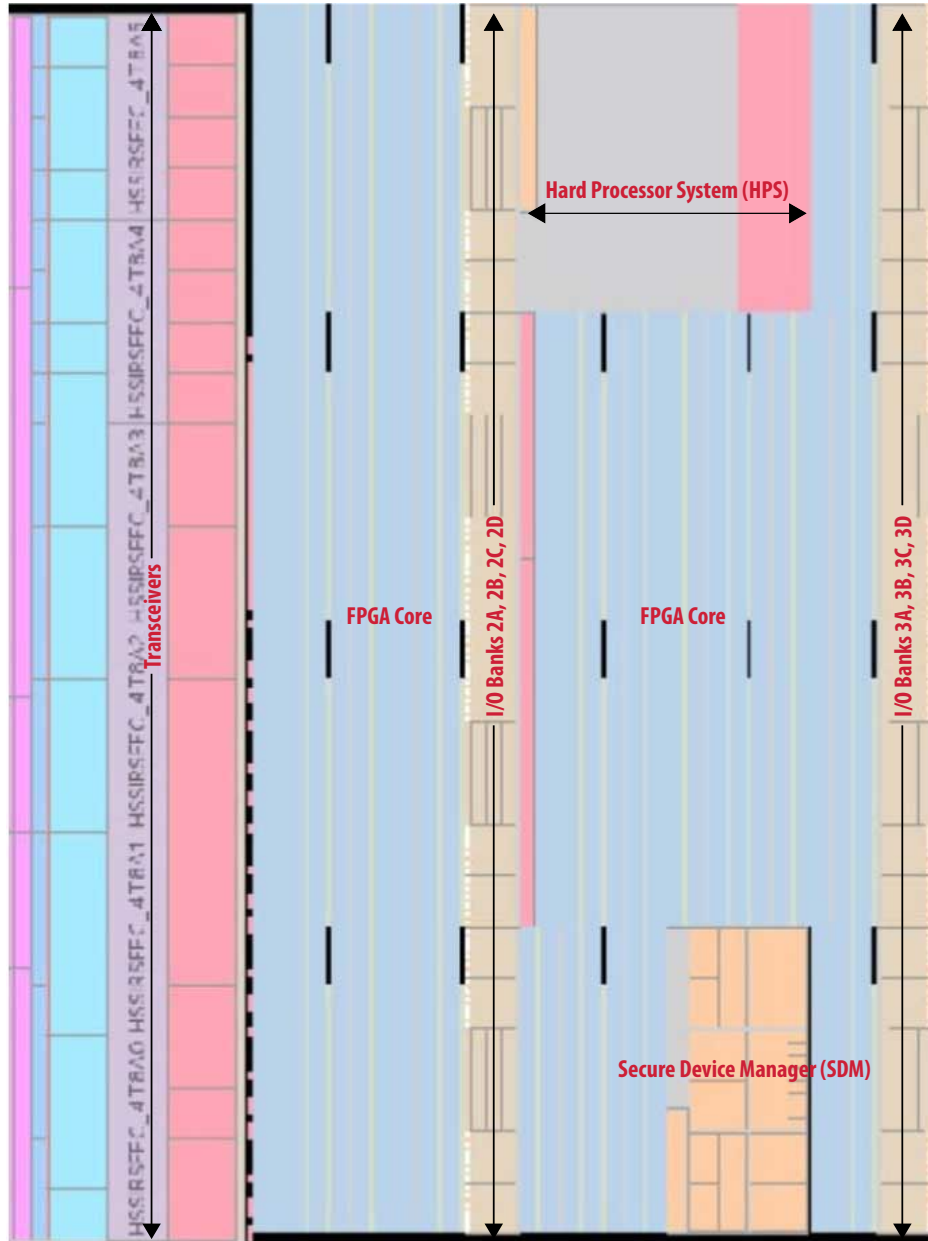
With the device floorplan and through real-design compilations, this document provides the recommendations for you to obtain the best achievable  $f_{MAX}$ .



## 1.1. Device Area Constraints

### 1.1.1. Chip Layout

Figure 1. Device Chip Layout



### 1.1.2. Floorplan Restrictions

There are notable restrictions on some areas because of the physical placement and resource availability which may affect the timing performance.



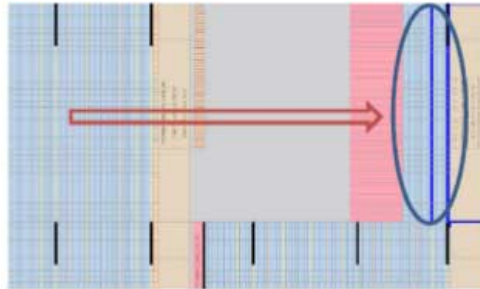
### 1.1.2.1. Possible Congestion Areas

#### 1.1.2.1.1. HPS and I/O Bank 3D Top-right Area

This is a place of possible congestion. Due to the fabric routing limitation, the external memory interface (EMIF) and LVDS on this side are not accessible.

#### Figure 2. HPS and I/O Bank 3D Top-right Possible Congestion Area

Intel recommends you to avoid the marked M20K line inside the area of emphasis to mitigate possible issues.

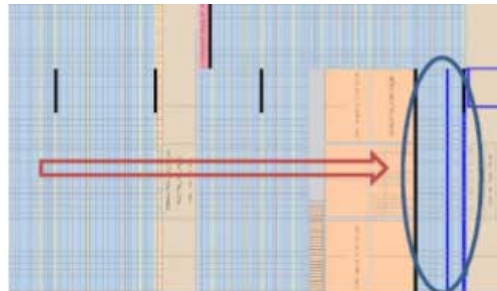


#### 1.1.2.1.2. SDM and I/O Bank 3A Bottom-right Area

This is also a place of possible congestion. The EMIF and LVDS on this side are not accessible as well.

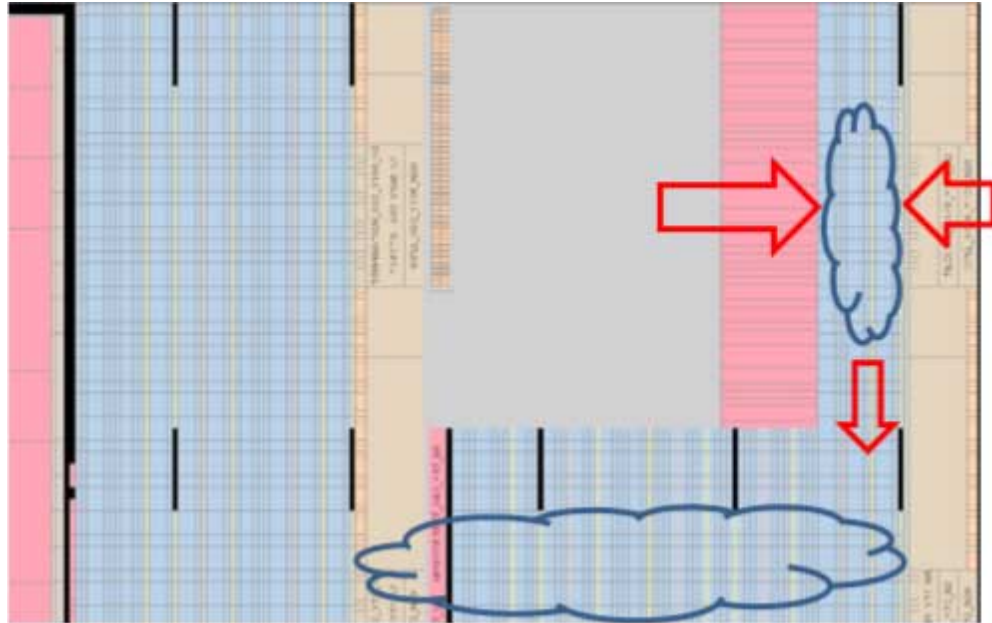
#### Figure 3. SDM and I/O Bank 3A Bottom-right Possible Congestion Area

Intel recommends you to avoid the marked M20K line inside the area of emphasis to mitigate possible issues.



### 1.1.2.2. HPS-to-Core and I/O-to-Core Traffic

Figure 4. HPS-to-Core and I/O-to-Core Traffic



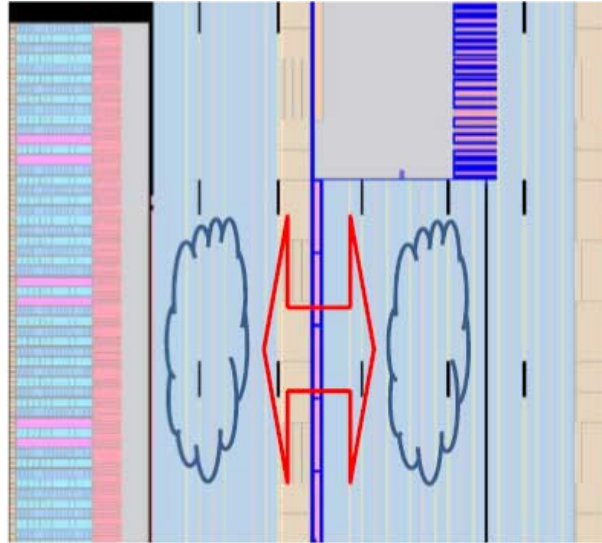
The hard processor system (HPS)-to-core connectivity on the top-right corner along with the routing congestion in the area makes the I/Os in that bank not suitable for EMIF and LVDS interfaces. Connecting the core logic at the right of the HPS interface to any logic going out of the area will increase the chance of routing congestion.

Limit the logic in the area by using the Logic Lock feature on designs to allow enough routing usage to ease congestion. If additional latency is allowed, pipelining helps mitigating the issue.



### 1.1.2.3. HPS Chimney

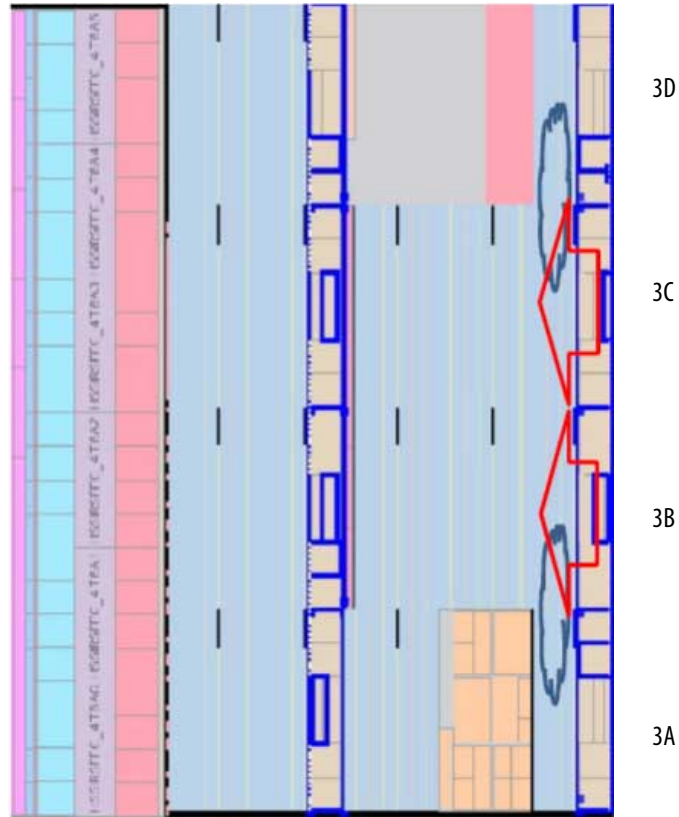
Figure 5. HPS Chimney



There is a risk in connecting logic on the left and right sides of the HPS chimney as shown in the figure above due to limited routing resources. Use the Logic Lock feature on designs to limit the amount of signals crossing the area and provide pipelines if allowed to facilitate retiming.

### 1.1.2.4. EMIF Usage

Figure 6. EMIF Usage



There is a risk of closing timing in the EMIF usage on banks 3B and 3C if the HPS and secure device manager (SDM) usage on top and bottom provides congestion in areas crossing the EMIF logic interfaces. Proper usage placement of EMIFs helps lessen the congestion.

You will be unable to access the EMIF usage on banks 3A and 3D due to a high risk of not being able to meet timing. Logic and memory resources available aggravated by routability issues at the right-bottom corner between the SDM and EMIF bank 3A and at the top-right corner between the HPS and EMIF bank 3D make it hard to meet timing closure.

**Table 1. Bank 3A, Bank 3B, Bank 3C, and Bank 3D Usage in Intel Stratix 10 GX 400, SX 400, and TX 400 Devices**

Bank	Intel Stratix 10 TX 400 (1ST040)	Intel Stratix 10 GX 400 (1SG040) and SX 400 (1SX040)
3A	Use for any general-purpose I/O (GPIO)	Use for GPIO only
3B	Use for GPIO, EMIF, or LVDS	Use for GPIO, EMIF, or LVDS
3C	Use for GPIO, EMIF, or LVDS	Use for 3.3V GPIOs only
3D	Use for any GPIO	Use for 1.8V GPIO only (it has 30 pins)





Real-design experiments will determine if a combination of HPS, SDM, and EMIFs on the right column is feasible.

### 1.1.3. Logic Utilization

With the preliminary internal investigations, Intel recommends you to keep the logic utilization in your design below 70%. For designs with more than 70% logic utilization, there is a high risk that your design might not meet the timing requirements.

Initial analysis of push button performance is based on a design with the following logic utilization and clock frequencies.

**Table 2. Example Logic Utilization and Clock Frequencies**

Clock Frequency (MHz)	Logic Utilization
491	16%
368	25%
320	25%

Allow register transfer level (RTL) rewrite and pipelining to help meet timing requirements.

## 1.2. Document Revision History for AN 906: Intel Stratix 10 GX 400, SX 400, and TX 400 Routing and Designing Floorplan Guidelines

Document Version	Changes
2020.02.06	Initial release.