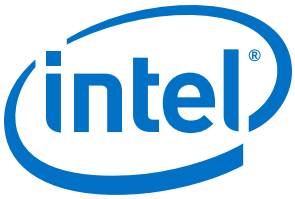

AN 890: JESD204B Intel® FPGA IP and ADI AD9174 Interoperability Report for Intel Stratix® 10 L-Tile Devices

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Contents

1. JESD204B Intel® FPGA IP and ADI AD9174 Hardware Checkout Report for Intel Stratix® 10 Devices

The JESD204B Intel® FPGA IP is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204B Intel FPGA IP has been hardware-tested with a number of selected JESD204B-compliant analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices.

This report highlights the interoperability of the JESD204B Intel FPGA IP with the AD9174 DAC Evaluation Module (EVM) Rev C from Analog Devices Inc. (ADI). The following sections describe the hardware checkout methodology and test results.

Related Information

JESD204B Intel FPGA IP User Guide

1.1. Hardware Requirements

The hardware checkout test requires the following hardware and software tools:

- Intel Stratix® 10 GX Signal Integrity Development Kit (ES Edition) with Intel Stratix 10 1SX280LU2F50E2VGS3 (transceiver L-tile) device
- ADI AD9174 DAC EVM Rev C
- Mini-USB cables
- SMA cables
- Tektronix TBS1202B digital storage oscilloscope

1.2. Hardware Setup

An Intel Stratix 10 GX Signal Integrity Development Kit (ES Edition) is used with the ADI AD9174 daughter card module installed to the development board's FMC+ connector.

- The AD9174 EVM derives power from the FMC+ pins.
- The FPGA clock is supplied by a Silicon Labs Si5341 clock generator on the development kit.
- The Si5341 clock generator provides a reference clock to the HMC7044 clock generator in the AD9174 EVM through an SMA cable. The phase-locked loop (PLL) in the AD9174 device generates the desired sampling clock.
- For subclass 1, the HMC7044 clock generator in the AD9174 EVM provides the SYSREF for the FPGA as well as the AD9174 device.
- The sync_n signal is transmitted from the DAC to the FPGA through the FMC+ pins.

Figure 1. Hardware Setup

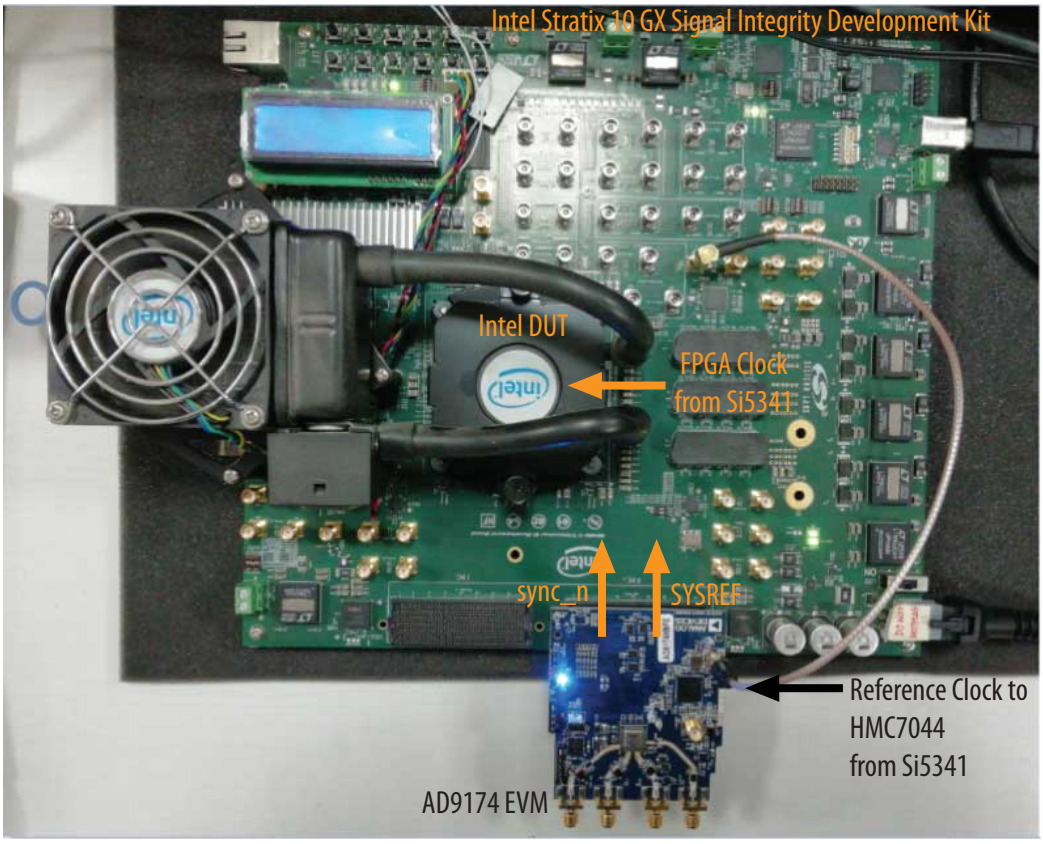
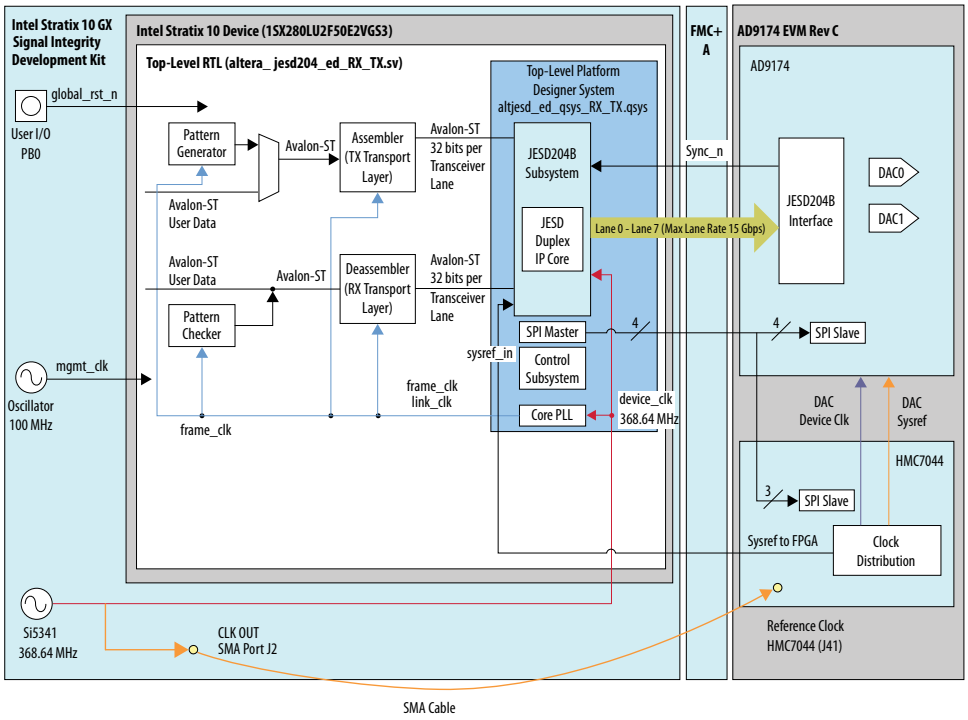


Figure 2. System Diagram

This system-level diagram shows how the different modules connect.



In this setup, where LMF = 821, the data rate of the transceiver lanes is 14.7456 Gbps. The HMC7044 clock generator in the AD9174 EVM provides SYSREF for both the FPGA and DAC. It also provides the reference clock to the DAC PLL to generate the desired DAC sample rate of 11796.48 Msps. The AD9174 DAC provides the sync_n signal through the FMC+ pins. The AD9174 DAC can operate in single or dual JESD links. The HMC7044 clock generator and DAC are programmed by the FPGA through the serial peripheral interface (SPI).

1.3. Hardware Checkout Methodology

This section describes the test objectives, procedures, and passing criteria. The test covers the following areas:

- Transmitter data link layer
- Transmitter transport layer
- Scrambling
- Deterministic latency (subclass 1)

1.3.1. Transmitter Data Link Layer

This test area covers the test cases for code group synchronization (CGS) and initial lane alignment (ILA) sequence.

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The Signal Tap logic analyzer monitors the transmitter data link layer operation.

1.3.1.1. Code Group Synchronization

Table 1. CGS Test Cases

Test Case	Objective	Description	Passing Criteria
CGS.1	Check that /K/ characters are transmitted when sync_n is asserted.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_tx_pcs_data[(L*32)-1..0] • jesd204_tx_pcs_kchar_data[(L*4)-1..0](1) The following signals in <*ip_variant_name*>.v are tapped: • sync_n • jesd204_tx_int The txlink_clk signal is used as the sampling clock for the Signal Tap logic analyzer. Each lane is represented by a 32-bit data bus for the jesd204_tx_pcs_data signal. The 32-bit data bus is divided into four octets. Check for the following status in the AD9174 register: • Code Group Synchronization Status	• The /K/ character or K28.5 (0xBC) is transmitted at each octet of the jesd204_tx_pcs_data bus when the receiver asserts the sync_n signal. • The jesd204_tx_pcs_kchar_data signal is asserted whenever control characters such as the /K/, /R/, /Q/, or /A/ characters are transmitted. • The jesd204_tx_int signal is deasserted if there is no error. • "Code Group Synchronization Status" for all lanes are asserted in the AD9174 register 0x470.
CGS.2	Check that /K/ characters are transmitted after sync_n is deasserted but before the start of multiframe.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_tx_pcs_data[(L*32)-1..0] • jesd204_tx_pcs_kchar_data[(L*4)-1..0](1) The following signals in <*ip_variant_name*>.v are tapped: • sync_n • tx_sysref • jesd204_tx_int The txlink_clk signal is used as the sampling clock for the Signal Tap logic analyzer. Each lane is represented by a 32-bit data bus for the jesd204_tx_pcs_data signal. The 32-bit data bus is divided into four octets. Check for the following errors in the AD9174 register: • 8b/10b Not-in-Table Error • 8b/10b Disparity Error	• /K/ character transmission continues for at least one frame plus nine octets. • The sync_n and jesd204_tx_int signals are deasserted. • "8b/10b Not-in-Table Error" and "8b/10b Disparity Error" are not asserted in the AD9174 registers 0x46E and 0x46D, respectively.

(1) L is the number of lanes.

1.3.1.2. Initial Frame and Lane Synchronization

Table 2. Initial Frame and Lane Synchronization Test Cases

Test Case	Objective	Description	Passing Criteria
ILA.1	Check that the /R/ and /A/ characters are transmitted at the beginning and end of each multiframe. Verify that four multiframes are transmitted in the ILAS phase and the receiver detects the initial lane alignment sequence correctly.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_tx_pcs_data[(L*32)-1..0] • jesd204_tx_pcs_kchar_data[(L*4)-1..0](2) The following signals in <*ip_variant_name*>.v are tapped: • sync_n • jesd204_tx_int The txlink_clk signal is used as the sampling clock for the Signal Tap logic analyzer. Each lane is represented by a 32-bit data bus for the jesd204_tx_pcs_data signal. The 32-bit data bus is divided into four octets. Check for the following status in the AD9174 registers: • Frame Synchronization • Initial Lane Synchronization	• The /R/ character or K28.0 (0x1C) is transmitted at the jesd204_tx_pcs_data bus to mark the beginning of each multiframe. • The /A/ character or K28.3 (0x7C) is transmitted at the jesd204_tx_pcs_data bus to mark the end of each multiframe. • The sync_n and jesd204_tx_int signals are deasserted. • The jesd204_rx_pcs_kchar_data signal is asserted whenever control characters such as the /K/, /R/, /Q/, or /A/ characters are transmitted. • The "Frame Synchronization" and "Initial Lane Synchronization" status for all lanes are asserted in the AD9174 registers 0x471 and 0x473, respectively.
ILA.2	Check that the JESD204B configuration parameters are transmitted in the second multiframe.	The following signal in <*ip_variant_name*>_inst_phy.v is tapped: • jesd204_tx_pcs_data[(L*32)-1..0](2) The following signal in <*ip_variant_name*>.v is tapped: • jesd204_tx_int The txlink_clk signal is used as the sampling clock for the Signal Tap logic analyzer. The system console accesses the following registers: • ilas_data1 • ilas_data2 The content of 14 configuration octets in the second multiframe is stored in the above 32-bit registers. Check for the following status and error in the AD9174 registers:	• The /R/ character is followed by the /Q/ character or K28.4 (0x9C) in the jesd204_tx_pcs_data signal at the beginning of the second multiframe. • The jesd204_tx_int signal is deasserted if there is no error. • The JESD204B parameters read from the ilas_data1 and ilas_data2 registers are the same as the parameters set in the JESD204B Intel FPGA IP Platform Designer component editor. • The "Good Checksum" status is asserted in the AD9174 register 0x472. • "Link Configuration Mismatch Error" is not asserted in the AD9174 register 0x4BB.

continued...

(2) L is the number of lanes.

Test Case	Objective	Description	Passing Criteria
		• Good Checksum • Configuration Mismatch Error	
ILA.3	Check the constant pattern of the transmitted user data after the end of the fourth multiframe. Verify that the receiver successfully enters user data phase.	The following signal in <*ip_variant_name*>_inst_phy.v is tapped: • jesd204_tx_pcs_data[(L*32)-1..0](2) The following signal in <*ip_variant_name*>.v is tapped: • jesd204_tx_int The txlink_clk signal is used as the sampling clock for the Signal Tap logic analyzer. The system console accesses the JESD configuration and status register (CSR) tx_err. Check for the following errors in the AD9174 registers: • Lane FIFO Full • Lane FIFO Empty	• When the scrambler is turned off, the first user data is transmitted after the last /A/ character, which marks the end of the fourth multiframe transmitted.(3) • Bits 2 and 3 of the JESD tx_err register are not set to "1". • The "Lane FIFO Full" and "Lane FIFO Empty" errors are not asserted in the AD9174 registers 0x30C and 0x30D, respectively. • The jesd204_tx_int signal is deasserted if there is no error.

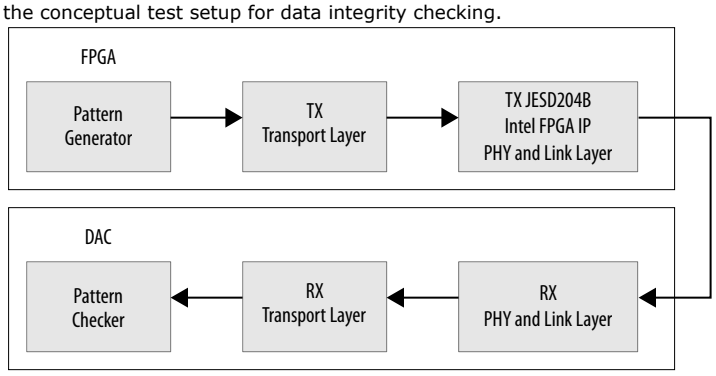
1.3.2. Transmitter Transport Layer

To verify the data integrity of the payload data stream through the transmitter (TX) JESD204B Intel FPGA IP and transport layer, the DAC JESD core is configured to check the short transport layer (STPL) test pattern that is transmitted from the FPGA's test pattern generator. The DAC JESD core checks the transport layer test patterns based on the F = 1, 2, 3, 4, or 8 configuration. The STPL test pattern has a duration of one frame period and is repeated continuously for the duration of the test.

To verify that data from the FPGA digital domain is successfully sent to the DAC analog domain, the FPGA is configured to generate a sine wave. An oscilloscope is used to observe the waveform at the DAC analog channels.

Figure 3. Data Integrity Check Using Short Transport Layer Test Pattern Checker

This figure shows the conceptual test setup for data integrity checking.



The Signal Tap logic analyzer monitors the operation of the TX transport layer.

(3) When the scrambler is turned on, the data pattern cannot be recognized after the fourth multiframe in the ILAS phase.

Table 3. Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
TL.1	Check the transport layer mapping using the STPL test pattern.	The following signals in `altera_jesd204_transport_tx_top.sv` are tapped: • `jesd204_tx_data_valid` • `jesd204_tx_data_ready` The following signal in `altera_jesd204_ed_RX_TX.sv` is tapped: • `jesd204_tx_int` The `txframe_clk` signal is used as the sampling clock for the Signal Tap logic analyzer. Check the following in the DAC: • STPL test status	• The `jesd204_tx_data_ready` and `jesd204_tx_data_valid` signals are asserted. • The STPL test status in DAC register 0x32F for all DACs does not show an error. • The `jesd204_tx_int` signal is deasserted if there is no error.
TL.2	Verify the data transfer from digital to analog domain.	Enable the sine wave generator in the FPGA and observe the DAC analog channel output on the oscilloscope.	A monotone sine wave is observed on the oscilloscope.

1.3.3. Scrambling

With the descrambler enabled, the transport layer test pattern checker at the DAC JESD core checks the data integrity of the scrambler in the FPGA.

The Signal Tap logic analyzer monitors the operation of the TX transport layer.

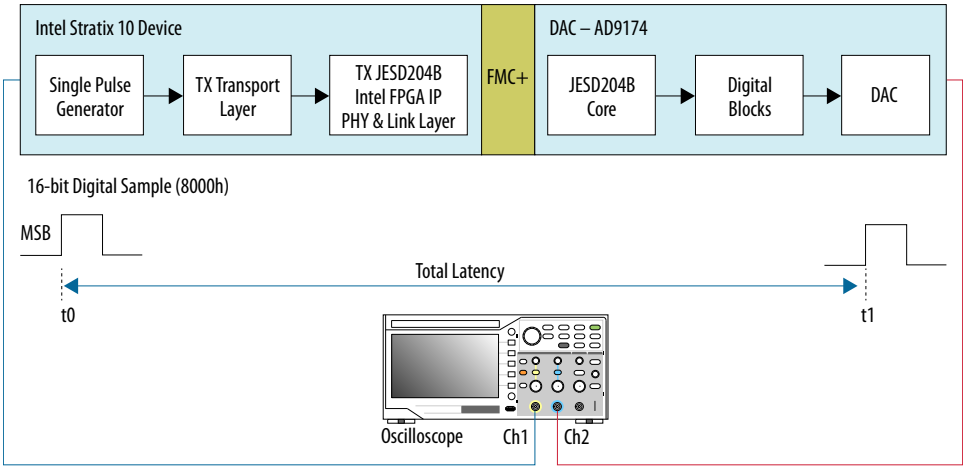
Table 4. Scrambler Test Cases

Test Case	Objective	Description	Passing Criteria
SCR.1	Check the functionality of the scrambler using the STPL test pattern as specified in the parameter configuration.	Enable the descrambler at the DAC JESD core and the scrambler at the TX JESD204B Intel FPGA IP. The signals that are tapped in this test case are similar to test case TL.1. Check the following in the DAC: • STPL test status	• The `jesd204_tx_data_ready` and `jesd204_tx_data_valid` signals are asserted. • The STPL test status in DAC register 0x32F for all DACs does not show an error. • The `jesd204_tx_int` signal is deasserted if there is no error.
SCR.2	Verify the data transfer from digital to analog domain.	Enable the descrambler at the DAC JESD core and the scrambler at the TX JESD204B Intel FPGA IP. Enable the sine wave generator in the FPGA and observe the DAC analog channel output on the oscilloscope.	A monotone sine wave is observed on the oscilloscope.

1.3.4. Deterministic Latency (Subclass 1)

The following figure shows the block diagram of the deterministic latency test setup. The HMC7044 clock generator in the AD9174 EVM provides periodic SYSREF pulses for both the DAC and JESD204B Intel FPGA IP.

Figure 4. Deterministic Latency Test Setup Block Diagram



The FPGA generates a 16-bit digital sample with a value of 8000 (hexadecimal) at the transport layer. The most-significant bit of this digital sample has a logic 1 value. This bit is routed out from the FPGA and probed at channel 1 of the oscilloscope. The DAC analog channel is probed at channel 2 of the oscilloscope. The time difference between the pulses at channel 1 (t0) and channel 2 (t1) is measured. This time difference represents the total latency of the JESD204B link, DAC digital blocks, and analog channel.

Table 5. Deterministic Latency Test Cases

Test Case	Objective	Description	Passing Criteria
DL.1	Measure the total latency.	Measure the time difference between the rising edge of pulses at channels 1 and 2 of the oscilloscope.	Latency is consistent.
DL.2	Re-measure the total latency after the DAC power cycle and FPGA reconfiguration.	Measure the time difference between the rising edge of pulses at channels 1 and 2 of the oscilloscope.	Latency is consistent.

1.4. JESD204B Intel FPGA IP and DAC Configurations

The JESD204B Intel FPGA IP parameters (L, M, and F) in this hardware checkout are natively supported by the AD9174 device's configuration registers. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the AD9174 operating conditions.

The hardware checkout testing implements the JESD204B Intel FPGA IP with the following parameter configurations.

Table 6. Parameter Configuration

Mode	LMF	N/ N'	S	Channel per DAC	Interpolation	DAC Rate (Msps)	Data Rate (Msps)	Lane Rate (Mbps)	FPGA Device Clock (MHz)(4)	FPGA Link Clock (MHz)(5)	FPGA Frame Clock (MHz)(5)	Data Pattern(6)(7)(8)
0	124	16	1	1	16	5898.24	3686.4	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xFEBC, M1S0 – 0xA5ED
1	244	16	1	2	32	11796.48	3686.4	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M1S0 – 0xD3C4, M2S0 – 0xB5A6, M3S0 – 0x9780
2	364	16	1	3	32	11796.48	3686.4	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M1S0 – 0xD3C4, M2S0 – 0xB5A6, M3S0 – 0x9780, M4S0 – 0xFEBC , M5S0 – 0xA5ED
3	222	16	1	1	8	5898.24	7372.8	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xFEBC, M1S0 – 0xA5ED
4	442	16	1	2	16	11796.48	7372.8	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M1S0 – 0xD3C4, M2S0 – 0xB5A6, M3S0 – 0x9780
5	123	12	1	1	12	5898.24	4915.2	14745.6	368.64	368.64	245.76	Sine, single pulse, constant, M0S0 – 0xFEB, M1S0 – 0xA5E
6	243	12	1	2	24	11796.48	4915.2	14745.6	368.64	368.64	245.76	Sine, single pulse, constant, M0S0 – 0xF1E, M1S0 – 0xD3C, M2S0 – 0x5EC, M3S0 – 0xA3D

continued...

(4) The device clock is used to clock the transceiver.

(5) The link clock and frame clock are derived from the device clock using an internal PLL.

(6) The sine wave pattern is used in the TL.2 and SCR.2 test cases to verify that the pattern generated in the FPGA transport layer is transmitted by the DAC analog channel.

(7) The single pulse pattern is used in the deterministic latency test cases DL.1 and DL.2 only.

(8) The constant pattern is used for the STPL test.

Mode	LMF	N/ N'	S	Channel per DAC	Interpolation	DAC Rate (Msps)	Data Rate (Msps)	Lane Rate (Mbps)	FPGA Device Clock (MHz)(4)	FPGA Link Clock (MHz)(5)	FPGA Frame Clock (MHz)(5)	Data Pattern(6)(7)(8)
7	148	16	1	2	64	11796.48	1843.20	14745.6	368.64	368.64	184.32	Sine, single pulse, constant, M0S0 – 0xF1E2, M1S0 – 0xD3C4, M2S0 – 0xB5A6, M3S0 – 0x9780
8	421	16	1	1	8	11796.48	1474.56	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xFEBC, M1S0 – 0xA5ED
9	422	16	2	1	8	11796.48	1474.56	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M0S1 – 0xD3C4, M1S0 – 0xB5A6, M1S1 – 0x9780
10	821	16	2	1	4	11796.48	2949.12	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M0S1 – 0xD3C4, M1S0 – 0xB5A6, M1S1 – 0x9780
11	822	16	4	1	4	11796.48	2949.12	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M0S1 – 0xD3C4, M0S2 – 0xB5A6, M0S3 – 0x9780, M1S0 – 0x5ECB, M1S1 – 0xAED5, M1S2 – 0x49AD, M1S3 – 0xF1BC
12	823	12	8	1	2	5898.24	2949.12	11059.2	368.64	276.48	184.32	Sine, single pulse, constant, M0S0 – 0xF1E, M0S1 – 0xD3C, M0S2 – 0xB5A, M0S3 – 0x978, M0S4 – 0x5EC, M0S5 – 0xAED, M0S6 – 0x49A,

continued...

(4) The device clock is used to clock the transceiver.

(5) The link clock and frame clock are derived from the device clock using an internal PLL.

(6) The sine wave pattern is used in the TL.2 and SCR.2 test cases to verify that the pattern generated in the FPGA transport layer is transmitted by the DAC analog channel.

(7) The single pulse pattern is used in the deterministic latency test cases DL.1 and DL.2 only.

(8) The constant pattern is used for the STPL test.

Mode	LMF	N/ N'	S	Channel per DAC	Interpolation	DAC Rate (Msps)	Data Rate (Msps)	Lane Rate (Mbps)	FPGA Device Clock (MHz)(4)	FPGA Link Clock (MHz)(5)	FPGA Frame Clock (MHz)(5)	Data Pattern(6) (7)(8)
												M0S7 – 0xF1B, M1S0 – 0xF50, M1S1 – 0xD6E, M1S2 – 0xB8C, M1S3 – 0x9AA, M1S4 – 0x61E, M1S5 – 0xB1F, M1S6 – 0x4CC, M1S7 – 0xF4D
18	411	16	2	1	1	2949.12	2949.12	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xFEBC, M1S0 – 0xA5ED
19	412	16	4	1	1	2949.12	2949.12	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M0S1 – 0xD3C4, M0S2 – 0xB5A6, M0S3 – 0x9780, M0S4 – 0x5ECB, M0S5 – 0xAED5, M0S6 – 0x49AD, M0S7 – 0xF1BC
20	811	16	4	1	1	5898.24	5898.24	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M0S1 – 0xD3C4, M0S2 – 0xB5A6, M0S3 – 0x9780
21	812	16	8	1	1	5898.24	5898.24	14745.6	368.64	368.64	368.64	Sine, single pulse, constant, M0S0 – 0xF1E2, M0S1 – 0xD3C4, M0S2 – 0xB5A6, M0S3 – 0x9780, M0S4 – 0x5ECB, M0S5 – 0xAED5, M0S6 – 0x49AD, M0S7 – 0xF1BC
22	423	12	4	1	6	11796.48	1966.08	14745.6	368.64	368.64	245.76	Sine, single pulse, constant, M0S0 – 0xF1E, M0S1 – 0xD3C, M0S2 – 0xB5A, M0S3 – 0x978, M1S0 – 0x5EC,

(4) The device clock is used to clock the transceiver.
(5) The link clock and frame clock are derived from the device clock using an internal PLL.
(6) The sine wave pattern is used in the TL.2 and SCR.2 test cases to verify that the pattern generated in the FPGA transport layer is transmitted by the DAC analog channel.
(7) The single pulse pattern is used in the deterministic latency test cases DL.1 and DL.2 only.
(8) The constant pattern is used for the STPL test.

Mode	LMF	N/ N'	S	Channel per DAC	Interpolation	DAC Rate (Msps)	Data Rate (Msps)	Lane Rate (Mbps)	FPGA Device Clock (MHz)(4)	FPGA Link Clock (MHz)(5)	FPGA Frame Clock (MHz)(5)	Data Pattern(6)(7)(8)
												M1S1 – 0xAED, M1S2 – 0x49A, M1S3 – 0xF1B

1.5. Test Results

The following table contains the possible results and their definition.

Table 7. Results Definition

Result	Definition
PASS	The device under test (DUT) was observed to exhibit conformant behavior.
PASS with comments	The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included (example: due to time limitations, only a portion of the testing was performed).
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Refer to comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, TL.2, SCR.1, and SCR.2 with K = 32, subclass 1, and different values of L, M, F, data rate, sampling clock, link clock, and SYSREF pulse frequency.

Table 8. Results for Test Cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, TL.2, SCR.1, and SCR.2

Test No.	L	M	F	SCR(9)	Lane Rate (Gbps)	DAC Rate (Msps)	Link Clock (MHz)	SYSREF Pulse Frequency (MHz)	Result
1	1	2	4	0	14.7456	5898.24	368.64	11.52	PASS
2	1	2	4	1	14.7456	5898.24	368.64	11.52	PASS
3	2	4	4	0	14.7456	11796.48	368.64	11.52	PASS
4	2	4	4	1	14.7456	11796.48	368.64	11.52	PASS
5	3	6	4	0	14.7456	11796.48	368.64	11.52	PASS
6	3	6	4	1	14.7456	11796.48	368.64	11.52	PASS

continued...

(4) The device clock is used to clock the transceiver.
(5) The link clock and frame clock are derived from the device clock using an internal PLL.
(6) The sine wave pattern is used in the TL.2 and SCR.2 test cases to verify that the pattern generated in the FPGA transport layer is transmitted by the DAC analog channel.
(7) The single pulse pattern is used in the deterministic latency test cases DL.1 and DL.2 only.
(8) The constant pattern is used for the STPL test.

(9) SCR denotes scrambler. 0 = scrambler disabled; 1 = scrambler enabled.

Test No.	L	M	F	SCR[9]	Lane Rate (Gbps)	DAC Rate (Msps)	Link Clock (MHz)	SYSREF Pulse Frequency (MHz)	Result
7	2	2	2	0	14.7456	5898.24	368.64	23.04	PASS
8	2	2	2	1	14.7456	5898.24	368.64	23.04	PASS
9	4	4	2	0	14.7456	11796.48	368.64	23.04	PASS
10	4	4	2	1	14.7456	11796.48	368.64	23.04	PASS
11	1	2	3	0	14.7456	11796.48	368.64	15.36	PASS
12	1	2	3	1	14.7456	11796.48	368.64	15.36	PASS
13	2	4	3	0	14.7456	11796.48	368.64	15.36	PASS
14	2	4	3	1	14.7456	11796.48	368.64	15.36	PASS
15	1	4	8	0	14.7456	11796.48	368.64	5.76	PASS
16	1	4	8	1	14.7456	11796.48	368.64	5.76	PASS
17	4	2	1	0	14.7456	11796.48	368.64	46.08	PASS
18	4	2	1	1	14.7456	11796.48	368.64	46.08	PASS
19	4	2	2	0	14.7456	11796.48	368.64	23.04	PASS
20	4	2	2	1	14.7456	11796.48	368.64	23.04	PASS
21	8	2	1	0	14.7456	11796.48	368.64	46.08	PASS
22	8	2	1	1	14.7456	11796.48	368.64	46.08	PASS
23	8	2	2	0	14.7456	11796.48	368.64	23.04	PASS
24	8	2	2	1	14.7456	11796.48	368.64	23.04	PASS
25	8	2	3	0	14.7456	5898.24	368.64	11.52	PASS
26	8	2	3	1	14.7456	5898.24	368.64	11.52	PASS
27	4	1	1	0	14.7456	2949.12	368.64	23.04	PASS
28	4	1	1	1	14.7456	2949.12	368.64	23.04	PASS
29	4	1	2	0	14.7456	2949.12	368.64	11.52	PASS
30	4	1	2	1	14.7456	2949.12	368.64	11.52	PASS
31	8	1	1	0	14.7456	5898.24	368.64	46.08	PASS
32	8	1	1	1	14.7456	5898.24	368.64	46.08	PASS
33	8	1	2	0	14.7456	5898.24	368.64	23.04	PASS
34	8	1	2	1	14.7456	5898.24	368.64	23.04	PASS
35	4	2	3	0	14.7456	11796.48	368.64	15.36	PASS
36	4	2	3	1	14.7456	11796.48	368.64	15.36	PASS

(9) SCR denotes scrambler. 0 = scrambler disabled; 1 = scrambler enabled.

The following table shows the results for test cases DL.1 and DL.2 with K = 32, subclass 1, and different values of L, M, F, lane rate, sampling clock, link clock, and SYSREF pulse frequency. This table also shows the configured values for the DAC registers LMFCVar (RBD offset) and LMFCDel (LMFC offset) to achieve the deterministic latencies tabulated.

Table 9. Results for Deterministic Latency Test

Test No.	L	M	F	Lane Rate (Gbps)	DAC Rate (Msps)	Link Clock (MHz)	LMFCVar	LMFCDel	SYSREF Pulse Frequency (MHz)	Total Latency (ns)	Result
1	1	2	4	14.7456	5898.24	368.64	0x05	0x08	11.52	364 to 368	PASS
2	2	4	4	14.7456	11796.48	368.64	0x05	0x08	11.52	288 to 290	PASS
3	3	6	4	14.7456	11796.48	368.64	0x05	0x08	11.52	292 to 294	PASS
4	2	2	2	14.7456	5898.24	368.64	0x05	0x07	23.04	270 to 274	PASS
5	4	4	2	14.7456	11796.48	368.64	0x05	0x07	23.04	232 to 234	PASS
6	1	2	3	14.7456	5898.24	368.64	0x05	0x0F	15.36	346 to 348	PASS
7	2	4	3	14.7456	11796.48	368.64	0x06	0x0F	15.36	282 to 284	PASS
8	1	4	8	14.7456	11796.48	368.64	0x05	0x28	5.76	406 to 408	PASS
9	4	2	1	14.7456	11796.48	368.64	0x05	0x07	46.08	196 to 197	PASS
10	4	2	2	14.7456	11796.48	368.64	0x05	0x07	23.04	192 to 193	PASS
11	8	2	1	14.7456	11796.48	368.64	0x05	0x06	46.08	173 to 174	PASS
12	8	2	2	14.7456	11796.48	368.64	0x05	0x08	23.04	170 to 172	PASS
13	8	2	3	14.7456	5898.24	368.64	0x05	0x0F	11.52	264 to 266	PASS
14	4	1	1	14.7456	2949.12	368.64	0x07	0x0	46.08	186 to 187	PASS
15	4	1	2	14.7456	2949.12	368.64	0x05	0x07	23.04	172 to 173	PASS
16	8	1	1	14.7456	5898.24	368.64	0x06	0x00	46.08	160 to 162	PASS
17	8	1	2	14.7456	5898.24	368.64	0x05	0x08	23.04	156 to 158	PASS
18	4	2	3	14.7456	11796.48	368.64	0x0B	0x0E	15.36	220 to 223	PASS

Figure 5. Sine Wave at DAC Analog Channel for LMF = 423 Configuration

This figure shows the sine wave output from the DAC analog channel for the LMF = 423 configuration.

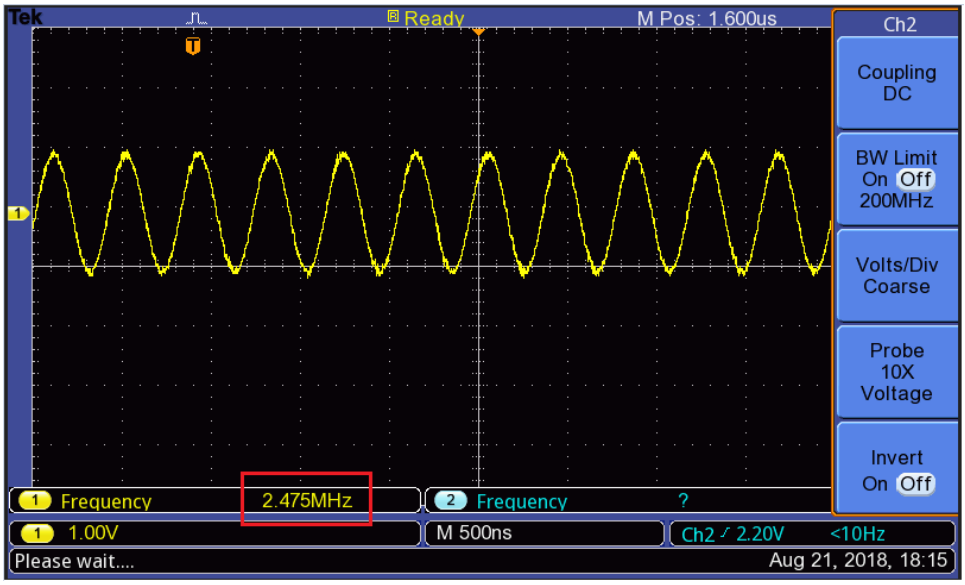
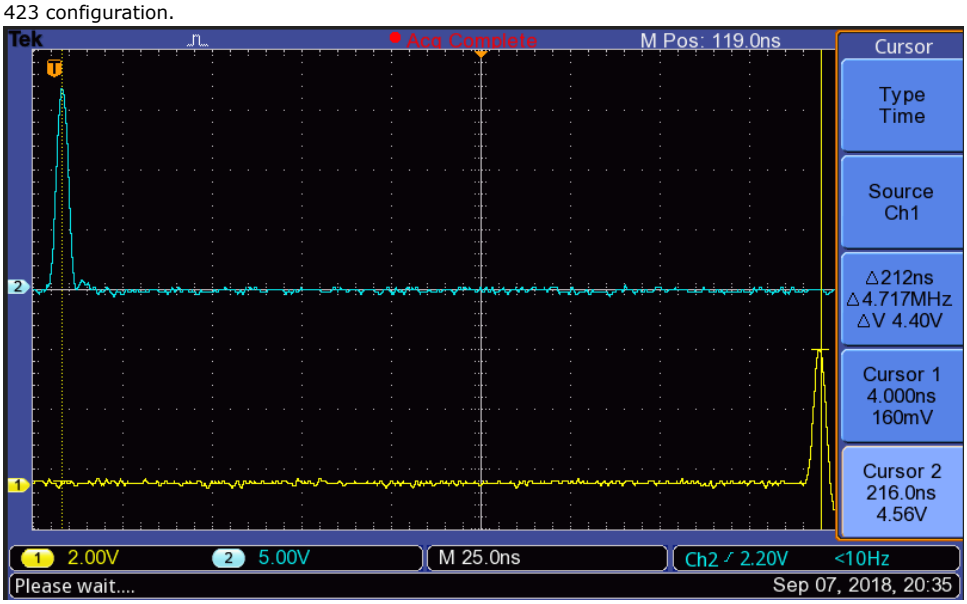


Figure 6. Deterministic Latency Measurement for LMF = 423 Configuration

This figure shows the time difference between pulses in the deterministic latency measurement for the LMF = 423 configuration.



1.6. Test Result Comments

In each test case, the TX JESD204B Intel FPGA IP successfully initializes from CGS phase, ILAS phase, and until user data phase. The behavior of the TX JESD204B Intel FPGA IP meets the passing criteria.

No data integrity issue is observed from the STPL test pattern checkers at the DAC JESD core for all the modes.

The sine wave is observed at the analog channels when the sine wave generators in the FPGA are enabled.

When the LMFCVar and LMFCDel registers at the DAC are not correctly configured, there are random STPL test failures. Hence, these registers are fine-tuned by reading the DYN_LINK_LATENCY_x register (DAC registers 0x302 and 0x303). By repeatedly power-cycling and reading the DYN_LINK_LATENCY_x register, the minimum and maximum delays across power cycles can be determined and used to calculate the LMFCVar and LMFCDel register values. For information on how to calculate these register values, refer to the AD9174 datasheet.

Setting the LMFCDel register appropriately ensures that all the corresponding data samples arrive in the same LMFC period. The LMFCVar value is then written into the receive buffer delay (RBD) register to absorb all link delay variations. This ensures that all data samples have arrived before reading. By setting the LMFCDel and LMFCVar registers to fixed values across runs and power cycles, deterministic latency is achieved.

In the deterministic latency test, deterministic latency variation of around 1 to 4 ns is observed. This variation might be attributed to the following:

- SYSREF sampling (according to the AD9174 datasheet, the amount of deterministic latency variation in subclass 1 is within ±4 DAC clock cycles at 12 GHz and ±2.5 DAC clock cycles at 6 GHz).
- Clock routing on the global clock tree in the FPGA. Potential variations are as follows:
  - I/O PLL f_{IN} variation
  - I/O PLL f_{OUT} variation
  - Clock tree variation

1.7. Document Revision History for AN 890: JESD204B Intel FPGA IP and ADI AD9174 Interoperability Report for Intel Stratix 10 L-Tile Devices

Document Version	Changes
2019.05.28	Initial release.

1.8. Appendix

Device Used and Quartus Tool Version

The Intel Stratix 10 1SX280LU2F50E2VGS3 device (transceiver speed grade -2 device) is used.

The Intel Quartus® Prime Pro Edition software version 18.1.0 Build 222 is used for compilation of designs.

Timing Closure Details

Synthesis/Fitter Settings:

The following Analysis/Fitter settings were added to the Quartus Settings File (**.qsf**) to close the timing requirements for some parameter configuration modes.

Compiler Setting	Value Used	Default Value
Optimization Technique	Speed	Balanced
Router Timing Optimization Level	Maximum	Normal
Auto Packed Registers	Normal	Auto
Physical Synthesis	ON	OFF
Restructure Multipliers	OFF	Auto

Known Issues/Warnings

In some parameter configuration modes, `sysref_in` is listed in the unconstrained paths. In addition, the warning "`sysref_in` was determined to be a clock but was found without an associated clock assignment" is encountered. This warning occurs because the clock measure module is used to measure the SYSREF frequency. The clock measure module measures the exact SYSREF frequency generated by the HMC7044 clock generator in the AD9174 EVM for the FPGA and DAC.

The HMC7044 clock generator in the AD9174 EVM and the PLL in the AD9174 device are used to generate the DAC sample rate (DAC sampling clock). The output clock generated by the HMC7044 clock generator is in multiples of 122.88 MHz. In addition, only the SPI_WRITE command is applicable to the HMC7044 registers while the SPI_READ command is not supported. Consequently, the lane rate is fixed to 14.7456 Gbps with a reference clock of 368.64 MHz (multiple of 122.88 MHz) and not 15 Gbps with a reference clock of 375 MHz.

These known issues/warnings do not have any material impact on the test results.