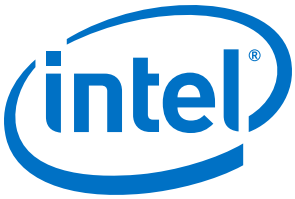


AN 832: Intel FPGA JESD204B IP Core and ADI AD9208 Hardware Checkout Report for Intel Stratix 10 Devices

AN-832 | 2018.05.24
Latest document on the web: PDF | HTML

Contents

1. Intel FPGA JESD204B IP Core and ADI AD9208 Hardware Checkout Report for Intel® Stratix® 10 Devices

The Intel FPGA JESD204B IP core is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204B IP core has been hardware-tested with a number of selected JESD204B-compliant ADC (analog-to-digital converter) devices.

This report highlights the interoperability of the JESD204B IP core with the AD9208 converter evaluation module (EVM) from Analog Devices Inc. (ADI). The following sections describe the hardware checkout methodology and test results.

Related Information

JESD204B IP Core User Guide

1.1. Hardware Requirements

The hardware checkout test requires the following hardware and software tools:

- Intel® Stratix® 10 GX H-Tile FPGA Development Kit (ES Edition) (1SG280HU1F50E1VGS1)
- ADI AD9208 EVM
- Micro-USB cable
- MMPX-to-SMA cables
- Clock source card capable of generating ADC sampling clock and FPGA device clock frequencies as listed in Table 6 on page 12.

  Note: In this application note, the Analog Devices ADF4355 clock source card is used. Review the clocking scheme with the clock source card manufacturer of your choice.

Related Information

Intel Stratix 10 GX FPGA Development Kit

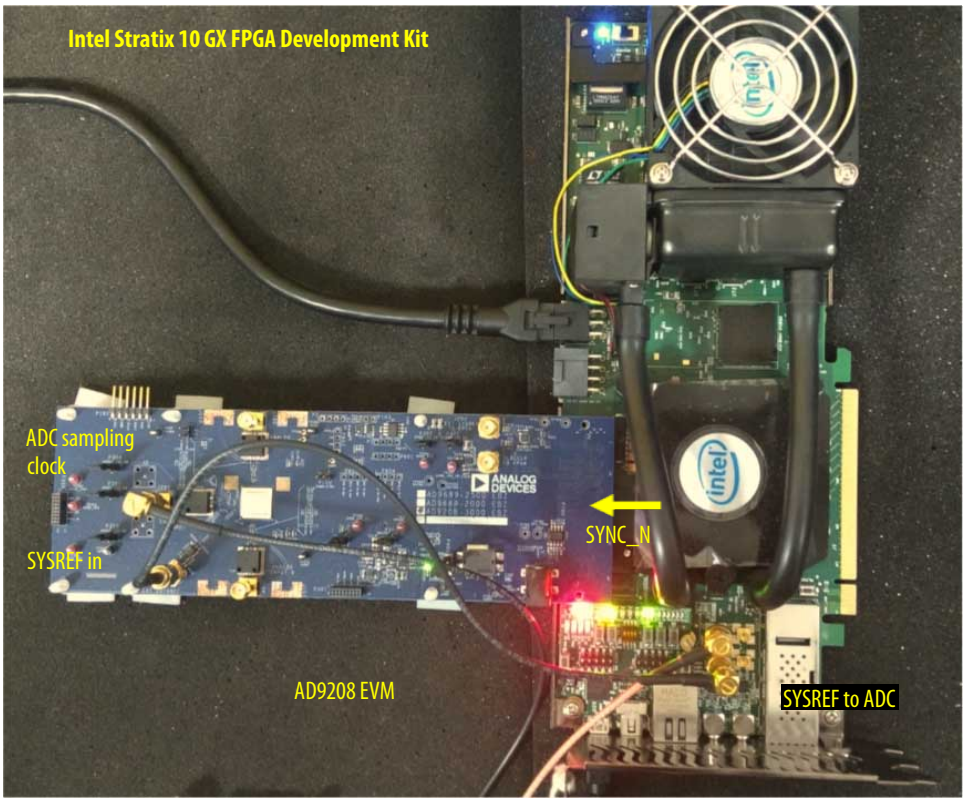
1.2. Hardware Setup

An Intel Stratix 10 GX H-Tile FPGA Development Kit (ES Edition) is used with the ADI AD9208 daughter card module installed to the development board's FMC connector.

- The AD9208 EVM derives power from FMC pins.
- The FPGA device clock is supplied by Si5341 and the sampling clock to the ADC AD9208 EVM is given by external clock source ADF4355.
- The ADF4355 derives reference clock from the FPGA fPLL. This fPLL derives the reference clock from the `device_clk` which is supplied by the Si5341 clock generator.
- For Subclass 1, the FPGA generates SYSREF for the JESD204B IP core as well as the AD9208 device.
- SYSREF is provided to the ADC through SMA connector.

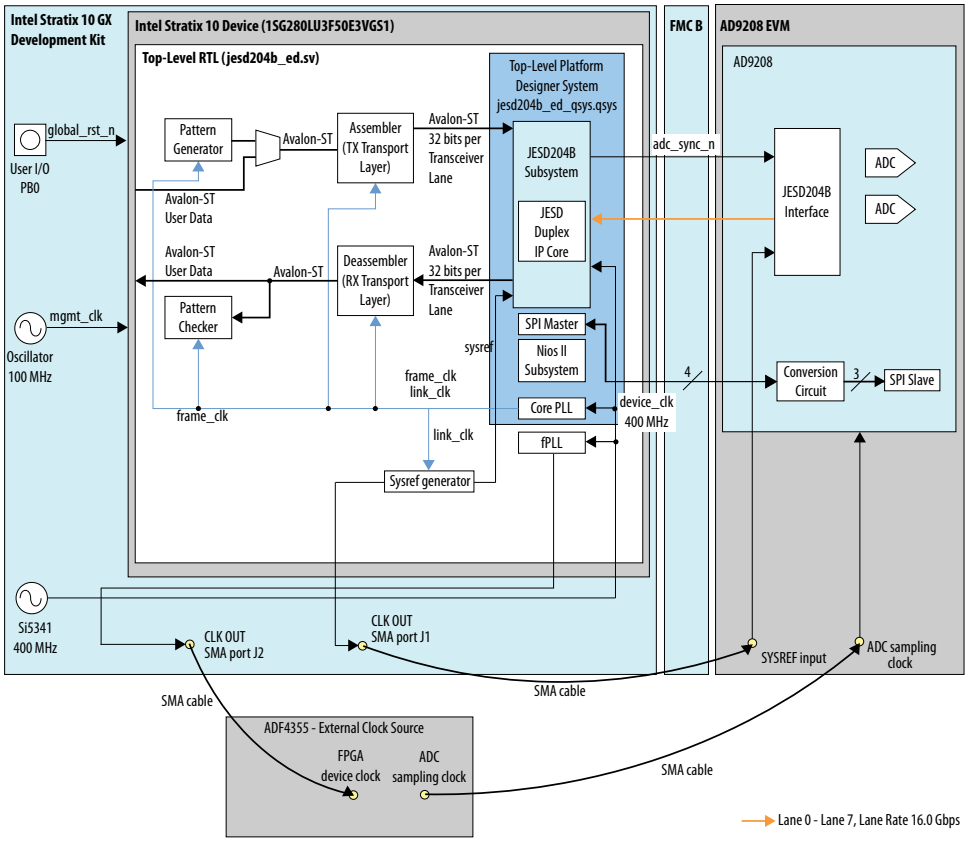
  Note: Intel recommends the SYSREF to be provided by the clock generator that sources the `device_clk` to FPGA and sampling clock to ADC.

Figure 1. Hardware Setup



The following system-level diagram shows how the different modules connect in this design.

Figure 2. System Diagram



In this setup, where LMF = 882, the data rate of transceiver lanes is 16.0 Gbps. An external clock source card provides 400 MHz clock to the FPGA and 1600 MHz sampling clock to AD9208 device. A periodic SYSREF is generated by the FPGA and provided to the ADC through the SMA connector. The JESD204B IP core is instantiated in Duplex mode but only the receiver path is used.

1.3. Hardware Checkout Methodology

The following section describes the test objectives, procedure, and the passing criteria. The test covers the following areas:

- Receiver data link layer
- Receiver transport layer
- Descrambling
- Deterministic latency (Subclass 1)

1.3.1. Receiver Data Link Layer

This test area covers the test cases for code group synchronization (CGS) and initial frame and lane synchronization (ILA).

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The Signal Tap Logic Analyzer tool monitors the receiver data link layer operation.

1.3.1.1. Code Group Synchronization (CGS)

Table 1. CGS Test Cases

Test Case	Objective	Description	Passing Criteria
CGS.1	Check whether sync request is deasserted after correct reception of four successive /K/ characters.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_rx_pcs_data[(L*32)-1:0] • jesd204_rx_pcs_data_valid[L-1:0] • jesd204_rx_pcs_kchar_data[(L*4)-1:0] (1) The following signals in <*ip_variant_name*>.v are tapped: • rx_dev_sync_n • jesd204_rx_int The rxlink_clk is used as the sampling clock for the Signal Tap. Each lane is represented by 32-bit data bus in jesd204_rx_pcs_data signal. The 32-bit data bus for is divided into 4 octets.	• /K/ character or K28.5 (0xBC) is observed at each octet of the jesd204_rx_pcs_data bus. • The jesd204_rx_pcs_data_valid signal is asserted to indicate data from the PCS is valid. • The jesd204_rx_pcs_kchar_data signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ characters are observed. • The rx_dev_sync_n signal is deasserted after correct reception of at least four successive /K/ characters. • The jesd204_rx_int signal is deasserted if there is no error.
CGS.2	Check full CGS at the receiver after correct reception of another four 8B/10B characters.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_rx_pcs_errdetect[(L*4)-1:0] • jesd204_rx_pcs_disperr[(L*4)-1:0] (1) The following signals in <*ip_variant_name*>.v are tapped: • jesd204_rx_int The rxlink_clk is used as the sampling clock for the Signal Tap.	The jesd204_rx_pcs_errdetect, jesd204_rx_pcs_disperr, and jesd204_rx_int signals should not be asserted during CGS phase.

(1) L is the number of lanes.

1.3.1.2. Initial Frame and Lane Synchronization (ILA)

Table 2. Initial Frame and Lane Synchronization Test Cases

Test Case	Objective	Description	Passing Criteria
ILA.1	Check whether the initial frame synchronization state machine enters FS_DATA state upon receiving non /K/ characters.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_rx_pcs_data[(L*32)-1:0] • jesd204_rx_pcs_data_valid[L-1:0] • jesd204_rx_pcs_kchar_data[(L*4)-1:0] (2) The following signals in <*ip_variant_name*>.v are tapped: • rx_dev_sync_n • jesd204_rx_int The rxlink_clk is used as the sampling clock for the Signal Tap. Each lane is represented by 32-bit data bus in jesd204_rx_pcs_data. The 32-bit data bus for is divided into 4 octets.	• /R/ character or K28.0 (0x1C) is observed after /K/ character at the jesd204_rx_pcs_data bus. • The jesd204_rx_pcs_data_valid signal must be asserted to indicate that data from the PCS is valid. • The rx_dev_sync_n and jesd204_rx_int signals are deasserted. • Each multiframe in ILAS phase ends with /A/ character or K28.3 (0x7C). • The jesd204_rx_pcs_kchar_data signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ characters are observed.
ILA.2	Check the JESD204B configuration parameters from ADC in second multiframe.	The following signals in <*ip_variant_name*>_inst_phy.v are tapped: • jesd204_rx_pcs_data[(L*32)-1:0] • jesd204_rx_pcs_data_valid[L-1:0] (2) The following signal in <*ip_variant_name*>.v is tapped: • jesd204_rx_int The rxlink_clk is used as the sampling clock for the Signal Tap. The system console accesses the following registers: • ilas_octet0 • ilas_octet1 • ilas_octet2 • ilas_octet3	• /R/ character is followed by /Q/ character or K28.4 (0x9C) at the beginning of second multiframe. • The jesd204_rx_int is deasserted if there is no error. • Octets 0-13 read from these registers match with the JESD204B parameters in each test setup.

continued...

(2) L is the number of lanes.

Test Case	Objective	Description	Passing Criteria
		The content of 14 configuration octets in second multiframe is stored in these 32-bit registers — `ilas_octet0`, `ilas_octet1`, `ilas_octet2`, and `ilas_octet3`.	
ILA.3	Check the lane alignment	The following signals in *<ip_variant_name>*`_inst_phy.v` are tapped: • `jesd204_rx_pcs_data[(L*32)-1:0]` • `jesd204_rx_pcs_data_valid[L-1:0]` (2) The following signals in *<ip_variant_name>*`.v` are tapped: • `rx_somf[3:0]` • `dev_lane_aligned` • `jesd204_rx_int` The `rxlink_clk` is used as the sampling clock for the Signal Tap.	• The `dev_lane_aligned` is asserted upon the last /A/ character of the ILAS is received, which is followed by the first data octet. • The `rx_somf` marks the start of multiframe in user data phase. • The `jesd204_rx_int` is deasserted if there is no error.

1.3.2. Receiver Transport Layer

To check the data integrity of the payload data stream through the JESD204B receiver IP Core and transport layer, the ADC is configured to output PRBS-9 and Ramp test data pattern. The ADC is also set to operate with the same configuration as set in the JESD204B IP Core. The PRBS checker/Ramp checker in the FPGA fabric checks data integrity for one minute.

This figure shows the conceptual test setup for data integrity checking.

Figure 3. Data Integrity Check Using PRBS/Ramp Checker

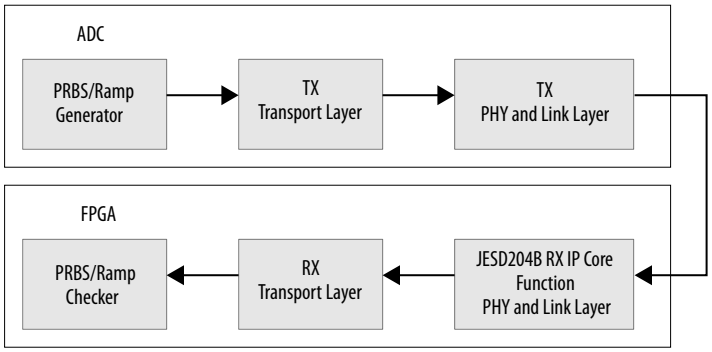


Table 3. Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
TL.1	Check the transport layer mapping using Ramp test pattern.	The following signals in `altera_jesd204_transport_rx_top.sv` are tapped: • `jesd204_rx_data_valid`	• The `jesd204_rx_data_valid` signal is asserted. • The `data_error` and `jesd204_rx_int` signals are deasserted.

continued...

Test Case	Objective	Description	Passing Criteria
		The following signals in `jesd204b_ed.sv` are tapped: • `data_error` • `jesd204_rx_int` The `rxframe_clk` is used as the sampling clock for the Signal Tap. The `data_error` signal indicates a pass or fail for the PRBS checker.	
TL.2	Check the transport layer mapping using PRBS-9 test pattern.	The following signals in `altera_jesd204_transport_rx_top.sv` are tapped: • `jesd204_rx_data_valid` The following signals in `jesd204b_ed.sv` are tapped: • `data_error` • `jesd204_rx_int` The `rxframe_clk` is used as the sampling clock for the Signal Tap. The `data_error` signal indicates a pass or fail for the PRBS checker.	• The `jesd204_rx_data_valid` signal is asserted. • The `data_error` and `jesd204_rx_int` signals are deasserted.

1.3.3. Descrambling

The PRBS/Ramp checker at the receiver transport layer checks the data integrity of descrambler.

The Signal Tap Logic Analyzer tool monitors the operation of the receiver transport layer.

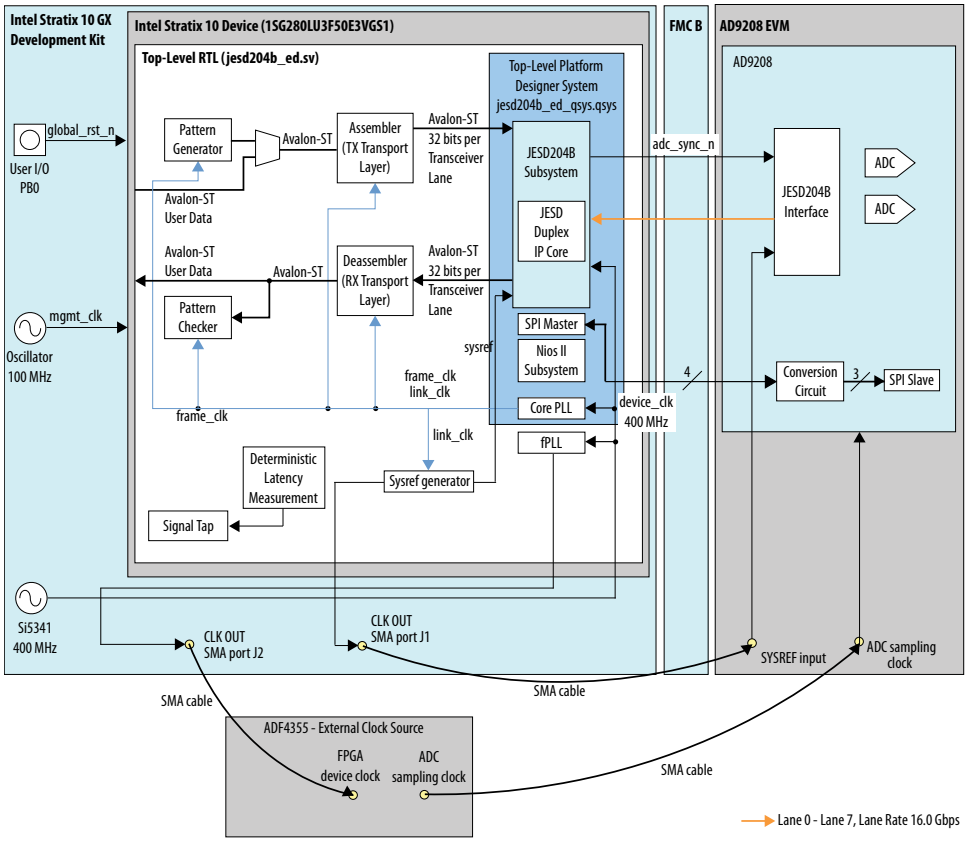
Table 4. Descrambler Test Cases

Test Case	Objective	Description	Passing Criteria
SCR.1	Check the functionality of the descrambler using Ramp test pattern.	Enable scrambler at the ADC and descrambler at the JESD204B receiver IP Core. The signals that are tapped in this test case are similar to test case TL.1	• The `jesd204_rx_data_valid` signal is asserted. • The `data_error` and `jesd204_rx_int` signals are deasserted.
SCR.2	Check the functionality of the descrambler using PRBS-9 test pattern.	Enable scrambler at the ADC and descrambler at the JESD204B receiver IP Core. The signals that are tapped in this test case are similar to test case TL.2	• The `jesd204_rx_data_valid` signal is asserted. • The `data_error` and `jesd204_rx_int` signals are deasserted.

1.3.4. Deterministic Latency (Subclass 1)

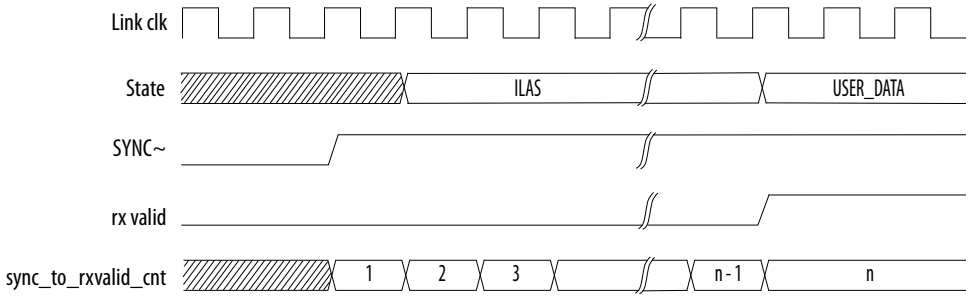
The figure below shows the block diagram of deterministic latency test setup. A SYSREF generator in the FPGA provides a periodic SYSREF pulse for both the AD9208 and JESD204B IP Core. The SYSREF generator is running in the link clock domain and the period of SYSREF pulse is configured to the desired multiframe size. The SYSREF pulse restarts the LMF counter and realigns it to the LMFC boundary.

Figure 4. Deterministic Latency Test Setup Block Diagram



The deterministic latency measurement block checks deterministic latency by measuring the number of link clock counts between the start of de-assertion of SYNC~ to the first user data output.

Figure 5. Deterministic Latency Measurement Timing Diagram



With the setup above, four test cases were defined to prove deterministic latency. The JESD204B IP Core does continuous SYSREF detection. The SYSREF N-shot mode is enabled on the AD9208 for this deterministic latency measurement.

Table 5. Deterministic Latency Test Cases

Test Case	Objective	Description	Passing Criteria
DL.1	Check the FPGA SYSREF single detection.	Check that the FPGA detects the first rising edge of SYSREF pulse. Read the status of `sysref_singledet (bit[2])` identifier in `syncn_sysref_ctrl` register at address 0x54. Read the status of `csr_sysref_lmfc_ err (bit[1])` identifier in the `rx_err0` register at address 0x60.	The value of `sysref_singledet` identifier should be zero. The value of `csr_sysref_lmfc_err` identifier should be zero.
DL.2	Check the SYSREF capture.	Check that FPGA and ADC capture SYSREF correctly and restart the LMF counter. Both FPGA and ADC are also repetitively reset. Read the value of `rbd_count (bit[10:3])` identifier in `rx_status0` register at address 0x80.	If the SYSREF is captured correctly and the LMF counter restarts, for every reset, the `rbd_count` value should only drift within 1-2 link clocks due to word alignment.
DL.3	Check the latency from start of SYNC~ deassertion to first user data output.	Check that the latency is fixed for every FPGA and ADC reset and power cycle. Record the number of link clocks count from the start of SYNC~ deassertion to the first user data output, which is the assertion of `jesd204_rx_link_valid` signal. The deterministic latency measurement block in Figure 4 on page 10 has a counter to measure the link clock count.	Consistent latency from the start of SYNC~ deassertion to the assertion of `jesd204_rx_link_valid` signal.
DL.4	Check the data latency during user data phase.	Check that the data latency is fixed during user data phase. Observe the ramp pattern from the Signal Tap Logic Analyzer.	The ramp pattern should be in perfect shape with no distortion.

1.4. JESD204B IP Core and ADC Configurations

The JESD204B IP Core parameters (L, M, and F) in this hardware checkout are natively supported by the AD9208 device's quick configuration register at address 0x570. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the AD9208 operating conditions.

The hardware checkout testing implements the JESD204B IP Core with the following parameter configuration.

Global setting for all configuration:

- N' = 16
- CS = 0
- CF = 0

- Subclass = 1
- FPGA Management Clock (MHz) = 100
- Character Replacement = Enabled
- PCS Option = Soft PCS

Table 6. Parameter Configuration

LMF	HD	S	N	ADC Sampling Clock (MHz)	FPGA Device Clock (MHz) (3)	FPGA Link Clock (MHz) (4)	FPGA Frame Clock (MHz) (4)	Lane Rate (Gbps)	DDC Enabled	Decimation Factor	Data Pattern	
112	0	1	14	800	400	400	400	16.0	No	1	PRBS-9	Ramp
114	0	2	14	800	400	400	400	16.0	No	1	PRBS-9	Ramp
211	1	1	14	1600	400	400	400	16.0	No	1	PRBS-9	Ramp
212	0	2	14	1600	400	400	400	16.0	No	1	PRBS-9	Ramp
411	1	2	14	3000	375	375	375	15.0	No	1	PRBS-9	Ramp
412	0	4	14	3000	375	375	375	15.0	No	1	PRBS-9	Ramp
811	1	4	14	3000	187.5	187.5	187.5	7.5	No	1	PRBS-9	Ramp
812	0	8	14	3000	187.5	187.5	187.5	7.5	No	1	PRBS-9	Ramp
124	0	1	14	400	400	400	400	16.0	No	1	PRBS-9	Ramp
128	0	2	14	400	400	400	200	16.0	No	1	PRBS-9	Ramp
222	0	1	14	800	400	400	400	16.0	No	1	PRBS-9	Ramp
224	0	2	14	800	400	400	400	16.0	No	1	PRBS-9	Ramp
421	1	1	14	1600	400	400	400	16.0	No	1	PRBS-9	Ramp
422	0	2	14	1600	400	400	400	16.0	No	1	PRBS-9	Ramp
821	1	2	14	3000	375	375	375	15.0	No	1	PRBS-9	Ramp
822	0	4	14	3000	375	375	375	15.0	No	1	PRBS-9	Ramp
148	0	1	16	400	400	400	200	16.0	Yes	2	PRBS-9	Ramp
244	0	1	16	800	400	400	400	16.0	Yes	2	PRBS-9	Ramp
248	0	2	16	800	400	400	200	16.0	Yes	2	PRBS-9	Ramp
442	0	1	16	1600	400	400	400	16.0	Yes	2	PRBS-9	Ramp
444	0	2	16	1600	400	400	400	16.0	Yes	2	PRBS-9	Ramp
841	1	1	16	3000	375	375	400	15.0	Yes	2	PRBS-9	Ramp
842	0	2	16	3000	375	375	400	15.0	Yes	2	PRBS-9	Ramp
288	0	1	16	400	400	400	200	16.0	Yes	2	PRBS-9	Ramp
484	0	1	16	800	400	400	400	16.0	Yes	2	PRBS-9	Ramp

continued...

(3) The device clock is used to clock the transceiver.

(4) The frame clock and link clock are derived from the device clock using an internal PLL.

LMF	HD	S	N	ADC Sampling Clock (MHz)	FPGA Device Clock (MHz) (3)	FPGA Link Clock (MHz) (4)	FPGA Frame Clock (MHz) (4)	Lane Rate (Gbps)	DDC Enabled	Decimation Factor	Data Pattern	
488	0	2	16	800	400	400	200	16.0	Yes	2	PRBS-9	Ramp
882	0	1	16	1600	400	400	400	16.0	Yes	2	PRBS-9	Ramp
884	0	2	16	1600	400	400	400	16.0	Yes	2	PRBS-9	Ramp

1.5. Test Results

The following table contains the possible results and their definition.

Table 7. Results Definition

Result	Definition
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with comments	The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Refer to comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, TL.2, SCR.1, and SCR.2 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

Table 8. Results for Test Cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, TL.2, SCR.1, and SCR.2

Test	L	M	F	SCR	K	Data rate (Gbps)	ADC Sampling Clock (MHz)	Link Clock (MHz)	Result
1	1	1	2	0	32	16.0	800	400	PASS
2	1	1	2	1	32	16.0	800	400	PASS
3	1	1	2	0	16	16.0	800	400	PASS
4	1	1	2	1	16	16.0	800	400	PASS
5	1	1	4	0	32	16.0	800	400	PASS
6	1	1	4	1	32	16.0	800	400	PASS
7	1	1	4	0	16	16.0	800	400	PASS
8	1	1	4	1	16	16.0	800	400	PASS

continued...

(3) The device clock is used to clock the transceiver.

(4) The frame clock and link clock are derived from the device clock using an internal PLL.

Test	L	M	F	SCR	K	Data rate (Gbps)	ADC Sampling Clock (MHz)	Link Clock (MHz)	Result
9	2	1	1	0	32	16.0	1600	400	PASS
10	2	1	1	1	32	16.0	1600	400	PASS
11	2	1	1	0	20	16.0	1600	400	PASS
12	2	1	1	1	20	16.0	1600	400	PASS
13	2	1	2	0	32	16.0	1600	400	PASS
14	2	1	2	1	32	16.0	1600	400	PASS
15	2	1	2	0	16	16.0	1600	400	PASS
16	2	1	2	1	16	16.0	1600	400	PASS
17	4	1	1	0	32	15.0	3000	375	PASS
18	4	1	1	1	32	15.0	3000	375	PASS
19	4	1	1	0	20	15.0	3000	375	PASS
20	4	1	1	1	20	15.0	3000	375	PASS
21	4	1	2	0	32	15.0	3000	375	PASS
22	4	1	2	1	32	15.0	3000	375	PASS
23	4	1	2	0	16	15.0	3000	375	PASS
24	4	1	2	1	16	15.0	3000	375	PASS
25	8	1	1	0	32	7.5	3000	187.5	PASS
26	8	1	1	1	32	7.5	3000	187.5	PASS
27	8	1	1	0	20	7.5	3000	187.5	PASS
28	8	1	1	1	20	7.5	3000	187.5	PASS
29	8	1	2	0	32	7.5	3000	187.5	PASS
30	8	1	2	1	32	7.5	3000	187.5	PASS
31	8	1	2	0	16	7.5	3000	187.5	PASS
32	8	1	2	1	16	7.5	3000	187.5	PASS
33	1	2	4	0	32	16.0	400	400	PASS
34	1	2	4	1	32	16.0	400	400	PASS
35	1	2	4	0	16	16.0	400	400	PASS
36	1	2	4	1	16	16.0	400	400	PASS
37	1	2	8	0	32	16.0	400	400	PASS
38	1	2	8	1	32	16.0	400	400	PASS
39	1	2	8	0	16	16.0	400	400	PASS
40	1	2	8	1	16	16.0	400	400	PASS
41	2	2	2	0	32	16.0	800	400	PASS
42	2	2	2	1	32	16.0	800	400	PASS
43	2	2	2	0	16	16.0	800	400	PASS

continued...

Test	L	M	F	SCR	K	Data rate (Gbps)	ADC Sampling Clock (MHz)	Link Clock (MHz)	Result
44	2	2	2	1	16	16.0	800	400	PASS
45	2	2	4	0	32	16.0	800	400	PASS
46	2	2	4	1	32	16.0	800	400	PASS
47	2	2	4	0	16	16.0	800	400	PASS
48	2	2	4	1	16	16.0	800	400	PASS
49	4	2	1	0	32	16.0	1600	400	PASS
50	4	2	1	1	32	16.0	1600	400	PASS
51	4	2	1	0	20	16.0	1600	400	PASS
52	4	2	1	1	20	16.0	1600	400	PASS
53	4	2	2	0	32	16.0	1600	400	PASS
54	4	2	2	1	32	16.0	1600	400	PASS
55	4	2	2	0	16	16.0	1600	400	PASS
56	4	2	2	1	16	16.0	1600	400	PASS
57	8	2	1	0	32	15.0	3000	375	PASS
58	8	2	1	1	32	15.0	3000	375	PASS
59	8	2	1	0	20	15.0	3000	375	PASS
60	8	2	1	1	20	15.0	3000	375	PASS
61	8	2	2	0	32	15.0	3000	375	PASS
62	8	2	2	1	32	15.0	3000	375	PASS
63	8	2	2	0	16	15.0	3000	375	PASS
64	8	2	2	1	16	15.0	3000	375	PASS
65	1	4	8	0	32	16.0	400	400	PASS
66	1	4	8	1	32	16.0	400	400	PASS
67	1	4	8	0	16	16.0	400	400	PASS
68	1	4	8	1	16	16.0	400	400	PASS
69	2	4	4	0	32	16.0	800	400	PASS
70	2	4	4	1	32	16.0	800	400	PASS
71	2	4	4	0	16	16.0	800	400	PASS
72	2	4	4	1	16	16.0	800	400	PASS
73	2	4	8	0	32	16.0	800	400	PASS
74	2	4	8	1	32	16.0	800	400	PASS
75	2	4	8	0	16	16.0	800	400	PASS
76	2	4	8	1	16	16.0	800	400	PASS
77	4	4	2	0	32	16.0	1600	400	PASS
78	4	4	2	1	32	16.0	1600	400	PASS

continued...

Test	L	M	F	SCR	K	Data rate (Gbps)	ADC Sampling Clock (MHz)	Link Clock (MHz)	Result
79	4	4	2	0	16	16.0	1600	400	PASS
80	4	4	2	1	16	16.0	1600	400	PASS
81	4	4	4	0	32	16.0	1600	400	PASS
82	4	4	4	1	32	16.0	1600	400	PASS
83	4	4	4	0	16	16.0	1600	400	PASS
84	4	4	4	1	16	16.0	1600	400	PASS
85	8	4	1	0	32	15.0	3000	375	PASS
86	8	4	1	1	32	15.0	3000	375	PASS
87	8	4	1	0	20	15.0	3000	375	PASS
88	8	4	1	1	20	15.0	3000	375	PASS
89	8	4	2	0	32	15.0	3000	375	PASS
90	8	4	2	1	32	15.0	3000	375	PASS
91	8	4	2	0	16	15.0	3000	375	PASS
92	8	4	2	1	16	15.0	3000	375	PASS
93	2	8	8	0	32	16.0	400	400	PASS
94	2	8	8	1	32	16.0	400	400	PASS
95	2	8	8	0	16	16.0	400	400	PASS
96	2	8	8	1	16	16.0	400	400	PASS
97	4	8	4	0	32	16.0	800	400	PASS
98	4	8	4	1	32	16.0	800	400	PASS
99	4	8	4	0	16	16.0	800	400	PASS
100	4	8	4	1	16	16.0	800	400	PASS
101	4	8	8	0	32	16.0	800	400	PASS
102	4	8	8	1	32	16.0	800	400	PASS
103	4	8	8	0	16	16.0	800	400	PASS
104	4	8	8	1	16	16.0	800	400	PASS
105	8	8	2	0	32	16.0	1600	400	PASS
106	8	8	2	1	32	16.0	1600	400	PASS
107	8	8	2	0	16	16.0	1600	400	PASS
108	8	8	2	1	16	16.0	1600	400	PASS
109	8	8	4	0	32	16.0	1600	400	PASS
110	8	8	4	1	32	16.0	1600	400	PASS
111	8	8	4	0	16	16.0	1600	400	PASS
112	8	8	4	1	16	16.0	1600	400	PASS

The following table shows the results for test cases DL.1, DL.2, DL.3, and DL.4 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

Table 9. Results for Deterministic Latency Test

Test	L	M	F	Subclass	K	Data rate (Gbps)	Sampling Clock(MHz)	Link Clock (MHz)	Result	Latency (Link Clock Cycles)
DL.1	1	1	2	1	16/32	16.0	800	400	PASS	75 (K=16) 115 (K=32)
DL.2	1	1	2	1	16/32	16.0	800	400	PASS	
DL.3	1	1	2	1	16/32	16.0	800	400	PASS	
DL.4	1	1	2	1	16/32	16.0	800	400	PASS	
DL.1	1	1	4	1	16/32	16.0	800	400	PASS	115 (K=16) 193 (K=32)
DL.2	1	1	4	1	16/32	16.0	800	400	PASS	
DL.3	1	1	4	1	16/32	16.0	800	400	PASS	
DL.4	1	1	4	1	16/32	16.0	800	400	PASS	
DL.1	2	1	1	1	20/32	16.0	1600	400	PASS	63 (K=20) 83 (K=32)
DL.2	2	1	1	1	20/32	16.0	1600	400	PASS	
DL.3	2	1	1	1	20/32	16.0	1600	400	PASS	
DL.4	2	1	1	1	20/32	16.0	1600	400	PASS	
DL.1	2	1	2	1	16/32	16.0	1600	400	PASS	83 (K=16) 115 (K=32)
DL.2	2	1	2	1	16/32	16.0	1600	400	PASS	
DL.3	2	1	2	1	16/32	16.0	1600	400	PASS	
DL.4	2	1	2	1	16/32	16.0	1600	400	PASS	
DL.1	4	1	1	1	20/32	15.0	3000	375	PASS	58 (K=20) 75 (K=32)
DL.2	4	1	1	1	20/32	15.0	3000	375	PASS	
DL.3	4	1	1	1	20/32	15.0	3000	375	PASS	
DL.4	4	1	1	1	20/32	15.0	3000	375	PASS	
DL.1	4	1	2	1	16/32	15.0	3000	375	PASS	75 (K=16) 115 (K=32, SCR=1) 116 (K=32, SCR=0)
DL.2	4	1	2	1	16/32	15.0	3000	375	PASS	
DL.3	4	1	2	1	16/32	15.0	3000	375	PASS	
DL.4	4	1	2	1	16/32	15.0	3000	375	PASS	
DL.1	8	1	1	1	20/32	7.5	3000	187.5	PASS	58 (K=20) 69 (K=32)
DL.2	8	1	1	1	20/32	7.5	3000	187.5	PASS	
DL.3	8	1	1	1	20/32	7.5	3000	187.5	PASS	
DL.4	8	1	1	1	20/32	7.5	3000	187.5	PASS	
DL.1	8	1	2	1	16/32	7.5	3000	187.5	PASS	68 (K=16) 100 (K=32)
DL.2	8	1	2	1	16/32	7.5	3000	187.5	PASS	
DL.3	8	1	2	1	16/32	7.5	3000	187.5	PASS	
DL.4	8	1	2	1	16/32	7.5	3000	187.5	PASS	

continued...

Test	L	M	F	Subclass	K	Data rate (Gbps)	Sampling Clock(MHz)	Link Clock (MHz)	Result	Latency (Link Clock Cycles)
DL.1	1	2	4	1	16/32	16.0	400	400	PASS	115 (K=16) 195 (K=32)
DL.2	1	2	4	1	16/32	16.0	400	400	PASS	
DL.3	1	2	4	1	16/32	16.0	400	400	PASS	
DL.4	1	2	4	1	16/32	16.0	400	400	PASS	
DL.1	1	2	8	1	16/32	16.0	400	400	PASS	195 (K=16) 323 (K=32)
DL.2	1	2	8	1	16/32	16.0	400	400	PASS	
DL.3	1	2	8	1	16/32	16.0	400	400	PASS	
DL.4	1	2	8	1	16/32	16.0	400	400	PASS	
DL.1	2	2	2	1	16/32	16.0	800	400	PASS	76 (K=16) 114 (K=32)
DL.2	2	2	2	1	16/32	16.0	800	400	PASS	
DL.3	2	2	2	1	16/32	16.0	800	400	PASS	
DL.4	2	2	2	1	16/32	16.0	800	400	PASS	
DL.1	2	2	4	1	16/32	16.0	800	400	PASS	115 (K=16) 195 (K=32)
DL.2	2	2	4	1	16/32	16.0	800	400	PASS	
DL.3	2	2	4	1	16/32	16.0	800	400	PASS	
DL.4	2	2	4	1	16/32	16.0	800	400	PASS	
DL.1	4	2	1	1	20/32	16.0	1600	400	PASS	64 (K=20) 52 (K=32)
DL.2	4	2	1	1	20/32	16.0	1600	400	PASS	
DL.3	4	2	1	1	20/32	16.0	1600	400	PASS	
DL.4	4	2	1	1	20/32	16.0	1600	400	PASS	
DL.1	4	2	2	1	16/32	16.0	1600	400	PASS	82 (K=16) 115 (K=32)
DL.2	4	2	2	1	16/32	16.0	1600	400	PASS	
DL.3	4	2	2	1	16/32	16.0	1600	400	PASS	
DL.4	4	2	2	1	16/32	16.0	1600	400	PASS	
DL.1	8	2	1	1	20/32	15.0	3000	375	PASS	58 (K=20) 75 (K=32)
DL.2	8	2	1	1	20/32	15.0	3000	375	PASS	
DL.3	8	2	1	1	20/32	15.0	3000	375	PASS	
DL.4	8	2	1	1	20/32	15.0	3000	375	PASS	
DL.1	8	2	2	1	16/32	15.0	3000	375	PASS	75 (K=16) 115 (K=32)
DL.2	8	2	2	1	16/32	15.0	3000	375	PASS	
DL.3	8	2	2	1	16/32	15.0	3000	375	PASS	
DL.4	8	2	2	1	16/32	15.0	3000	375	PASS	
DL.1	1	4	8	1	16/32	16.0	400	400	PASS	227 (K=16) 387 (K=32)
DL.2	1	4	8	1	16/32	16.0	400	400	PASS	
DL.3	1	4	8	1	16/32	16.0	400	400	PASS	

continued...

Test	L	M	F	Subclass	K	Data rate (Gbps)	Sampling Clock(MHz)	Link Clock (MHz)	Result	Latency (Link Clock Cycles)
DL.4	1	4	8	1	16/32	16.0	400	400	PASS	
DL.1	2	4	4	1	16/32	16.0	800	400	PASS	130 (K=16) 195 (K=32)
DL.2	2	4	4	1	16/32	16.0	800	400	PASS	
DL.3	2	4	4	1	16/32	16.0	800	400	PASS	
DL.4	2	4	4	1	16/32	16.0	800	400	PASS	
DL.1	2	4	8	1	16/32	16.0	800	400	PASS	195 (K=16) 323 (K=32)
DL.2	2	4	8	1	16/32	16.0	800	400	PASS	
DL.3	2	4	8	1	16/32	16.0	800	400	PASS	
DL.4	2	4	8	1	16/32	16.0	800	400	PASS	
DL.1	4	4	2	1	16/32	16.0	1600	400	PASS	83 (K=16) 115 (K=32)
DL.2	4	4	2	1	16/32	16.0	1600	400	PASS	
DL.3	4	4	2	1	16/32	16.0	1600	400	PASS	
DL.4	4	4	2	1	16/32	16.0	1600	400	PASS	
DL.1	4	4	4	1	16/32	16.0	1600	400	PASS	115 (K=16) 195 (K=32)
DL.2	4	4	4	1	16/32	16.0	1600	400	PASS	
DL.3	4	4	4	1	16/32	16.0	1600	400	PASS	
DL.4	4	4	4	1	16/32	16.0	1600	400	PASS	
DL.1	8	4	1	1	20/32	15.0	3000	375	PASS	58 (K=20) 75 (K=32)
DL.2	8	4	1	1	20/32	15.0	3000	375	PASS	
DL.3	8	4	1	1	20/32	15.0	3000	375	PASS	
DL.4	8	4	1	1	20/32	15.0	3000	375	PASS	
DL.1	8	4	2	1	16/32	15.0	3000	375	PASS	75 (K=16) 115 (K=32)
DL.2	8	4	2	1	16/32	15.0	3000	375	PASS	
DL.3	8	4	2	1	16/32	15.0	3000	375	PASS	
DL.4	8	4	2	1	16/32	15.0	3000	375	PASS	
DL.1	2	8	8	1	16/32	16.0	400	400	PASS	226 (K=16) 386 (K=32)
DL.2	2	8	8	1	16/32	16.0	400	400	PASS	
DL.3	2	8	8	1	16/32	16.0	400	400	PASS	
DL.4	2	8	8	1	16/32	16.0	400	400	PASS	
DL.1	4	8	4	1	16/32	16.0	800	400	PASS	130 (K=16) 195 (K=32)
DL.2	4	8	4	1	16/32	16.0	800	400	PASS	
DL.3	4	8	4	1	16/32	16.0	800	400	PASS	
DL.4	4	8	4	1	16/32	16.0	800	400	PASS	
DL.1	4	8	8	1	16/32	16.0	800	400	PASS	195 (K=16) 323 (K=32)
DL.2	4	8	8	1	16/32	16.0	800	400	PASS	

continued...

Test	L	M	F	Subclass	K	Data rate (Gbps)	Sampling Clock(MHz)	Link Clock (MHz)	Result	Latency (Link Clock Cycles)
DL.3	4	8	8	1	16/32	16.0	800	400	PASS	
DL.4	4	8	8	1	16/32	16.0	800	400	PASS	
DL.1	8	8	2	1	16/32	16.0	1600	400	PASS	115 (K=32) 77 (K=16)
DL.2	8	8	2	1	16/32	16.0	1600	400	PASS	
DL.3	8	8	2	1	16/32	16.0	1600	400	PASS	
DL.4	8	8	2	1	16/32	16.0	1600	400	PASS	
DL.1	8	8	4	1	16/32	16.0	1600	400	PASS	195 (K=32) 115 (K=16)
DL.2	8	8	4	1	16/32	16.0	1600	400	PASS	
DL.3	8	8	4	1	16/32	16.0	1600	400	PASS	
DL.4	8	8	4	1	16/32	16.0	1600	400	PASS	

The following figure shows the Signal Tap waveform of the link latency count from the deassertion of SYNC~ to the assertion of the `jesd204_rx_link_valid` signal. The link latency count (in link clock cycles) measures the first user data output latency.

Figure 6. Deterministic Latency Measurement Ramp Test Pattern Diagram

1.6. Test Result Comments

In each test case, the JESD204B receiver IP core successfully initialize from CGS phase, ILA phase, and until user data phase.

No data integrity issue is observed by the PRBS and Ramp checker for all JESD configurations.

In the deterministic latency measurement, consistent total latency is observed across multiple power cycles or resets.

For a few JESD configurations, to avoid lane de-skew error or achieve deterministic latency on FPGA, RBD offset/lmfc offset register needs to be programmed. The modes and the corresponding values used are tabled below.

Mode (LMF)	csr_rbd_offset (syncn_sysref_ctrl [10:3])	csr_lmfc_offset (syncn_sysref_ctrl [19:12])
114-K32	0x2	—
222-K16	0x7	—
222-K32	0x1	—
244-K16	0x1	—
288-K16	0x1	0x1
288-K32	0x1	—
412-K32	0xF	—
421-K20	—	0x1
421-K32	0x1	—
422-K16	0x1	—
484-K16	0x1	—
811-K32 – SCR 0	0x6	—
812_K16	0x7	—
812-K32	0xF	—
821-K20	0x1	0x1

Related Information

Programmable RBD Offset

1.7. Document Revision History for AN 832: Intel FPGA JESD204B IP Core and ADI AD9208 Hardware Checkout Report for Intel Stratix 10 Devices

Document Version	Changes
2018.05.24	• Updated the *Hardware Requirements* topic. • Updated the *Hardware Setup* topic. • Updated the following Figures: — *Hardware Setup* — *System Diagram* — *Deterministic Latency Test Setup Block Diagram*

Date	Version	Changes
December 2017	2017.12.18	Initial release.

1.8. Appendix

Device Used and Quartus Tool Version

For interoperability with ADC AD9208, two device variants of Intel Stratix 10 are used.

- For lane rates above 15G and up to 16G: 1SG280HU1F50E1VGS1 (Transceiver speed grade -1 device)
- For lane rates of 15G and lower: 1SG280HU2F50E2VGS1 (Transceiver speed grade -2 device)

Except for the modes LMF 821/822/841/842, these modes were generated in Transceiver speed grade -1 device in order to achieve timing.

Intel Quartus® Prime Pro Edition software version 17.1 IR2 Build 50 is used for compilation of designs.

Timing Closure Details

To achieve timing closure, the I/O ports of Assembler (Assembler to JESD IP) & De-assembler (JESD IP to De-assembler) were pipelined for the test modes LMF 882 & 884.

Synthesis/Fitter Settings:

The following Analysis/Fitter settings were added to the qsf file to close the timing requirements for the variants LMF 882 & LMF 884.

Compiler Setting	Value Used	Default Value
Optimization Technique	Speed	Balanced
Optimization Mode	Aggressive	Balanced
Router Timing Optimization Level	Maximum	Normal
Auto Packed Registers	Normal	Auto

continued...

Compiler Setting	Value Used	Default Value
Physical Synthesis	ON	OFF
Restructure Multipliers	OFF	Auto
Fitter Initial Placement Seed	1-10	1

Additional JESD modes supported by ADC:

The modes enlisted here have not been validated in this interoperability test, but they are supported by the ADC. These have been tabulated here for future reference.

L M F	S	N	N'	Comments
1 8 16	1	14	16	F=16 configuration is not supported by transport layer of Intel FPGA example design.
1 1 1	1	8	8	N'=8 configuration is not supported by transport layer of Intel FPGA example design.
1 1 2	2	8	8	
2 1 1	2	8	8	
2 1 2	4	8	8	
2 1 4	8	8	8	
4 1 1	4	8	8	
4 1 2	8	8	8	
1 2 2	1	8	8	
2 2 1	1	8	8	
2 2 2	2	8	8	
4 2 1	2	8	8	
4 2 2	4	8	8	
4 2 4	8	8	8	