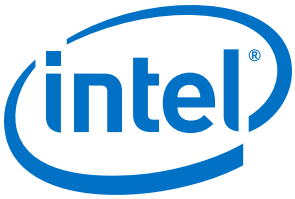

# AN 809: SerialLite III IP Core Feature and Interface Differences between Stratix 10, Arria 10, and Stratix V

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# SerialLite III IP Core Feature and Interface Differences between Stratix® 10 and Arria® 10, and Stratix® V

SerialLite III Streaming IP core enables high bandwidth, low latency data transfer in chip-to-chip, backplane, and board-to-board interface applications. The IP core utilizes lightweight serial protocol with minimal overhead, providing high data efficiency.

This document summarizes the SerialLite III Streaming IP core differences in Stratix® 10, Arria® 10, and Stratix V/Arria V GZ device families.

### Related Links

- SerialLite III Streaming IP Core User Guide
- Intel Stratix 10 SerialLite III Streaming IP Core Design Example User Guide
- Intel Arria 10 SerialLite III Streaming IP Core Design Example User Guide
- Stratix V SerialLite III Streaming IP Core Design Example User Guide

## Differences

The IP core differences in Stratix 10, Arria 10, and Stratix V device families are categorized as follow:

- Features
- Clocking
- IP Core GUI
- IP Core Signals

## Features

### Table 1. Features Comparison

| Stratix 10 | Arria 10 | Stratix V | Comments |
|---|---|---|---|
| MAC and PHY Control and Status Registers (CSRs) | PHY Control and Status Registers | PHY Control and Status Registers | For more information about the registers, refer to the MAC and PHY register map in SerialLite III Sreaming IP Core User Guide. |
| 17.4 Gbps | 17.4 Gbps | 14.1 Gbps | Maximum lane data rate |

### Table 2. Latency Measurement for Duplex Core (Stratix 10, Arria 10, and Stratix V)

These latency values are TX-to-RX round trip latencies (time from `start_of_burst_tx` to `start_of_burst_rx`).

| Device | Clocking Mode | Parameters | | Latency (ns) |
|---|---|---|---|---|
| | | Number of Lanes | Per-Lane Data Rate (Mbps) | |
| Stratix 10 | Standard | 6 | 12,500 | 304.128 |
| | Advanced | 6 | 12,500 | 272.810 |
| Arria 10 | Standard | 5 | 17,400 | 174.064 |
| | Advanced | 5 | 17,400 | 154.996 |
| Stratix V | Standard | 5 | 10,312.50 | 320.964 |
| | Advanced | 5 | 10,312.50 | 292.712 |

### Table 3. Estimated Resource Utilization in ALMs for Duplex Configuration (Stratix 10, Arria 10, and Stratix V)

| Device | Direction | Clocking Mode | Parameters | | | ALMs |
|---|---|---|---|---|---|---|
| | | | Number of Lanes | Per-Lane Data Rate (Mbps) | ECC | |
| Stratix 10 | Duplex | Standard | 16 | 17400 | Disabled | 5290 |
| | | Standard | 16 | 17400 | Enabled | 9986 |
| | | Advanced | 16 | 17400 | Disabled | 4725 |
| | | Advanced | 16 | 17400 | Enabled | 9375 |
| Arria 10 | Duplex | Standard | 24 | 17400 | Disabled | 6152 |
| | | Standard | 24 | 17400 | Enabled | 9313 |
| | | Advanced | 24 | 17400 | Disabled | 5833 |
| | | Advanced | 24 | 17400 | Enabled | 8868 |
| Stratix V | Duplex | Standard | 24 | 10312.50 | Disabled | 8742 |
| | | Standard | 24 | 10312.50 | Enabled | 14045 |
| | | Advanced | 24 | 10312.50 | Disabled | 7550 |
| | | Advanced | 24 | 10312.50 | Enabled | 12606 |

#### Related Links

SerialLite III Streaming IP Core User Guide

## Clocking

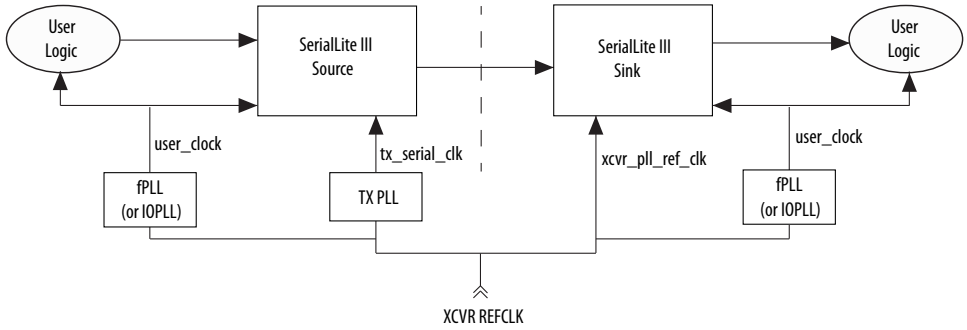
### Table 4. TX PLL Differences between Stratix 10, Arria 10, and Stratix V Devices

| Stratix 10 | Arria 10 | Stratix V | Comments |
|---|---|---|---|
| User shall instantiate a TX PLL outside the IP core | User shall instantiate a TX PLL outside the IP core | IP core includes a TX PLL | TX PLL (ATX, CMU, or fPLL) instantiation requirement |

**Table 5. Standard Clocking Mode Differences between Stratix 10, Arria 10, and Stratix V Devices**

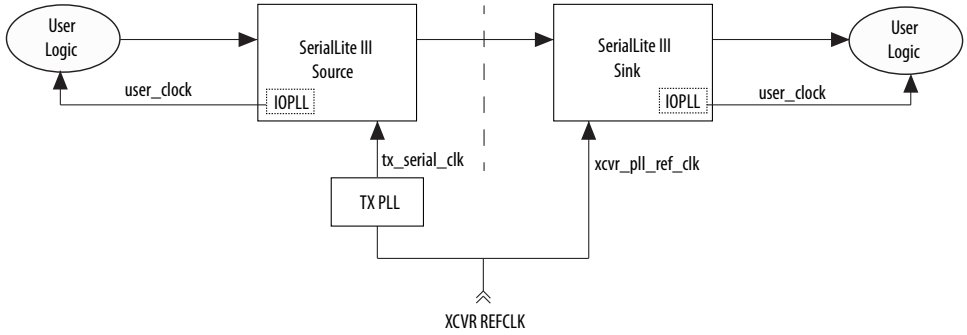
| Stratix 10 | Arria 10 | Stratix V | Comments |
|---|---|---|---|
| User logic shall provide a `user_clock` to the IP core | IP core provides a `user_clock` to user logic | IP core provides a `user_clock` to user logic | User clock direction.<br>Specify frequency in the IP parameter GUI. |
| External PLL instantiated by user provides the `user_clock` | An IOPLL inside the IP core generates the `user_clock` | An fPLL inside the IP core generates the `user_clock` | User clock generation. |
| User clock PLL (fPLL or IOPLL) sharing supported across multiple IP core instances | User clock PLL (IOPLL) cannot be automatically shared across multiple IP core instances | User clock PLL (fPLL) cannot be automatically shared across multiple IP core instances | PLL sharing for user clock.<br>For Stratix 10, user clock PLL is external to the IP core.<br>For Arria 10 and Stratix V, the user clock PLL is in the IP core. |

**Figure 1. Stratix 10 Standard Clocking Mode Clocking**



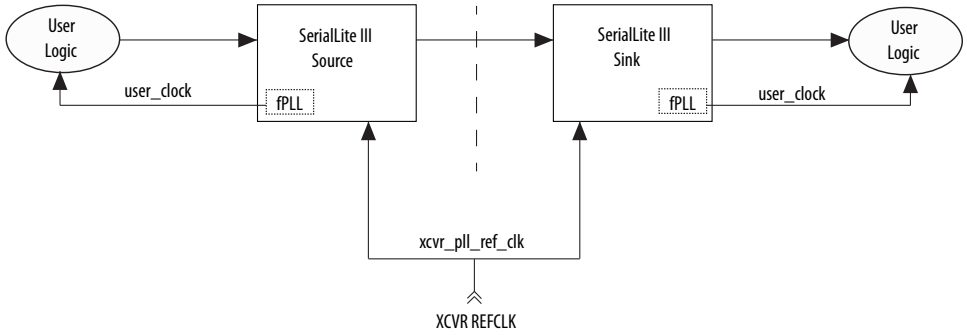

-Drive Source and Sink transceiver (XCVR) REFCLKs from the same oscillator
-Source and Sink fPLLs use XCVR REFCLK as reference clock
-Multiple SerialLite III instances can share TX PLL and/or fPLL (or IOPLL)

**Figure 2. Arria 10 Standard Clocking Mode Clocking**




-Drive Source and Sink transceiver (XCVR) REFCLKs from the same oscillator
-Source IOPLL reference clock is from the transceiver PHY tx_clkout
-Sink IOPLL reference clock is from the transceiver PHY rx_clkout
-IOPLL generates user_clock only
-IP core is clocked by the transceiver PHY parallel clock (tx_clkout, rx_clkout)
-Multiple Source instances can share a TX PLL

**Figure 3. Stratix V Standard Clocking Mode Clocking**

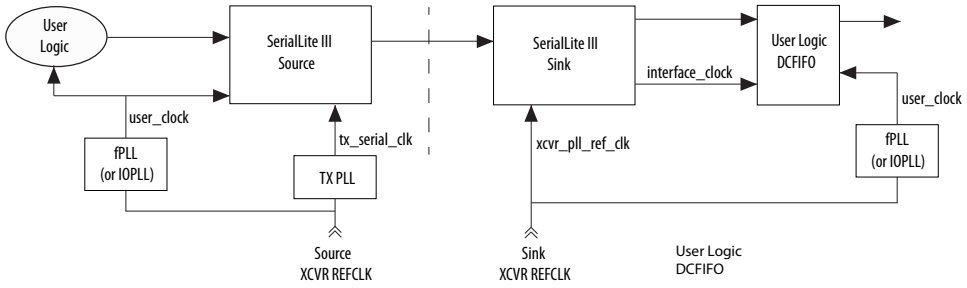



-Drive Source and Sink transceiver (XCVR) REFCLKs from the same oscillator
-Source fPLL reference clock is from the transceiver PHY tx_clkout
-Sink fPLL reference clock is from the transceiver PHY rx_clkout
-fPLL generates two clocks – user_clock and IP core clock

**Table 6. Advanced Clocking Mode Differences between Stratix 10, Arria 10, and Stratix V devices**

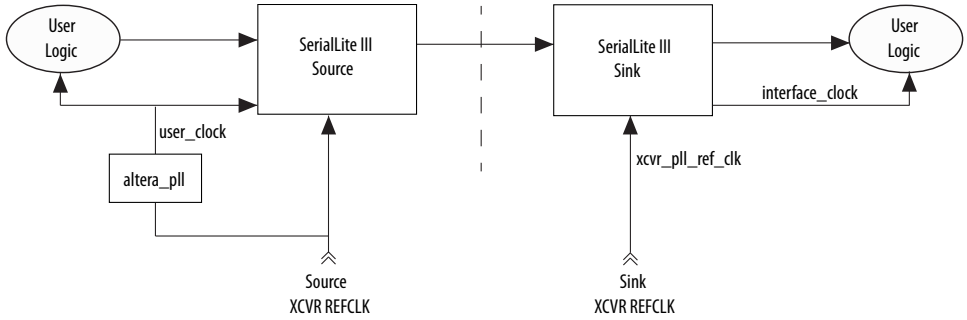
| Stratix 10 | Arria 10 | Stratix V | Comments |
|---|---|---|---|
| Lane data rate divided by PCS-PMA bus width (PCS-PMA bus width: 64) | Lane data rate divided by PCS-PMA bus width (PCS-PMA bus width: 64) | Lane data rate divided by PCS-PMA bus width (PCS-PMA bus width: 40) | Sink Interface clock frequency.<br>*Note:* Source user clock frequency is specified in the IP Core GUI if **User input** selects **User Clock Frequency**. |

**Figure 4. Stratix 10 and Arria 10 Advanced Clock Mode Clocking**




-Drive Source and Sink transceiver (XCVR) REFCLK's from the same oscillator

**Figure 5. Stratix V Advanced Clock Mode Clocking**




-Drive Source and Sink transceiver (XCVR) REFCLKs from the same oscillator

## IP Core GUI

**Table 7. IP Core GUI Differences between Stratix 10, Arria 10, and Stratix V**

| Stratix 10 | Arria 10 | Stratix V | Comments |
|---|---|---|---|
| Adaptation FIFO partial full threshold | N/A | N/A | Stratix 10: Backpressure the upstream data through tx_ready port when the partial full flag triggers. |
| N/A | N/A | Device speed grade | Transceiver speed grade.<br>Stratix 10 and Arria 10: N/A (user should refer to the transceiver PHY datasheet for the maximum data rate supported.)<br>Stratix V: This is used to determine supported data rate (Stratix V IP parameter does not generate an error) |
| N/A | N/A | PLL type (CMU, ATX, fPLL) | Stratix 10 and Arria 10: Transmitter (TX) PLL is instantiated outside the IP core. |
| **Example Design Presets** | | | |
| • Advanced_Clocking_Mode_6x12.5G<br>• Advanced_Clocking_Mode_6x17.4G<br>• Standard_Clocking_Mode_6x12.5G<br>• Standard_Clocking_Mode_6x17.4G | • Advanced Clocking Mode 2x10G<br>• Advanced Clocking Mode 6x12.5G<br>• Standard Clocking Mode 2x10G<br>• Advanced Clocking Mode 6x12.5G | • Advanced Clocking Mode 2x10G<br>• Standard Clocking Mode 2x10G | Presets in IP GUI supported for design example generation. |

### Related Links

- Intel Stratix 10 SerialLite III Streaming IP Core Design Example User Guide
- Intel Arria 10 SerialLite III Streaming IP Core Design Example User Guide
- Stratix V SerialLite III Streaming IP Core Design Example User Guide

## IP Core Signals

### Table 8. IP Core Signal Differences in Stratix 10, Arria 10, and Stratix V

| Stratix 10 | Arria 10 | Stratix V | Comments |
|---|---|---|---|
| ready (`ready_tx`, `ready_rx` in Duplex IP) | N/A | N/A | Stratix 10: This is backpressure signal. In Source application, IP core backpressures user logic based on internal FIFO fill level. In Sink application, user logic backpressures IP core when not ready. Leave unconnected if unused. |
| err_interrupt (`err_interrupt_tx`, `err_interrupt_rx` in Duplex IP) | N/A | N/A | Stratix 10: Interrupt output. This signal indicates whether a transmit/ receive has occurred in the current transmission. Leave unconnected if unused. |
| **Avalon-MM Interface** | | | |
| 12 + Ceil($Log_2N$) [1] | 10 + Ceil($Log_2N$) [1] | 9 | `phy_mgmt_addr` port width. |
| **Reset and Clock Interface** | | | |
| N/A | `core_reset` | `core_reset` | Stratix 10: There is no separate reset for the MAC (`phy_mgmt_clk_reset` resets both the MAC and PHY layers).<br>Arria 10 and Stratix V: Asynchronous reset input for the MAC layer. It resets the MAC except for the IOPLL (Arria 10)/fPLL (Stratix V) used in Standard Clocking Mode. |
| N/A | interface_clock_reset (`interface_clock_reset_tx`, `interface_clock_reset_rx` in Duplex) | interface_clock_reset (`interface_clock_reset_tx`, `interface_clock_reset_rx` in Duplex) | Arria 10 and Stratix V: IP core asserts this signal when the `core_reset` is high and deasserts this signal when the reset sequence is complete.<br>Available only in advanced clocking mode. |
| **Others** | | | |
| N/A | reconfig_busy | reconfig_busy | Stratix 10: Not used. Tie this signal to 0.<br>Arria 10 and Stratix V: When asserted, this signal indicates that a reconfiguration is in progress. |

## Summary

This document is to facilitate a quicker understanding of the differences in SerialLite III Streaming IP core for Stratix 10, Arria 10, and Stratix V devices and help you to migrate the SerialLite III interface designs between different device families.

For more information, contact your local field application engineer (FAE) or open a Service Request (SR).

### Related Links

- SerialLite III Streaming IP Core User Guide

1 N: number of lanes.

- Intel Stratix 10 SerialLite III Streaming IP Core Design Example User Guide
- Intel Arria 10 SerialLite III Streaming IP Core Design Example User Guide
- Stratix V SerialLite III Streaming IP Core Design Example User Guide

## Revision History

**Table 9.**

| Date | Version | Changes |
|---|---|---|
| June 2017 | 2017.06.19 | Initial release. |