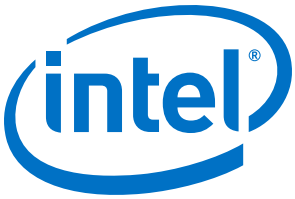

# AN 795: Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC Intel® FPGA IP in Intel® Arria® 10 Devices

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# Contents

# 1. Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC Intel® FPGA IP in Intel® Arria® 10 Devices

The implementing guidelines show you how to use Intel's Low Latency 10G Media Access Controller (MAC) and PHY IPs.

**Figure 1. Intel® Arria® 10 Low Latency Ethernet 10G MAC System**

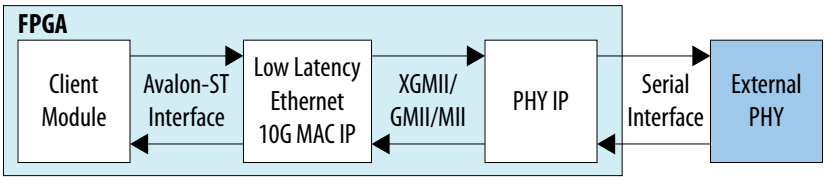



**Table 1. Intel® Arria® 10 Low Latency Ethernet 10G MAC Designs**

This table lists all the Intel® Arria® 10 designs for Low Latency Ethernet 10G MAC Intel FPGA IP.

| Design Example | MAC Variant | PHY | Development Kit |
|---|---|---|---|
| 10GBase-R Ethernet | 10G | Native PHY | Intel Arria 10 GX Transceiver SI |
| 10GBase-R Register Mode Ethernet | 10G | Native PHY | Intel Arria 10 GX Transceiver SI |
| XAUI Ethernet | 10G | XAUI PHY | Intel Arria 10 GX FPGA |
| 1G/10G Ethernet | 1G/10G | 1G/10GbE and 10GBASE-KR PHY | Intel Arria 10 GX Transceiver SI |
| 1G/10G Ethernet with 1588 | 1G/10G | 1G/10GbE and 10GBASE-KR PHY | Intel Arria 10 GX Transceiver SI |
| 10M/100M/1G/10G Ethernet | 10M/100M/1G/10G | 1G/10GbE and 10GBASE-KR PHY | Intel Arria 10 GX Transceiver SI |
| 10M/100M/1G/10G Ethernet with 1588 | 10M/100M/1G/10G | 1G/10GbE and 10GBASE-KR PHY | Intel Arria 10 GX Transceiver SI |
| 1G/2.5G Ethernet | 1G/2.5G | 1G/2.5G/5G/10G Multi-rate Ethernet PHY | Intel Arria 10 GX Transceiver SI |
| 1G/2.5G Ethernet with 1588 | 1G/2.5G | 1G/2.5G/5G/10G Multi-rate Ethernet PHY | Intel Arria 10 GX Transceiver SI |
| 1G/2.5G/10G Ethernet | 1G/2.5G/10G | 1G/2.5G/5G/10G Multi-rate Ethernet PHY | Intel Arria 10 GX Transceiver SI |
| 10G USXGMII Ethernet | 1G/2.5G/5G/10G (USXGMII) | 1G/2.5G/5G/10G Multi-rate Ethernet PHY | Intel Arria 10 GX Transceiver SI |

*Note:* You can access all the listed designs through the Low Latency Ethernet 10G MAC Intel FPGA IP parameter editor in the Intel Quartus® Prime software, except for the XAUI Ethernet reference design. You can get the XAUI Ethernet reference design from the Design Store.

Intel offers separate MAC and PHY IPs for the 10M to 1G Multi-rate Ethernet subsystems to ensure flexible implementation. You can instantiate the Low Latency Ethernet 10G MAC Intel FPGA IP with 1G/2.5G/5G/10G Multi-rate Ethernet PHY, Intel Arria 10 1G/10GbE and 10GBASE-KR PHY, or XAUI PHY and Intel Arria 10 Transceiver Native PHY to cater different design requirements.

**Related Information**

- Low Latency Ethernet 10G MAC Intel FPGA IP User Guide
  Provides detailed information about instantiating and parameterizing the MAC IP.
- Low Latency Ethernet 10G MAC Intel Arria 10 FPGA IP Design Example User Guide
  Provides detailed information about instantiating and parameterizing the MAC design examples.
- Intel Arria 10 Transceiver PHY User Guide
  Provides detailed information about instantiating and parameterizing the PHY IP.
- Low Latency Ethernet 10G MAC Debug Checklist
- AN 699: Using the Altera Ethernet Design Toolkit
  This toolkit helps you to configure and run Ethernet reference designs as well as debug any Ethernet related issues.
- Fault Tree Analysis for Low Latency 10G MAC Data Corruption Issue
- Arria 10 Low Latency Ethernet 10G MAC and XAUI PHY Reference Design
  Provides the files for the reference design.

## 1.1. Low Latency Ethernet 10G MAC and Intel Arria 10 Transceiver Native PHY Intel FPGA IPs

You can configure the Intel Arria 10 Transceiver Native PHY Intel FPGA IP to implement the 10GBASE-R PHY with the Ethernet specific physical layer running at 10.3125 Gbps data rate as defined in Clause 49 of the IEEE 802.3-2008 specification.

This configuration provides an XGMII to Low Latency Ethernet 10G MAC Intel FPGA IP and implements a single-channel 10.3 Gbps PHY providing a direct connection to an SFP+ optical module using SFI electrical specification.

Intel offers two 10GBASE-R Ethernet subsystem design examples and you can generate these designs dynamically using the Low Latency Ethernet 10G MAC Intel FPGA IP parameter editor. The designs support functional simulation and hardware testing on designated Intel development kits.

**Figure 2. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and Intel Arria 10 Transceiver Native PHY in 10GBASE-R Design Example**

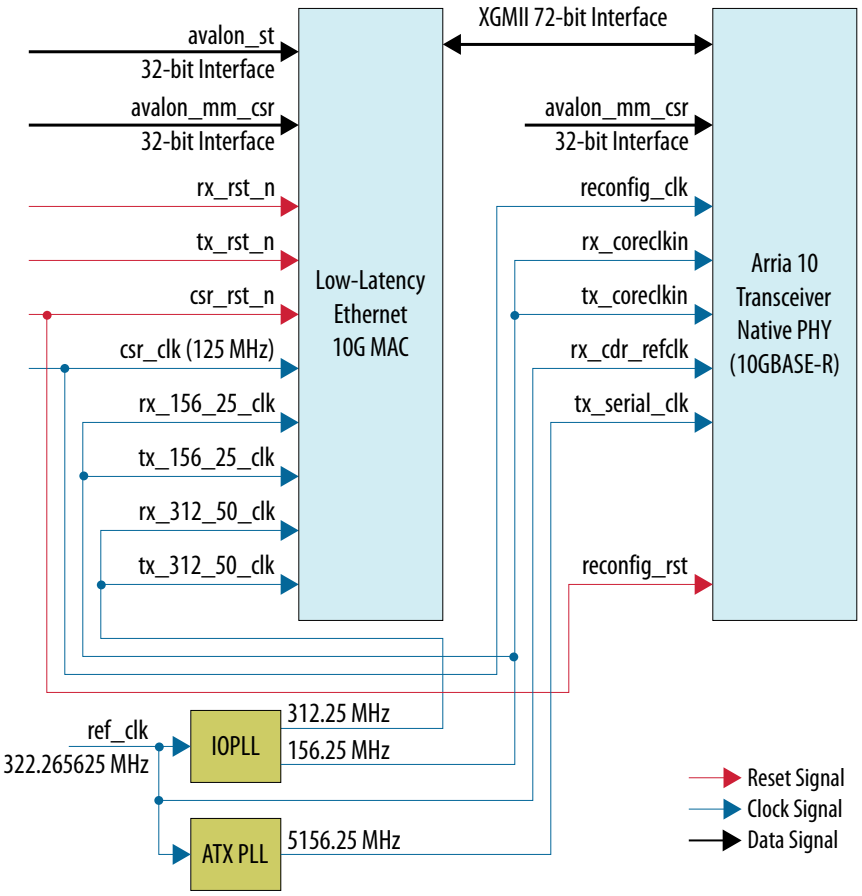
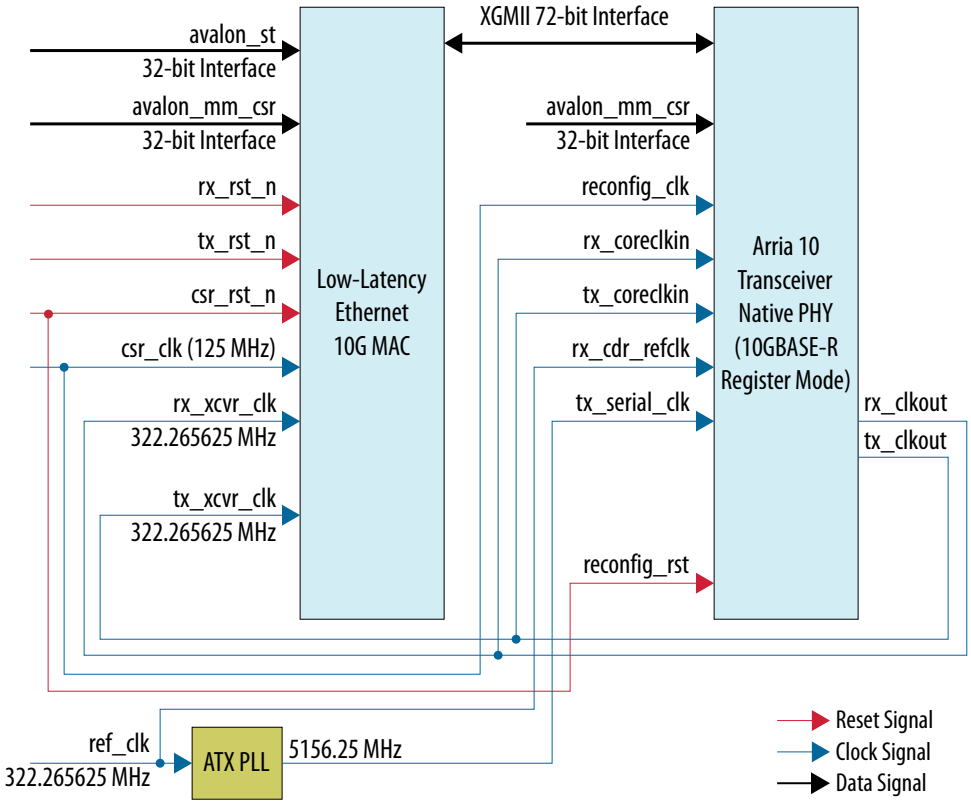


**Figure 3. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and Intel Arria 10 Transceiver Native PHY in 10GBASE-R Design Example with Register Mode Enabled**




**Related Information**

Low Latency Ethernet 10G MAC Intel Arria 10 FPGA IP Design Example User Guide
Provides detailed information about instantiating and parameterizing the MAC design examples.

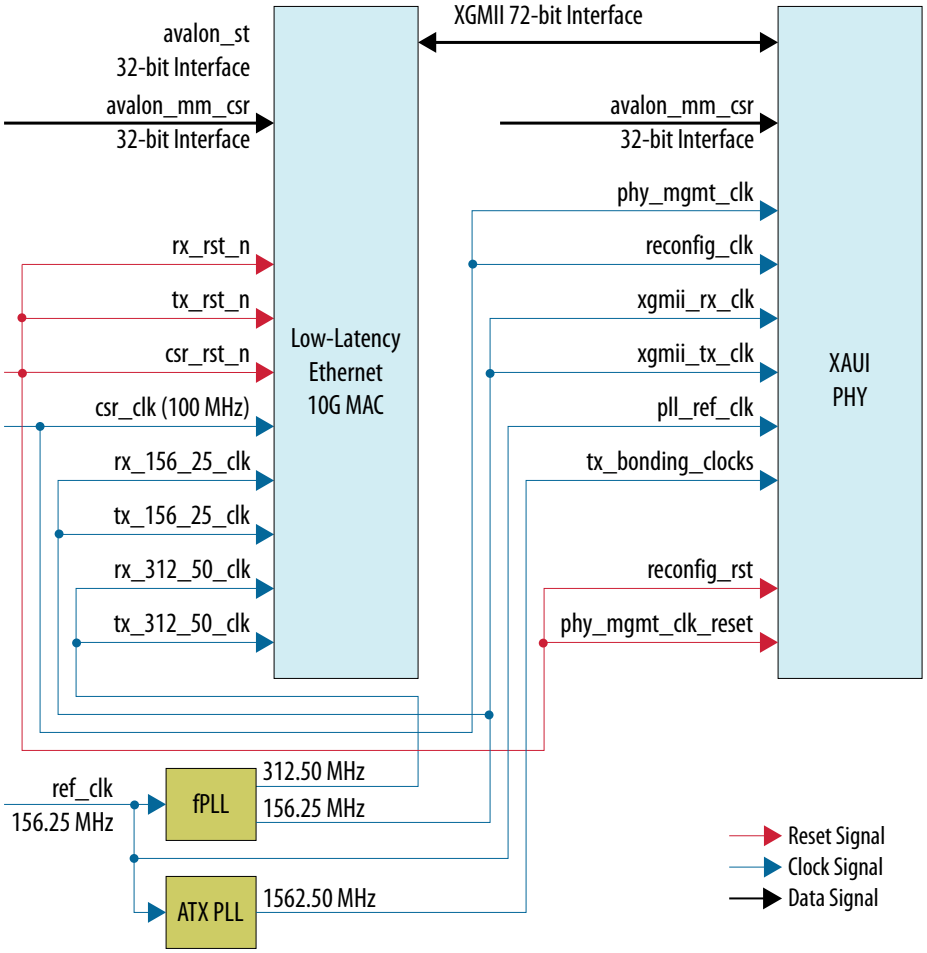
## 1.2. Low Latency Ethernet 10G MAC and XAUI PHY Intel FPGA IPs

The XAUI PHY Intel FPGA IP provides an XGMII to Low Latency Ethernet 10G MAC Intel FPGA IP and implements four lanes each at 3.125 Gbps at the PMD interface.

The XAUI PHY is a specific physical layer implementation of the 10 Gigabit Ethernet link defined in the IEEE 802.3ae-2008 specification.

You can obtain the reference design for the 10GbE subsystem implemented using Low Latency Ethernet 10G MAC and XAUI PHY Intel FPGA IPs from Design Store. The design supports functional simulation and hardware testing on designated Intel development kit.

**Figure 4. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and XAUI PHY Reference Design**




**Related Information**

- Arria 10 Low Latency Ethernet 10G MAC and XAUI PHY Reference Design
  Provides the files for the reference design.
- AN 794: Arria 10 Low Latency Ethernet 10G MAC and XAUI PHY Reference Design

## 1.3. Low Latency Ethernet 10G MAC and 1G/10GbE and 10GBASE-KR PHY Intel Arria 10 FPGA IPs

The 1G/10GbE and 10GBASE-KR PHY Intel Arria 10 FPGA IP provide MII, GMII and XGMII to Low Latency Ethernet 10G MAC Intel FPGA IP.

The 1G/10GbE and 10GBASE-KR PHY Intel Arria 10 FPGA IP implement a single-channel 10Mbps/100Mbps/1Gbps/10Gbps serial PHY. The designs provide a direct connection to 1G/10GbE dual speed SFP+ pluggable modules, 10M–10GbE 10GBASE-T and 10M/100M/1G/10GbE 1000BASE-T copper external PHY devices, or chip-to-chip interfaces. These IP cores support reconfigurable 10Mbps/100Mbps/1Gbps/10Gbps data rates.

Intel offers dual-speed 1G/10GbE and multi-speed 10Mb/100Mb/1Gb/10GbE design examples and you can generate these designs dynamically using the Low Latency Ethernet 10G MAC Intel FPGA IP parameter editor. The designs support functional simulation and hardware testing on designated Intel development kit.

The multi-speed Ethernet subsystem implementation using 1G/10GbE or 10GBASE-KR PHY Intel Arria 10 FPGA IP design requires manual SDC constraints for the internal PHY IP clocks and clock domain crossing handling. Refer to the `altera_eth_top.sdc` file in the design example to know more about the required `create_generated_clock`, `set_clock_groups` and `set_false_path` SDC constraints.

**Figure 5. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and Intel Arria 10 1G/10GbE and 10GBASE-KR Design Example (1G/10GbE Mode)**

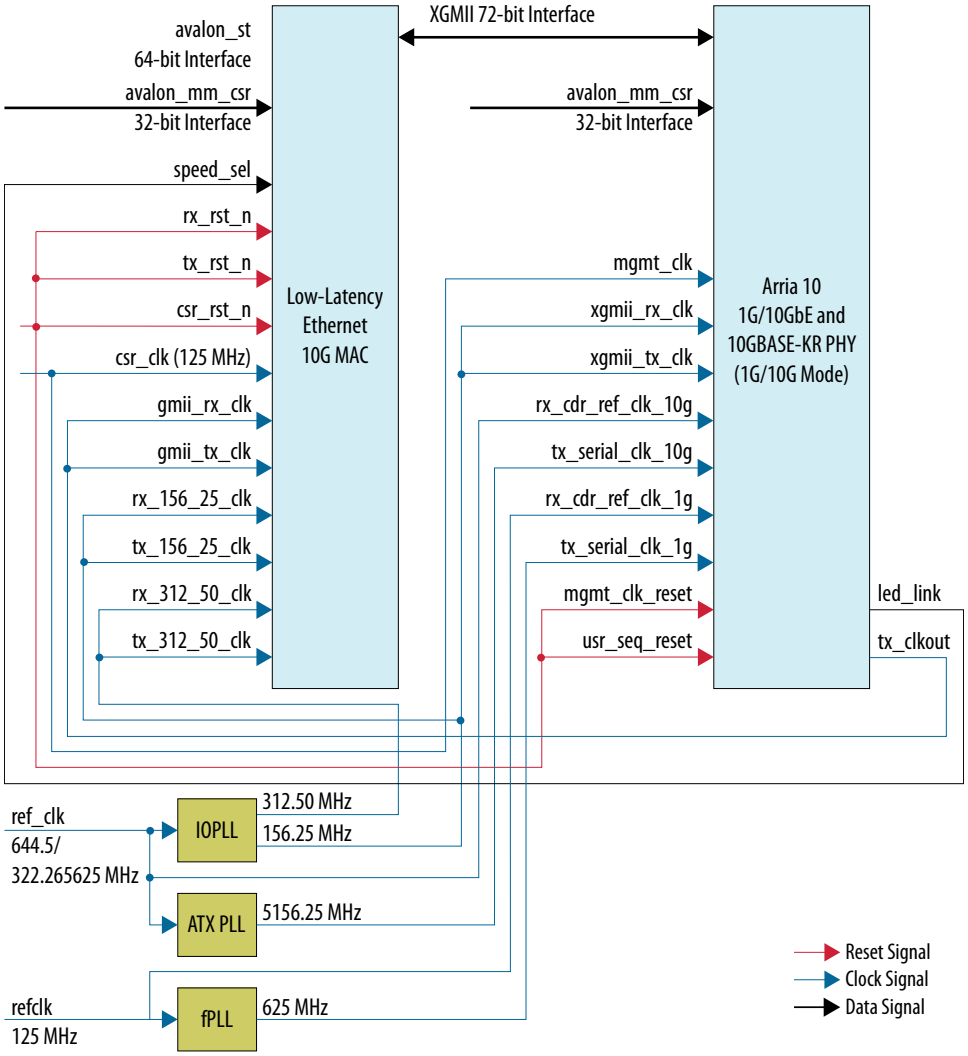
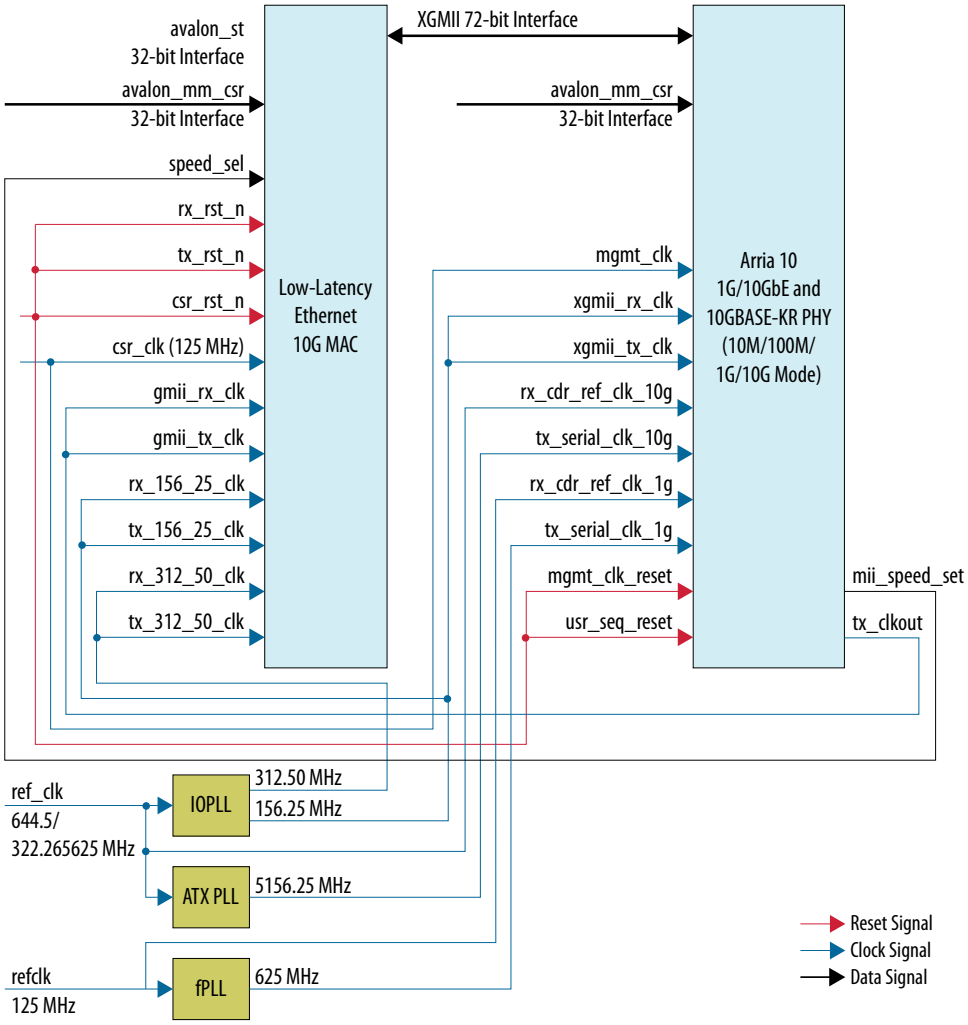


**Figure 6. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and Intel Arria 10 1G/10GbE and 10GBASE-KR Design Example (10Mb/100Mb/1Gb/10GbE Mode)**




### Related Information

Low Latency Ethernet 10G MAC Intel Arria 10 FPGA IP Design Example User Guide
Provides detailed information about instantiating and parameterizing the MAC design examples.

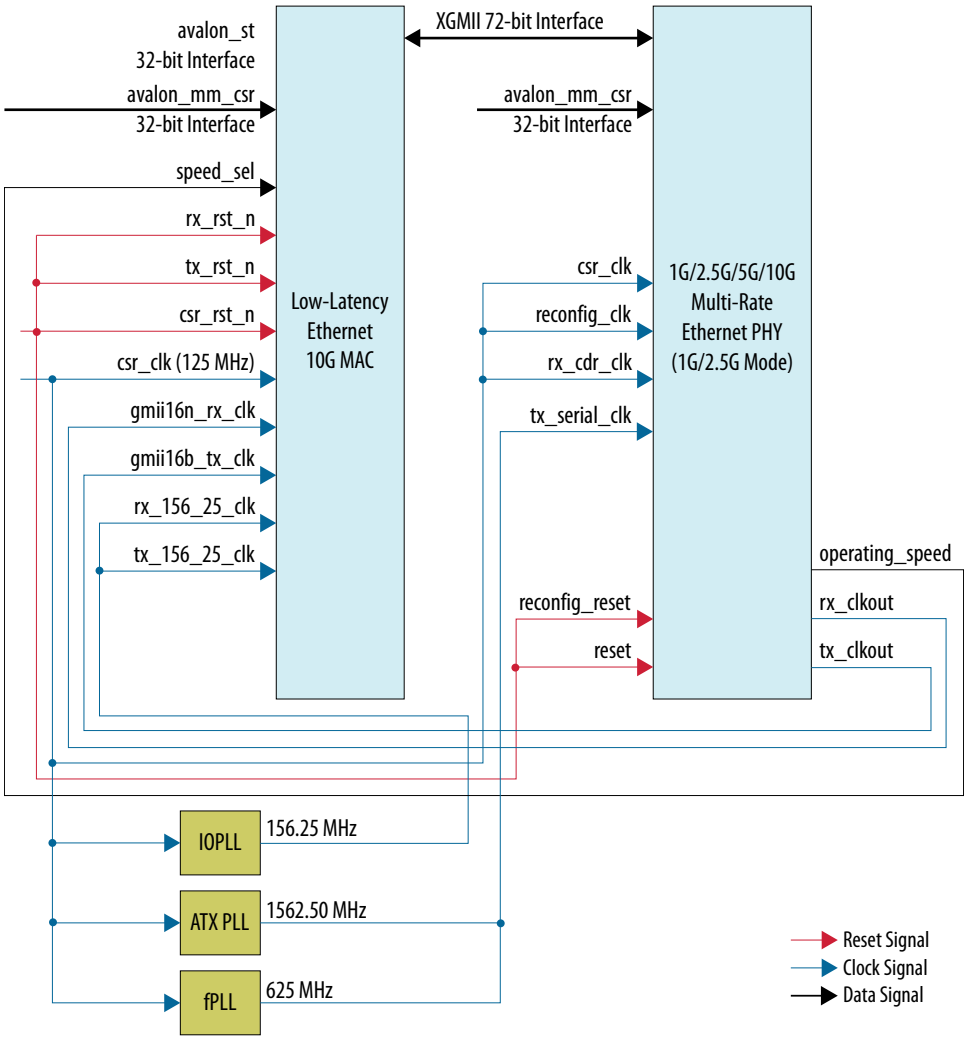
## 1.4. Low Latency Ethernet 10G MAC and 1G/2.5G/5G/10G Multi-Rate Ethernet PHY Intel FPGA IPs

The 1G/2.5G/5G/10G Multi-Rate Ethernet PHY Intel FPGA IP for Intel Arria 10 devices provides GMII and XGMII to the Low Latency Ethernet 10G MAC Intel FPGA IP.

The 1G/2.5G/5G/10G Multi-Rate Ethernet PHY Intel FPGA IP for Intel Arria 10 devices implements a single-channel 1G/2.5G/5G/10Gbps serial PHY. The design provides a direct connection to 1G/2.5GbE dual speed SFP+ pluggable modules, MGBASE-T and NBASE-T copper external PHY devices, or chip-to-chip interfaces. These IPs support reconfigurable 1G/2.5G/5G/10Gbps data rates.

Intel offers dual-speed 1G/2.5GbE, multi-speed 1G/2.5G/10GbE MGBASE-T, and multi-speed 1G/2.5G/5G/10GbE MGBASE-T design examples and you can generate these designs dynamically using the Low Latency Ethernet 10G MAC Intel FPGA IP parameter editor. The designs support functional simulation and hardware testing on designated Intel development kit.

**Figure 7. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and 1G/2.5G/5G/10G Multi-Rate Ethernet PHY Design Example (1G/2.5G Mode)**




For multi-speed 1G/2.5GbE and 1G/2.5G/10GbE MBASE-T Ethernet subsystem implementations using 1G/2.5G/5G/10G Multi-rate Ethernet PHY Intel FPGA IP, Intel recommends you copy the transceiver reconfiguration module

(`alt_mge_rcfg_a10.sv`) provided with the design example. This module reconfigures the transceiver channel speed from 1G to 2.5G, or to 10G, and vice versa.

The multi-speed 1G/2.5GbE and 1G/2.5G/10GbE MBASE-T Ethernet subsystem implementation also requires manual SDC constraints for the internal PHY IP clocks and clock domain crossing handling. Refer to the `altera_eth_top.sdc` file in the design example to know more about the required `create_generated_clock`, `set_clock_groups` and `set_false_path` SDC constraints.

**Figure 8. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and 1G/2.5G/5G/10G Multi-Rate Ethernet PHY Design Example (1G/2.5G/10GbE MBASE-T Mode)**

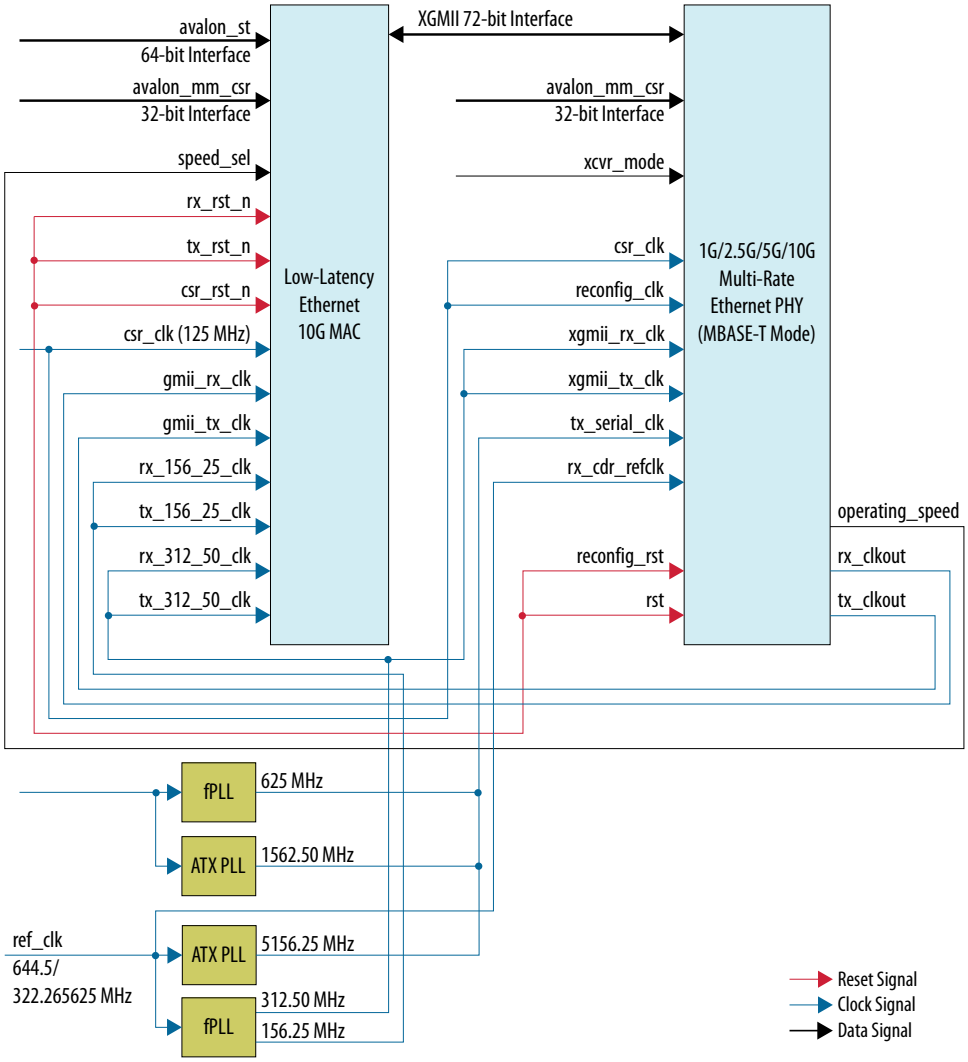
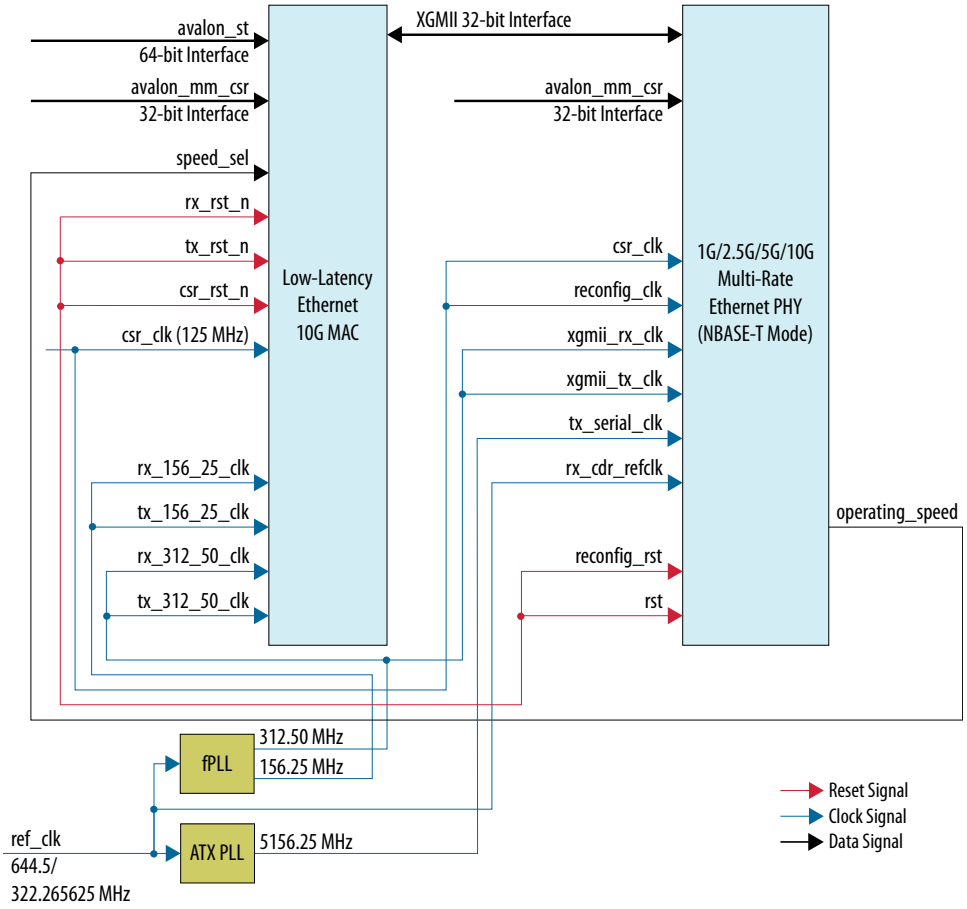


**Figure 9. Clocking and Reset Scheme for Low Latency Ethernet 10G MAC and 1G/2.5G/5G/10G Multi-Rate Ethernet PHY Design Example (1G/2.5G/5G/10GbE NBASE-T Mode)**




### Related Information

Low Latency Ethernet 10G MAC Intel Arria 10 FPGA IP Design Example User Guide
Provides detailed information about instantiating and parameterizing the MAC design examples.

## 1.5. Document Revision History for AN 795: Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC Intel FPGA IP in Intel Arria 10 Devices

| Document Version | Changes |
|---|---|
| 2020.10.28 | • Rebranded as Intel.<br>• Renamed the document as *AN 795: Implementing Guidelines for 10G Ethernet Subsystem Using Low Latency 10G MAC Intel FPGA IP in Intel Arria 10 Devices*. |

| Date | Version | Changes |
|---|---|---|
| February 2017 | 2017.02.01 | Initial release. |