AN 778: Intel® Stratix® 10 L-Tile/H-Tile Transceiver Usage

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1. Transceiver Layout

Note: This application note applies to Intel® Stratix® 10 L-tile and H-tile production devices only.

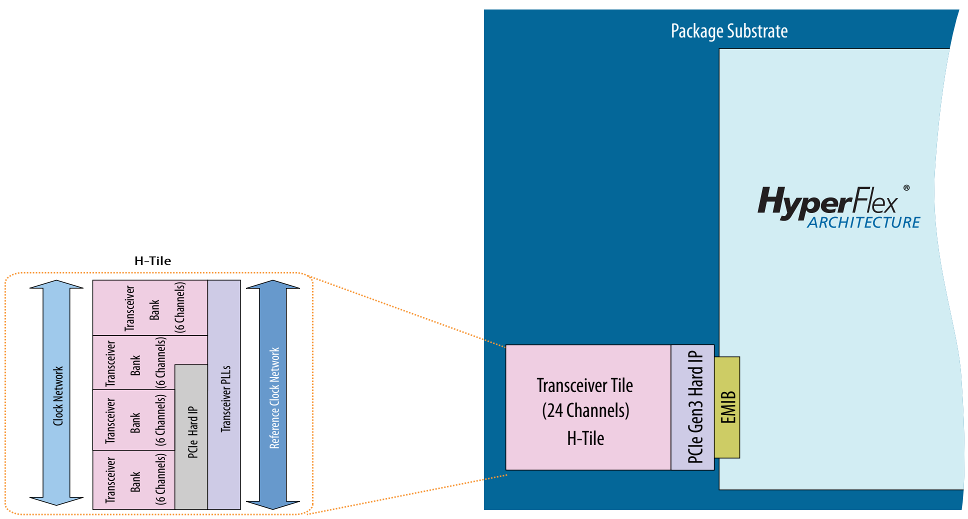
Intel Stratix 10 devices support a transceiver tile architecture. A tile consists of 24 transceiver channels and associated phase locked loops (PLLs), reference clock buffers, and Hard IPs.

The range of capabilities in each tile type offers a customized solution suited to the various transceiver applications. The next section describes the L-tile in greater detail. An Intel Stratix 10 device contains one or more tiles on the left and right side of the device. The types of tiles do not have to be homogeneous.

Refer to the table "Transceiver Tile Variants—Comparison of Transceiver Capabilities" in the Overview chapter of the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide* for additional information.

Figure 1. Transceiver Tile Layout

Example Intel Stratix 10 GX/SX device with an H-tile on the left side of the device.



Related Information

Overview

1.1. L-Tile and H-Tile Overview

The Intel Stratix 10 L-tile/H-tile transceivers contain 24 full-duplex channels, grouped into four transceiver banks.

Each tile is divided into banks of six channels each.

- 1 tile = 4 banks * 6 channels = 24 transceiver channels

Each bank contains two triplets of 3 channels each.

- 1 tile = 4 banks * 2 triplets * 3 channels = 24 transceiver channels

In L-tile up to 8 transceiver channels can be configured as GXT channels, reaching datarates up to 26.6 Gbps. Similarly in an H-tile, up to 16 channels can be configured as GXT channels reaching datarates up to 28.3 Gbps.

1.1.1. PLLs

Each Intel Stratix 10 L-tile/H-tile transceiver bank includes the following TX Phase Locked Loops (PLLs):

- Two Advanced Transmit (ATX) PLLs
- Two Fractional PLLs (fPLL)
- Two Clock Multiplier Unit (CMU) PLLs (Located in channel 1 and channel 4 of each bank)

Table 1. Transmitter PLLs in Stratix 10 L-Tile/H-Tile Devices

PLL Type	Characteristics
ATX PLL	• Best jitter performance • LC tank based voltage controlled oscillator (VCO) • Supports fractional synthesis mode (in cascade mode only) • Used for both bonded and non-bonded channel configurations
Fractional PLL (fPLL)	• Ring oscillator based VCO • Supports fractional synthesis mode • Used for both bonded and non-bonded channel configurations
Clock Multiplier Unit (CMU) PLL or Channel PLL [1]	• Ring oscillator based VCO • Used as an additional clock source for non-bonded applications

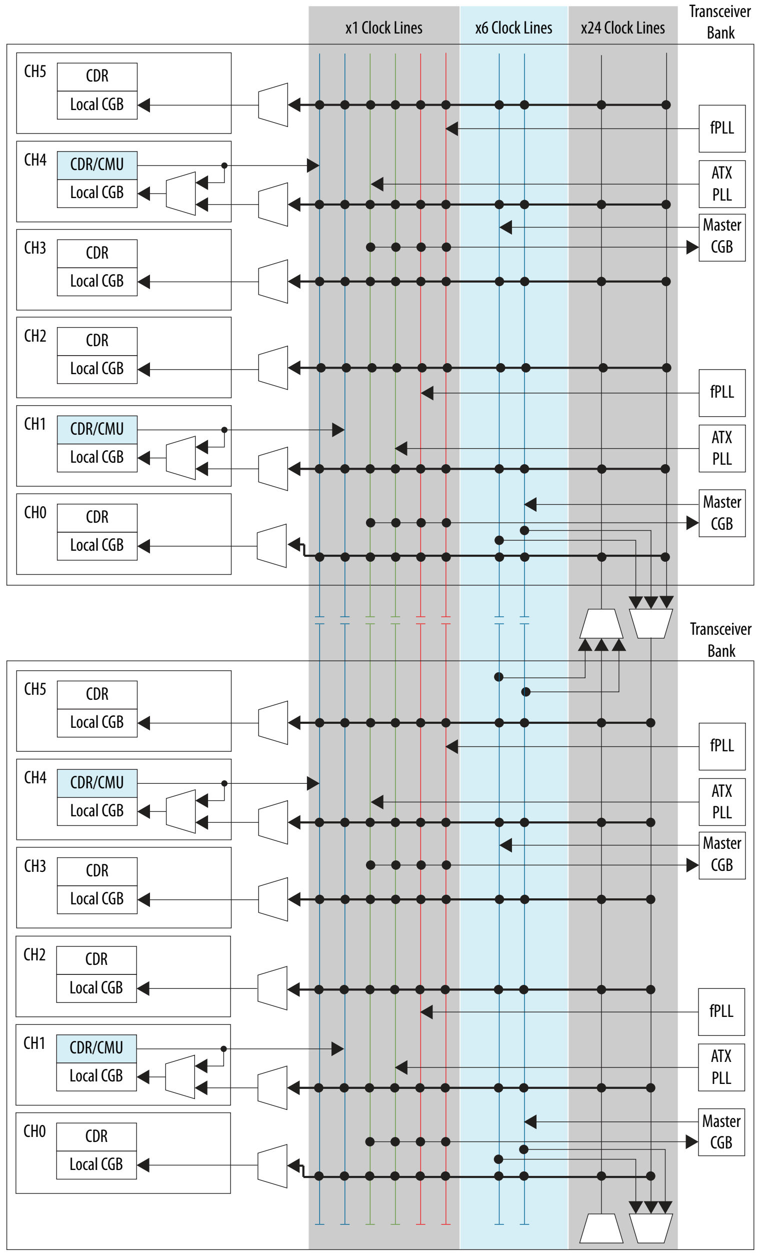
The total number of TX PLLs per tile is:

- Eight ATX PLLs (2 ATX PLLs per bank * 4 banks per tile)
- Eight fPLLs (2 fPLLs per bank * 4 banks per tile)
- Eight CMU PLLs (2 CMU PLLs per bank * 4 banks per tile)

(1) The CMU PLL or Channel PLL of channel 1 and channel 4 can be used as a transmitter PLL or as a clock data recovery (CDR) block. The channel PLL of all other channels (0, 2, 3, and 5) can only be used as a CDR.

Figure 2. Stratix 10 PLLs and Clock Networks in Two Banks of Intel Stratix 10 L-Tile/H-Tile

The ATX PLL, fPLL and CMU PLLs can drive the x1 clock network to support non-bonded transceivers. The ATX PLL and fPLL can drive the x6 clock network to support bonded transceivers within the bank. The x6 clock network can drive the x24 clock network in adjacent banks, allowing ATX PLLs and fPLLs to support up to 24 bonded transceiver channels. The x1, x6, and x24 clock networks are described in the *Transceiver Clock Network* section.



Note: For further details on CGB, refer to "PLL and Clock Networks" chapter in *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*.

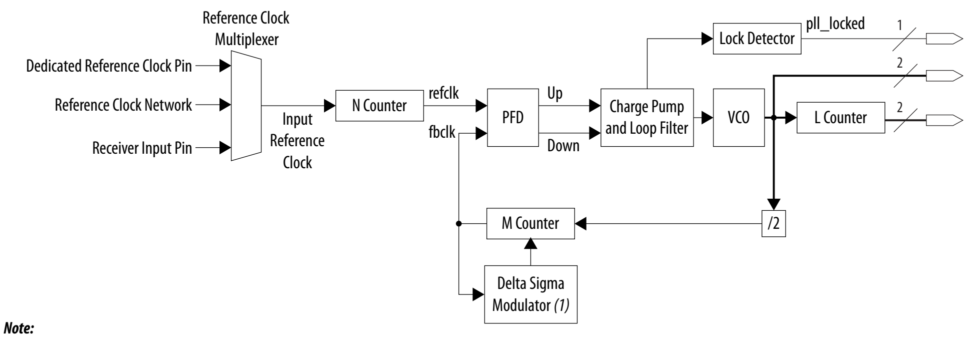
Related Information

- Transmitter Clock Network on page 7
- PLL and Clock Networks
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

1.1.1.1. ATX PLL

The ATX PLLs can be used for bonded and non-bonded applications. The ATX PLLs can access x1, x6, and x24 clock lines. There are spacing rules between two ATX PLLs running at the same VCO frequency. You can find the VCO frequency by looking at your PLL IP Platform Designer parameter. For more details, refer to *Transceiver Clock Network* and *ATX PLL Spacing Requirements*.

Figure 3. ATX PLL Block Diagram



Note:
1. The Delta Sigma Modulator is engaged only when the ATX PLL is used in fractional mode.

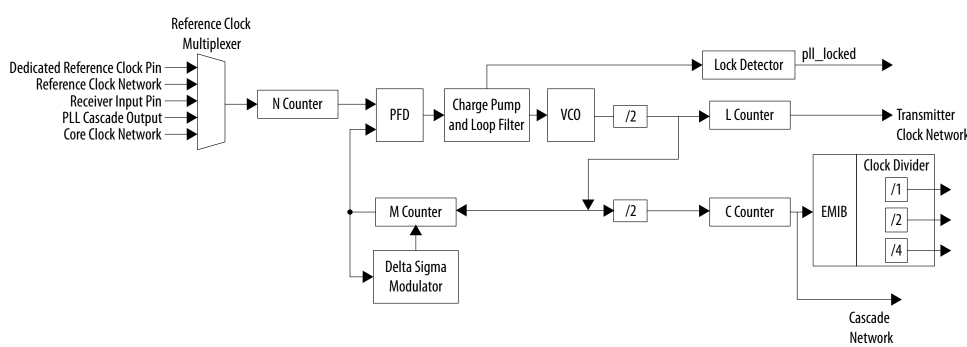
Related Information

Transmitter Clock Network on page 7

1.1.1.2. fPLL

The fPLLs can be used for bonded and non-bonded applications. The fPLLs can access x1, x6, and x24 clock lines. There are no spacing rules between fPLLs regardless of their VCO frequencies.

Figure 4. fPLL Block Diagram

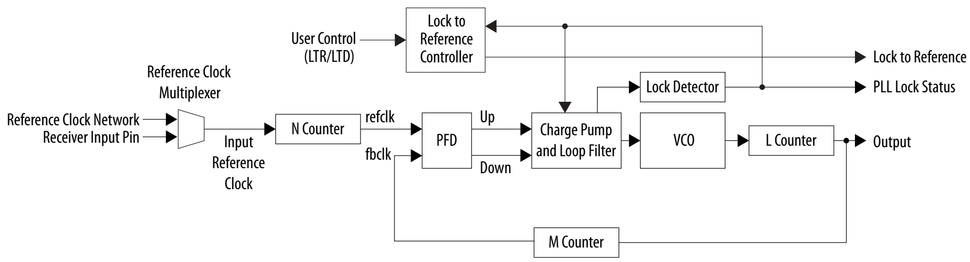


1.1.1.3. CMU PLL

CMU PLLs can only be used for non-bonded applications and can only access the x1 clock lines.

When using a CMU PLL in channel 1 or channel 4 of a bank, that channel is no longer available to receive data, but the channel can still be used for transmitting data.

Figure 5. CMU PLL Block Diagram



1.1.2. Transmitter Clock Network

The transmitter clock network routes the clock from the transmitter PLL to one or more transmitter channels. It provides two types of clocks to the transmitter channel:

- High-Speed Serial Clock - high-speed clock for the serializer
- Low-Speed Parallel Clock - low-speed clock for the serializer and the PCS

In a bonded channel configuration, both the serial clock and the parallel clock are routed from the transmitter PLL to the transmitter channels. In a non-bonded channel configuration, only the serial clock is routed to the transmitter channels, while the parallel clock is generated locally within each channel.

To support various bonded and non-bonded clocking configurations, three types of transmitter clock network lines are available:

- x1 clock lines: Span a single bank within a tile and are used for non-bonded channel clocking only
- x6 clock lines: Span a single bank within a tile and are used for bonded channel clocking
- x24 clock lines: Span all banks within a tile and are used for both PMA bonded and PMA-PCS bonded transceiver channels.

All clock lines are contained within a single tile and cannot span across multiple tiles.

Figure 6. x1 Clock Lines

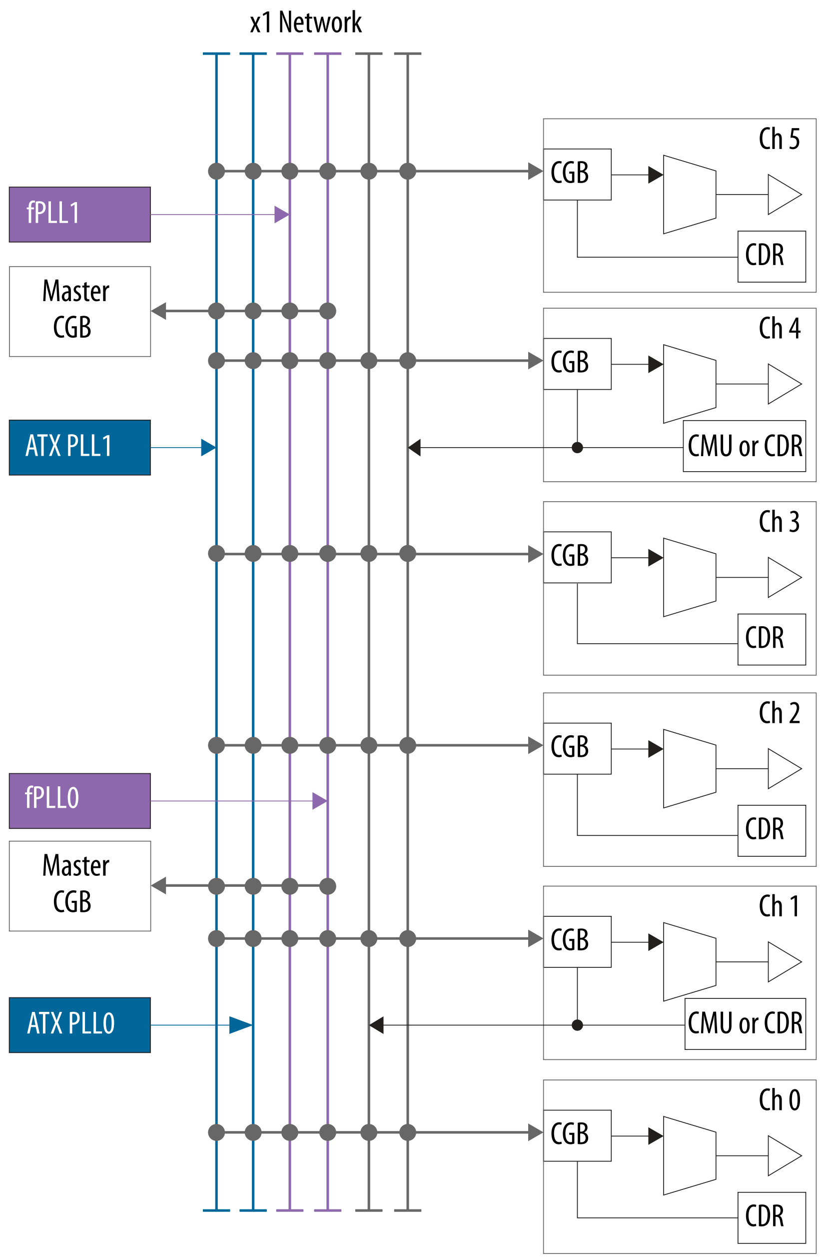


Figure 7. x6 Clock Lines

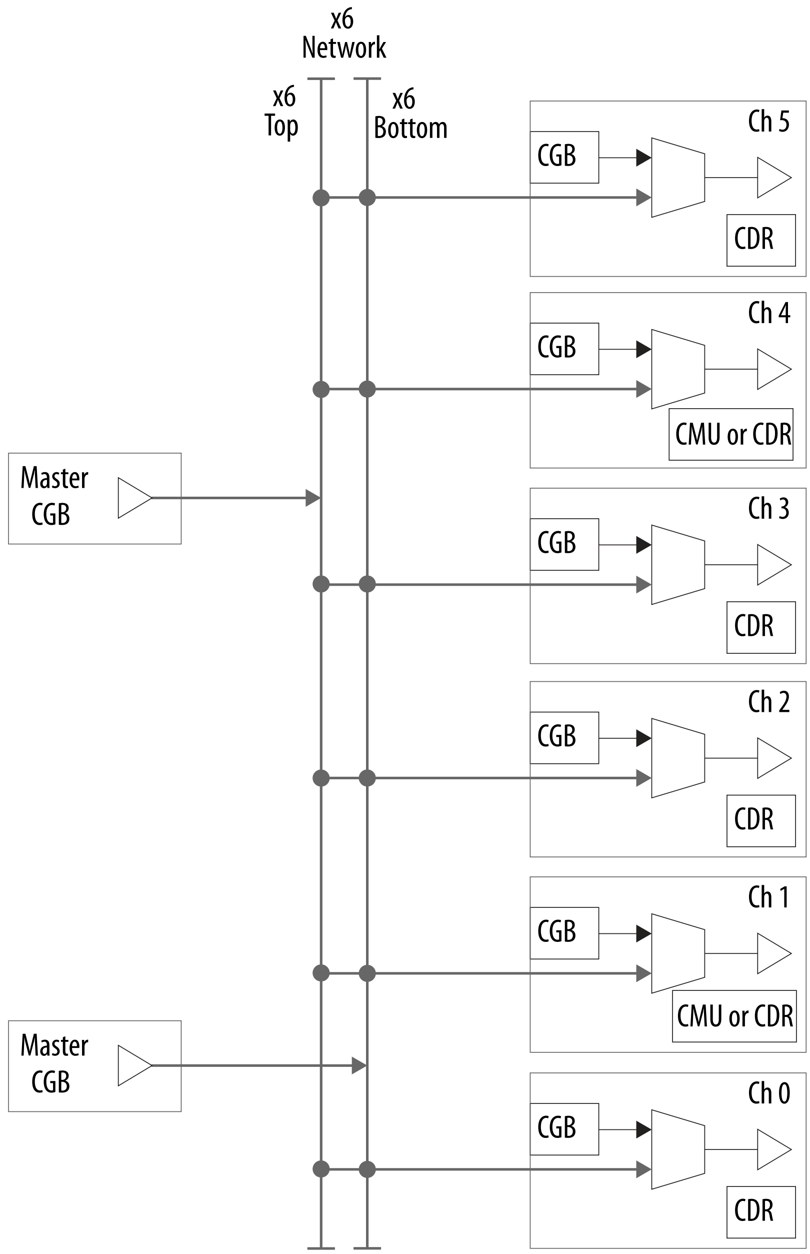
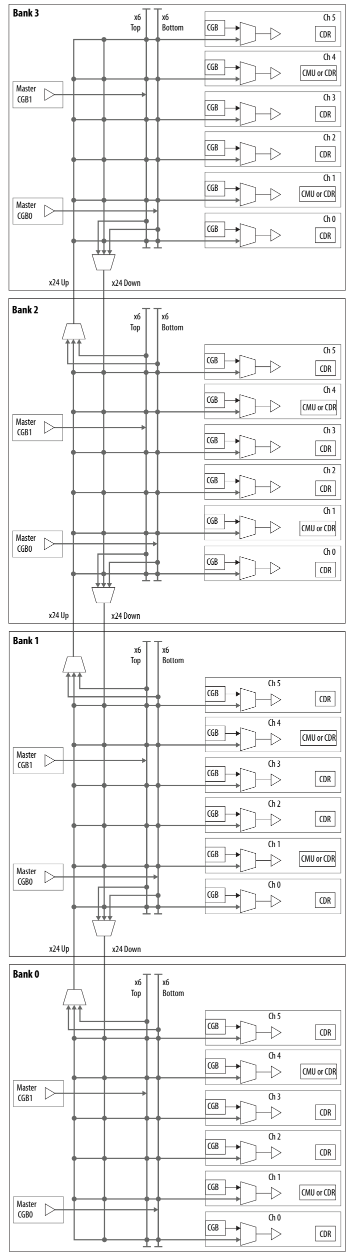


Figure 8. x24 Clock Lines



There are two x24 lines available per tile:

- x24 Up: Routes clocks to transceiver banks located above the current bank
- x24 Down: Routes clocks to transceiver banks located below the current bank

When using the x24 lines, the maximum channel span is two banks above and two banks below the master bank containing the instantiated TX PLL. If using the x24 clock lines across all four banks within the tile, the TX PLL must be instantiated in one of the middle banks to comply with the channel span requirements.

Related Information

- PLL and Clock Networks
- Channel Bonding

1.1.2.1. Bonded Transceiver Channels - Guidelines for VCCR_GXB and VCCT_GXB

Table 2. Voltage Requirements

For transceiver channels that require bonding via the x6/x24 transceiver clock networks, refer to this table for specific voltage requirements.

Channel Type	Transceiver Link Type	Data Rate	V_{CCR_GXB}/V_{CCT_GXB} Typical		
			Min	Typical	Max
GX	Chip to Chip and Backplane	1 Gbps to 16 Gbps	1 V	1.03 V	1.06 V
		16 Gbps to 17.4 Gbps	1.1 V	1.12 V	1.14 V
GXT	Chip to Chip and Backplane	> 17.4 Gbps	N/A (Bonding is not supported)		

For non-bonded transceiver channels, refer to the "Transceiver Power Supply Operating Conditions" in the Intel Stratix 10 Device Datasheet.

Related Information

Intel Stratix 10 Device Datasheet

1.1.3. GXT Clock Network

Both the L-tile and H-tile contains the GXT clock network. The GXT clock network allows an ATX PLL to drive up to six transmitter channels—four in its bank and two in an adjacent bank. The GXT clock network is used for data rates above 17.4 Gbps. Refer to *GXT Channels* for specification details. See "Using the ATX PLL for GXT Channels" in the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide* for an in-depth discussion of the GXT clock network and the ATX PLL usage of it.

Figure 9. Top ATX PLL GXT Network Reach (Right Side of Below Figure)

If the ATX PLL is in the upper triplet, its drive span is all four GXT channels within its own bank and channels ch0 and ch1 of the bank above.

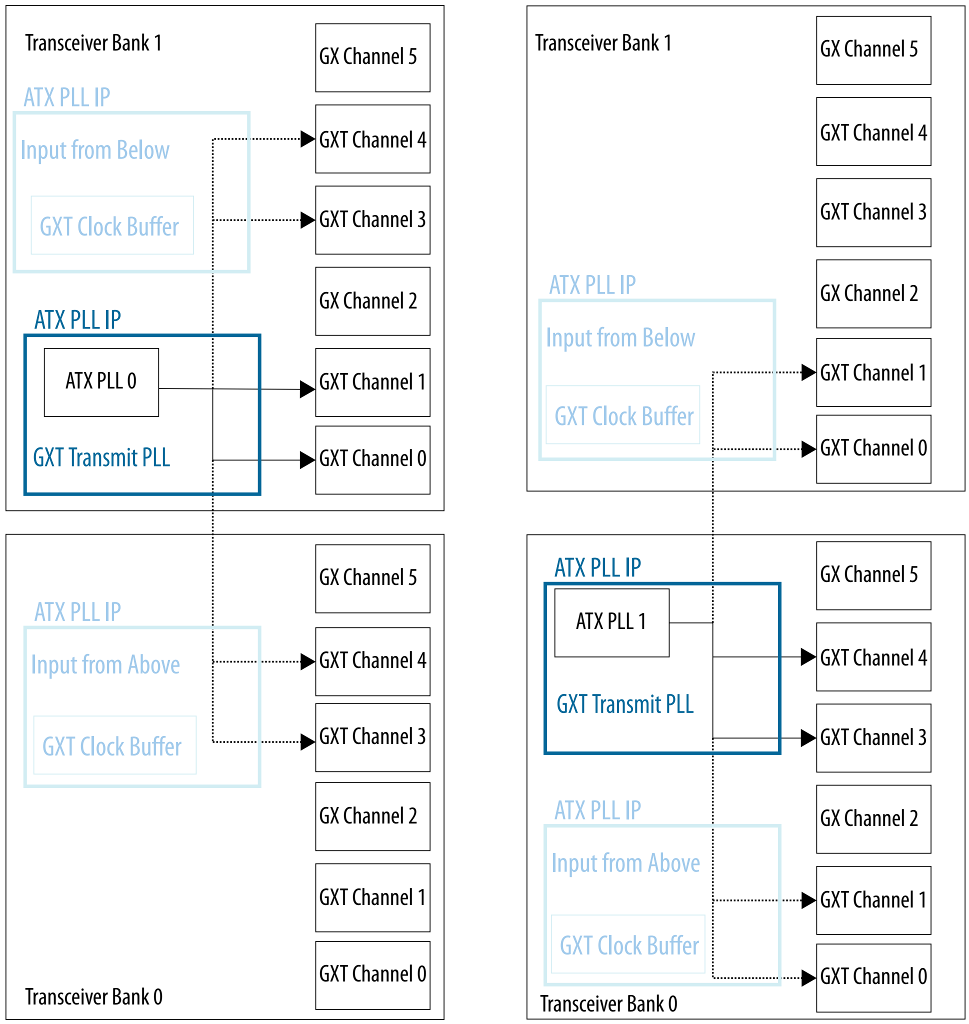
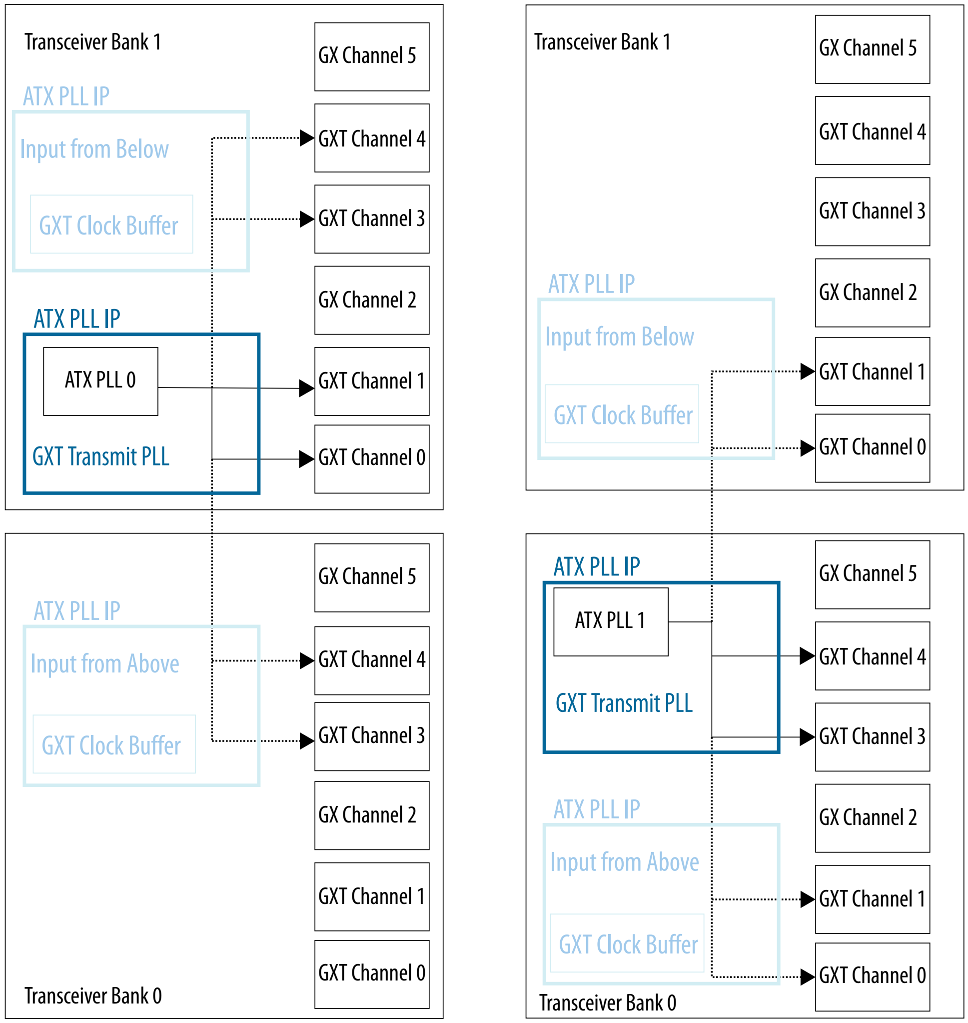


Figure 10. Bottom ATX PLL GXT Network Reach (Left Side of Below Figure)

If the ATX PLL is in the bottom triplet, its drive span is all four GXT channels within its own bank and channels ch3 and ch4 from the bank below.



Related Information

- GXT Channels on page 21
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

1.1.4. Calibration

The transceiver is calibrated at device power on. The OSC_CLK_1 signal is used for device configuration and by transceiver calibration logic. OSC_CLK_1 must be driven by a free running 25 MHz, 100 MHz, or 125 MHz clock source if the transceiver tiles are used. The internal FPGA oscillator cannot be used for transceiver calibration.

The clock source must be stable at FPGA device configuration and should continue to run during device operation.

2. Tile Architecture Constraints

2.1. Transceiver Channel Placement

The Intel Stratix 10 product family introduces several transceiver tile variants to support a wide variety of protocol implementations.

Table 3. Channel Types

There are a total of 24 channels available per tile. You can configure them as either GX channels or as a combination of GX and (up to 16) GXT channels as long as the total does not exceed 24. You can use a GXT channel as a GX channel, but it would be subject to all of the GX channel placement constraints.

Feature	L-Tile Transceivers	H-Tile Transceivers
Maximum Datarate (Chip-to-chip)	GX [(2)]—17.4 Gbps	GX—17.4 Gbps GXT—28.3 Gbps
	GXT [(2)]—26.6 Gbps	
Maximum Datarate (Backplane)	GX and GXT—12.5 Gbps	

Related Information

L-Tile/H-Tile Building Blocks

2.1.1. Possible Combinations of GX and GXT Channels

Related Information

ATX PLL Usage Model When Driving GXT Channels on page 29

2.1.1.1. Possible Combinations of GX and GXT Channels in H-Tile

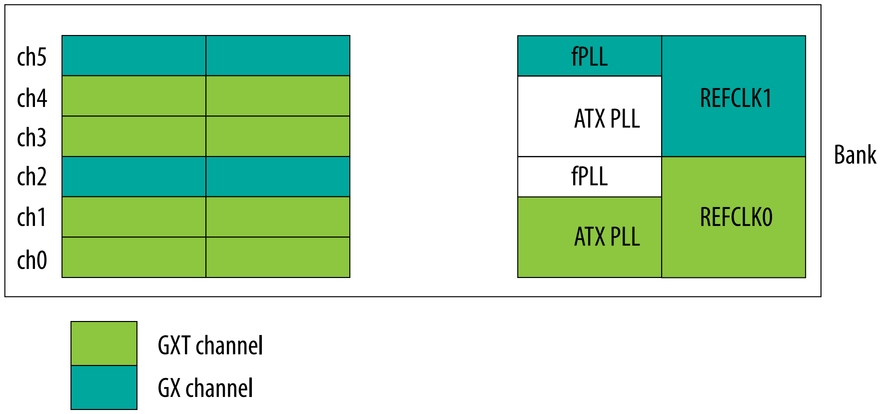
Table 4. Combination 1: 4 GXT and 2 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for H-Tile	
		Chip-to-Chip	Backplane
GX	2	12.5 Gbps	N/A
GXT [(3)]	4	28.3 Gbps	28.3 Gbps

(2) Refer to the *L-Tile/H-Tile Building Blocks* section for further descriptions of GX and GXT channels.

(3) If you use GXT channel data rates, the VCCR_GXB and VCCT_GXB voltages must be set to 1.12 V.

Figure 11. Example Combination 1: 4 GXT and 2 GX Channels

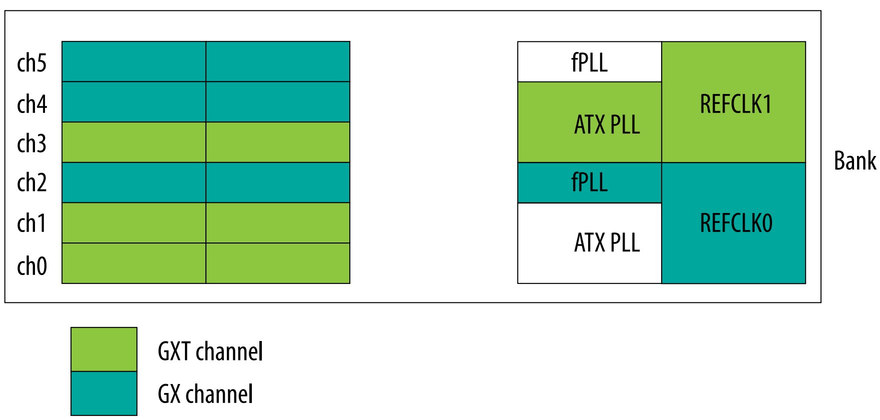


Note:
You cannot use ATX PLL for GX channels when using more than 2 GXT channels per bank

Table 5. Combination 2: 3 GXT and 3 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for H-Tile	
		Chip-to-Chip	Backplane
GX	3	12.5 Gbps	N/A
GXT (3)	3	28.3 Gbps	28.3 Gbps

Figure 12. Example Combination 2: 3 GXT and 3 GX Channels



Note:
You cannot use ATX PLL for GX channels when using more than 2 GXT channels per bank

Table 6. Combination 3: 2 GXT and 4 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for H-Tile	
		Chip-to-Chip	Backplane
GX	4	12.5 Gbps	N/A
GXT (3)	2	28.3 Gbps	28.3 Gbps

Figure 13. Example Combination 3: 2 GXT and 4 GX Channels

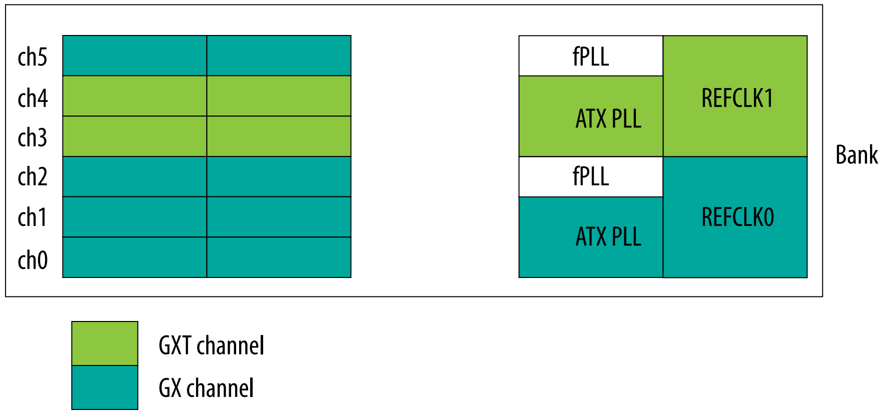
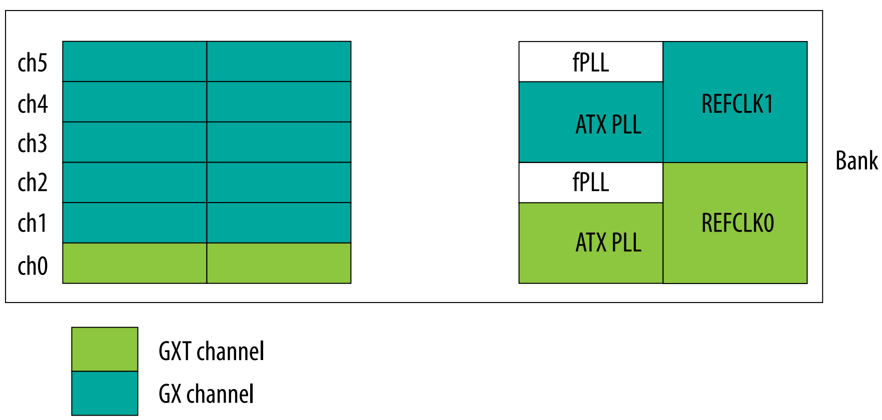


Table 7. Combination 4: 1 GXT and 5 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for H-Tile	
		Chip-to-Chip	Backplane
GX	5	12.5 Gbps	N/A
GXT (3)	1	28.3 Gbps	28.3 Gbps

Figure 14. Example Combination 4: 1 GXT and 5 GX Channels



Note:
You can place the single GXT channel in channel locations 0, 1, 3 or 4

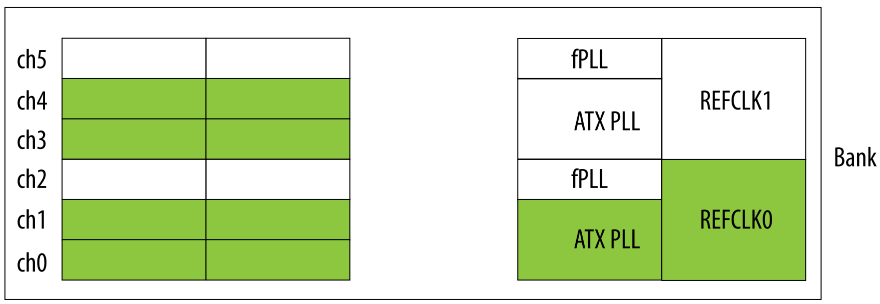
2.1.1.2. Possible Combinations of GX and GXT Channels in L-Tile

GXT channels are only supported in banks GXB1D/H/L and GXB4D/H/L and GXB1F/J/N and GXB4F/J/N.

Table 8. Combination 1: 4 GXT and 0 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for L-Tile	
		Chip-to-Chip	Backplane
GX	0	N/A	N/A
GXT [4]	4	26.6 Gbps	N/A

Figure 15. Example Combination 1: 4 GXT and 0 GX Channels



Note:
You cannot use ATX PLL for GX channels when using more than 2 GXT channels per bank

Table 9. Combination 2: 3 GXT and 1 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for L-Tile	
		Chip-to-Chip	Backplane
GX	1	12.5 Gbps	12.5 Gbps
GXT [4]	3	26.6 Gbps	N/A

(4) If you use GXT channel data rates, the VCCR_GXB and VCCT_GXB voltages must be set to 1.12 V.

Figure 16. Example Combination 2: 3 GXT and 1 GX Channels

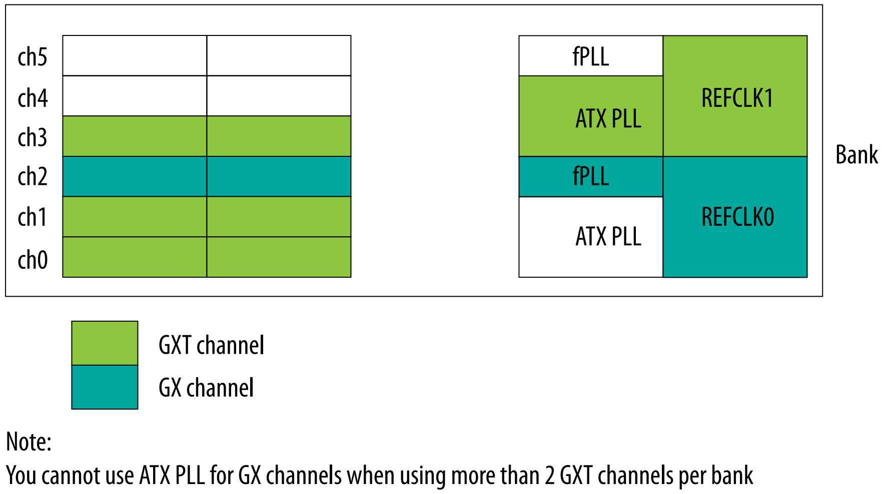


Table 10. Combination 3: 2 GXT and 2 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for L-Tile	
		Chip-to-Chip	Backplane
GX	2	12.5 Gbps	12.5 Gbps
GXT [(4)]	2	26.6 Gbps	N/A

Figure 17. Example Combination 3: 2 GXT and 2 GX Channels

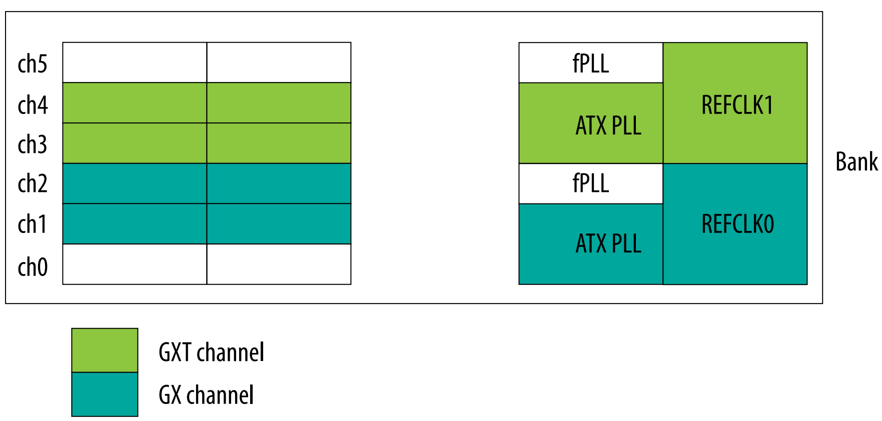
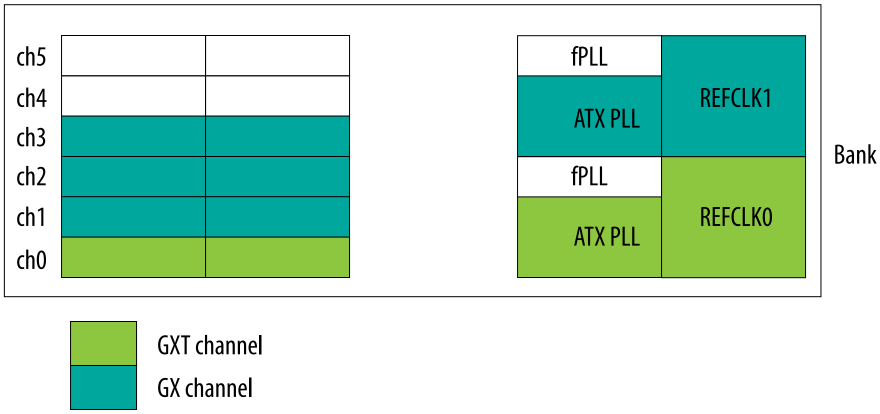


Table 11. Combination 4: 1 GXT and 3 GX Channels

Channel Type	Number of Channels per Bank	Channel Capability for L-Tile	
		Chip-to-Chip	Backplane
GX	3	12.5 Gbps	12.5 Gbps
GXT [(4)]	1	26.6 Gbps	N/A

Figure 18. Example Combination 4: 1 GXT and 3 GX Channels



Note:
You can place the single GXT channel in channel locations 0, 1, 3 or 4

2.1.2. GX Channels

The Intel Stratix 10 GX transceiver channels can support data rates up to 17.4 Gbps for chip-to-chip applications, and 12.5 Gbps for backplane applications.

The Intel Stratix 10 L-tile and H-tile transceiver clocking architecture supports both bonded and non-bonded transceiver channel configurations. Channel bonding is used to minimize the clock skew between multiple transceiver channels. For Intel Stratix 10 L-tile and H-tile transceivers, the term bonding you can refer to PMA bonding as well as PMA-PCS bonding.

2.1.2.1. Non-bonded GX Channels

Non-bonded channels can be placed anywhere within the transceiver tile.

Separate PHY IP cores, TX PLL, and REFCLK sources are required for each tile even if the transceivers are running at the same datarate with the same functionality.

2.1.2.2. Bonded GX Channels

Bonding across multiple transceiver tiles is not supported. All bonded channels must be placed within the same transceiver tile. A maximum of 24 channels can be bonded.

When PMA bonding is enabled, the channels do not need to be placed contiguously in the transceiver tile. When both PMA and PCS bonding are enabled, the channels must be placed contiguously in transceiver tile and in ascending order.

Figure 19. x4 Configuration

The figure below shows a way of placing 4 bonded channels. In this case, the logical PCS Master Channel number 2 must be specified as Physical channel 4 of bank 0.

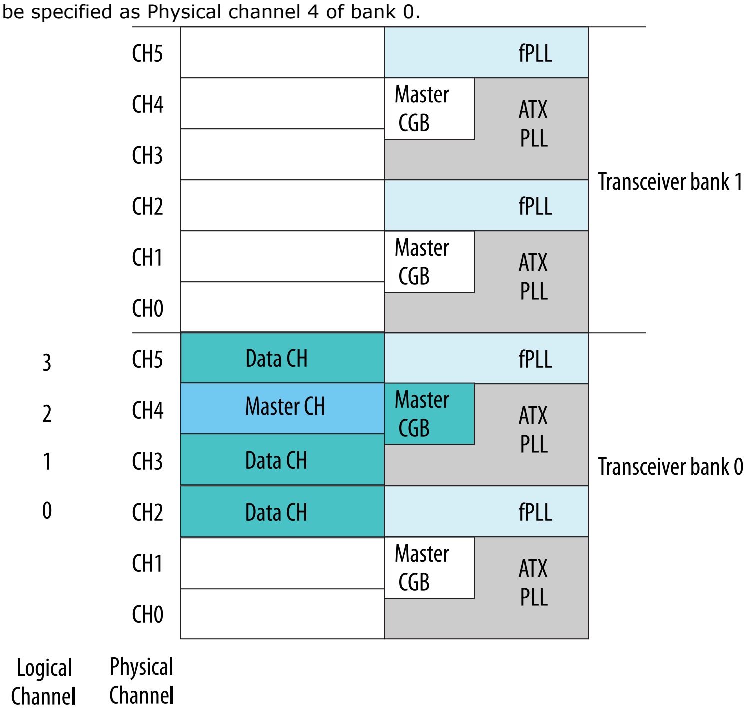
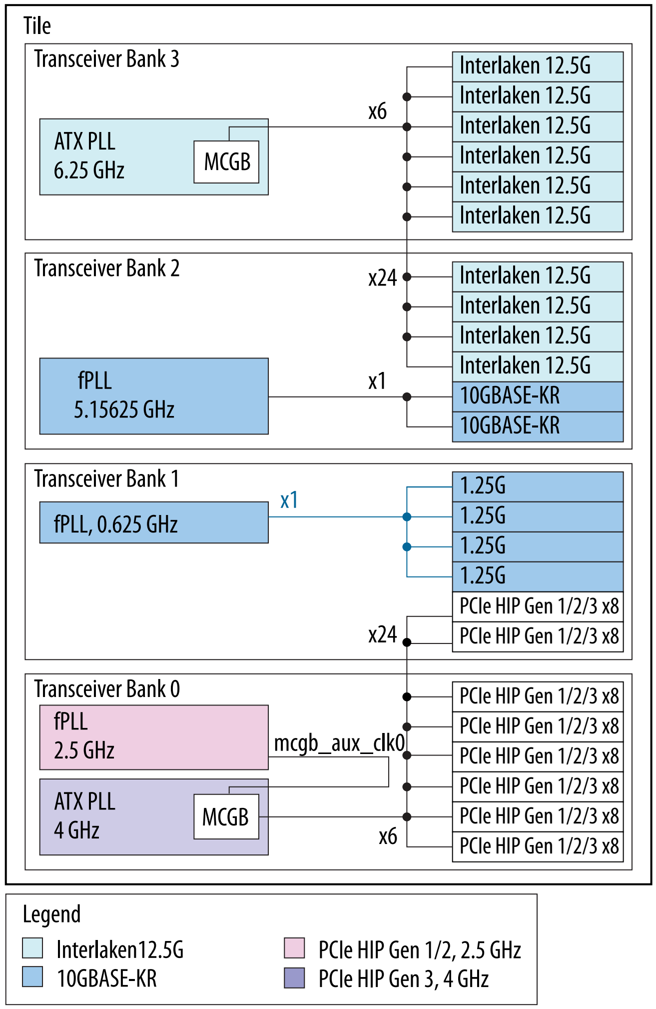


Figure 20. Mix and Match GX Channels Design Example

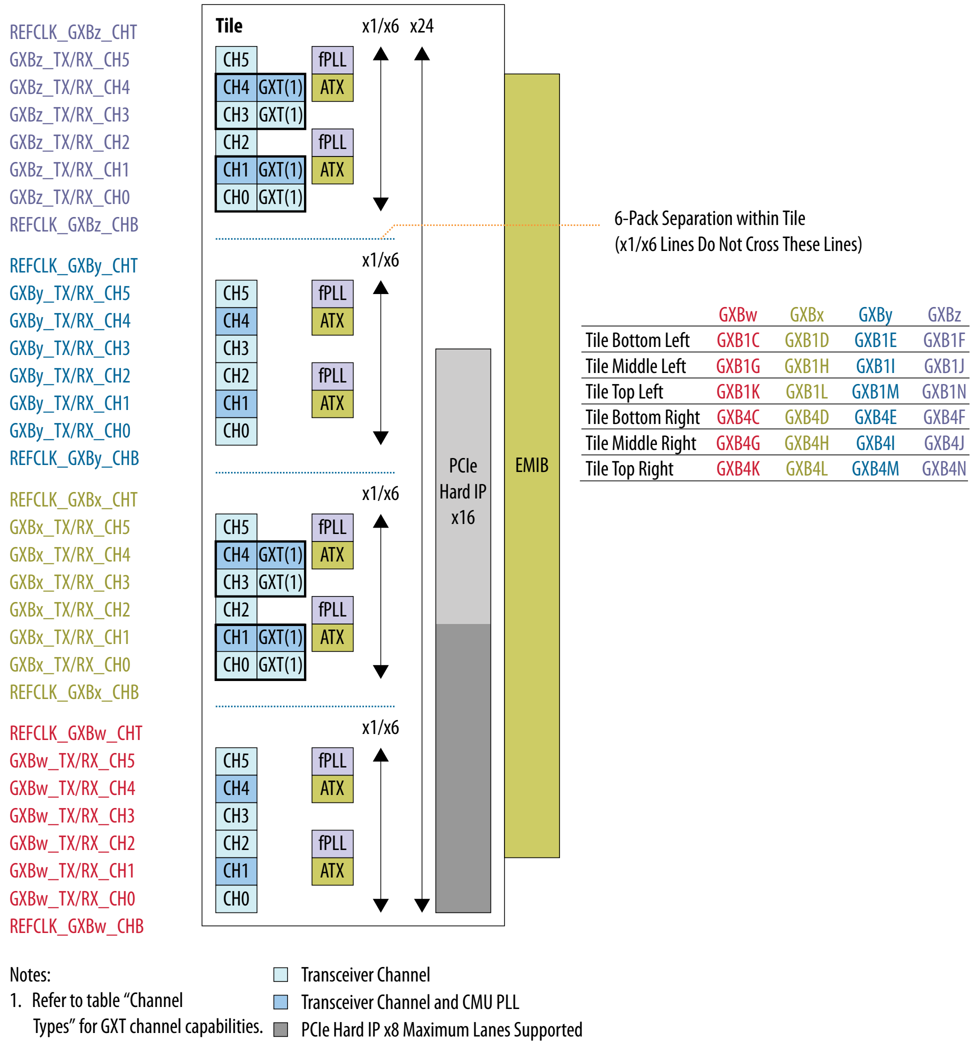
Example Intel Stratix 10 L-tile/H-tile, with Interlaken, 10GBaseKR, PCIe* transceivers instantiated.



2.1.3. GXT Channels

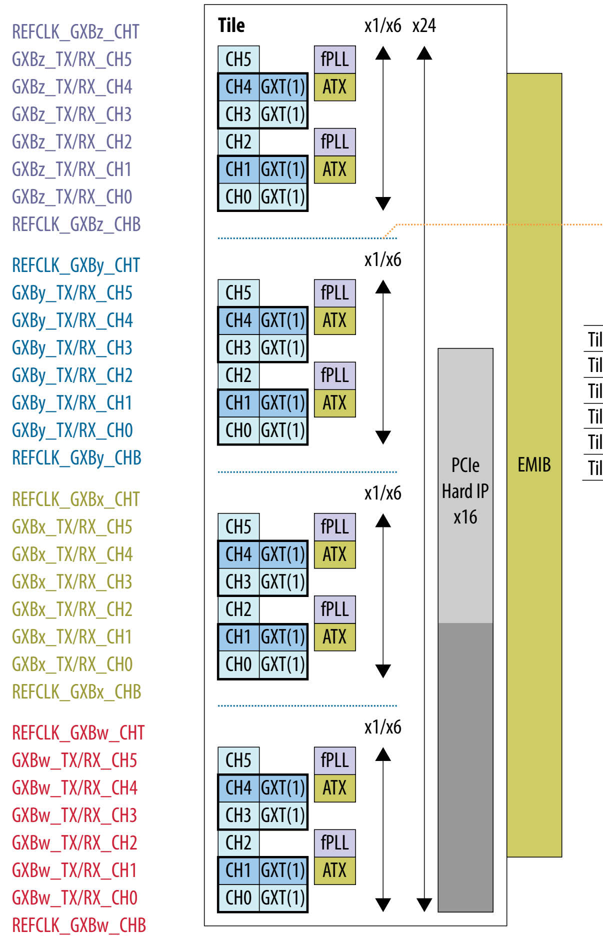
For more information on different channel types and the datarates supported by them, please refer to table "Channel Types" in *L-Tile and H-Tile Overview*.

Figure 21. Intel Stratix 10 L-Tile GXT Channel Location



	GXBw	GXBx	GXBy	GXBz
Tile Bottom Left	GXB1C	GXB1D	GXB1E	GXB1F
Tile Middle Left	GXB1G	GXB1H	GXB1I	GXB1J
Tile Top Left	GXB1K	GXB1L	GXB1M	GXB1N
Tile Bottom Right	GXB4C	GXB4D	GXB4E	GXB4F
Tile Middle Right	GXB4G	GXB4H	GXB4I	GXB4J
Tile Top Right	GXB4K	GXB4L	GXB4M	GXB4N

Figure 22. Intel Stratix 10 H-Tile GXT Channel Location



	GXBw	GXBx	GXBy	GXBz
Tile Bottom Left	GXB1C	GXB1D	GXB1E	GXB1F
Tile Middle Left	GXB1G	GXB1H	GXB1I	GXB1J
Tile Top Left	GXB1K	GXB1L	GXB1M	GXB1N
Tile Bottom Right	GXB4C	GXB4D	GXB4E	GXB4F
Tile Middle Right	GXB4G	GXB4H	GXB4I	GXB4J
Tile Top Right	GXB4K	GXB4L	GXB4M	GXB4N

Notes:
1. Refer to table "Channel Types" for GXT Channel Capabilities.

- Transceiver Channel
- Transceiver Channel and CMU PLL
- PCIe Hard IP x8 Maximum Lanes Supported

Figure 23. GXT and GX Channel Placement Example for L-Tile

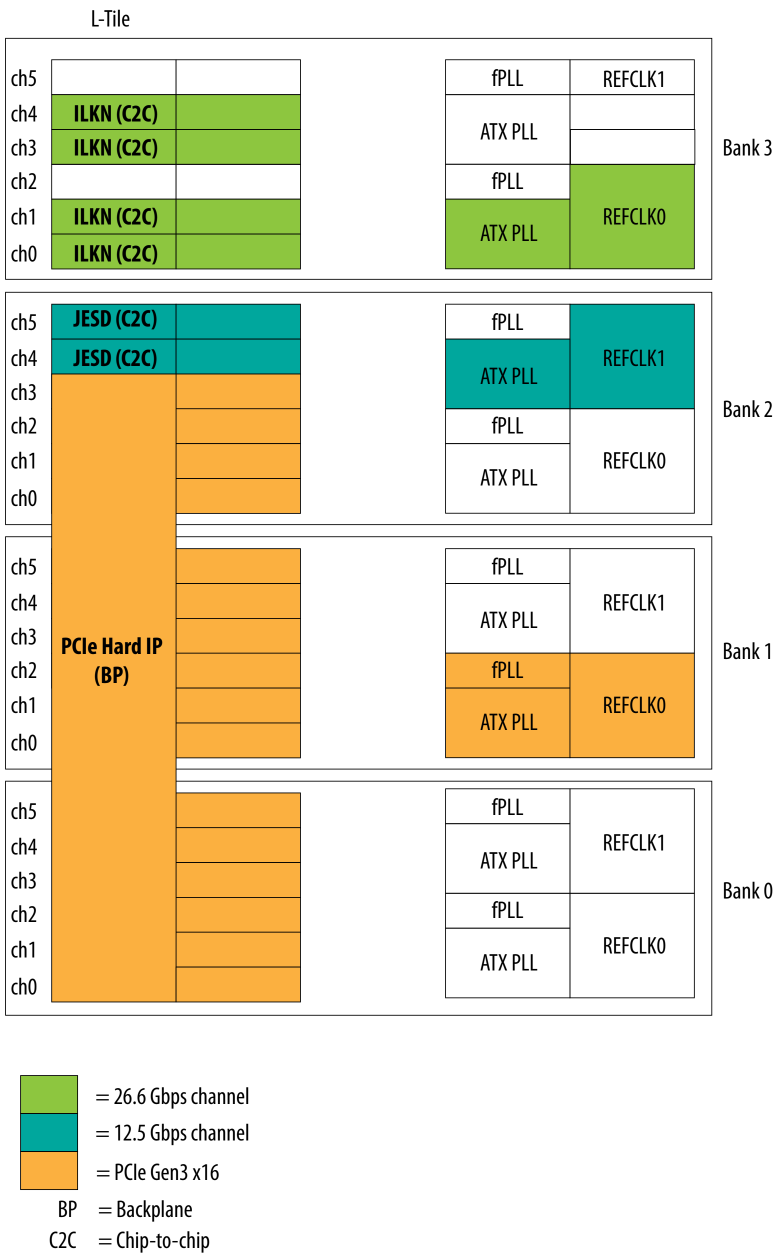


Figure 24. GXT and GX Channel Placement Example for H-Tile

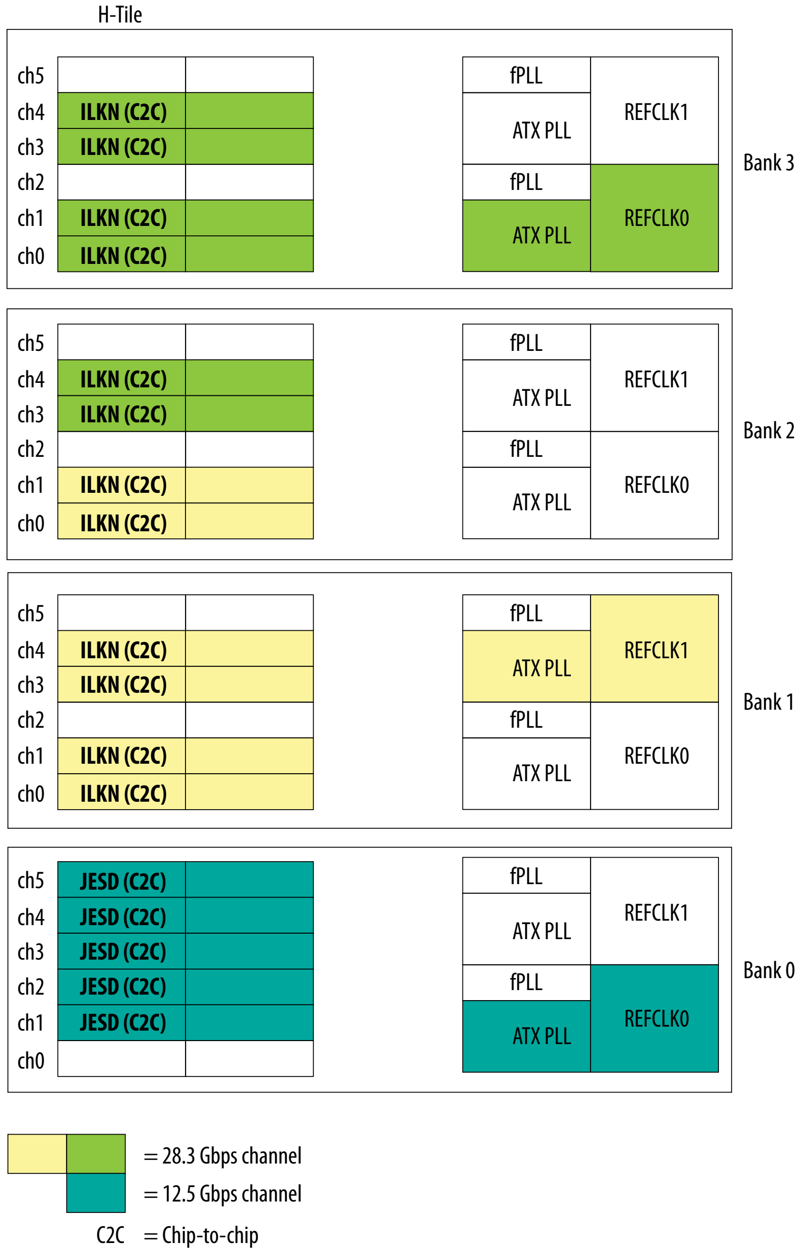
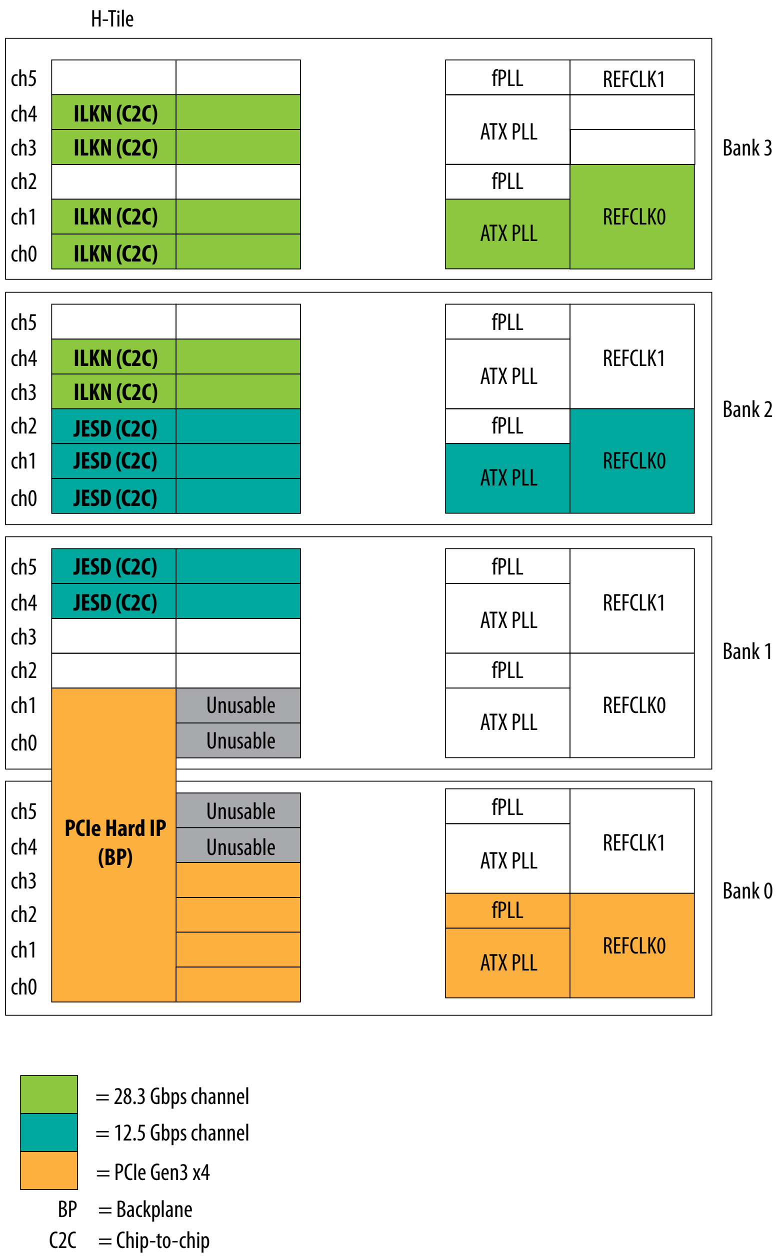


Figure 25. GXT and GX Channel Placement Example with PCIe Interface for H-Tile



Refer to the *Intel Stratix 10 Device Datasheet* for more information about performance specifications.

Related Information

- L-Tile and H-Tile Overview on page 3
- Intel Stratix 10 Device Datasheet

2.1.4. Reference Clock Guidelines for L-Tile and H-Tile

The transmitter PLL and the clock data recovery (CDR) block need an input reference clock source to generate the clocks required for transceiver operation. The input reference clock must be stable and free-running at device power-up for proper PLL calibrations.

Intel Stratix 10 L-tile and H-tile transceiver PLLs have five possible input reference clock sources, depending on jitter requirements:

- Dedicated reference clock pins
- Receiver input pins
- Reference clock network
- PLL cascade output (fPLL only)
- Core clock network (fPLL only)

Note: Each core clock network reference clock pin cannot drive fPLLs located on multiple L/H-tiles.

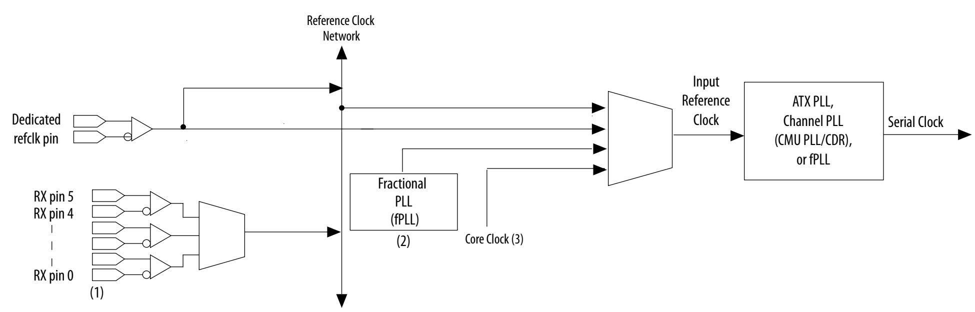
Intel recommends using the dedicated reference clock pins and the reference clock network for the best jitter performance.

For the best jitter performance, Intel recommends placing the reference clock as close as possible to the transmitter PLL. The following protocols require the reference clock to be placed in same bank as the transmitter PLL:

- OTU2e, OTU2, OC-192 and 10G PON
- 6G and 12G SDI

Note: For optimum performance of GXT channel, the reference clock of transmitter PLL is recommended to be from a dedicated reference clock pin in the same triplet.

Figure 26. Input Reference Clock Sources



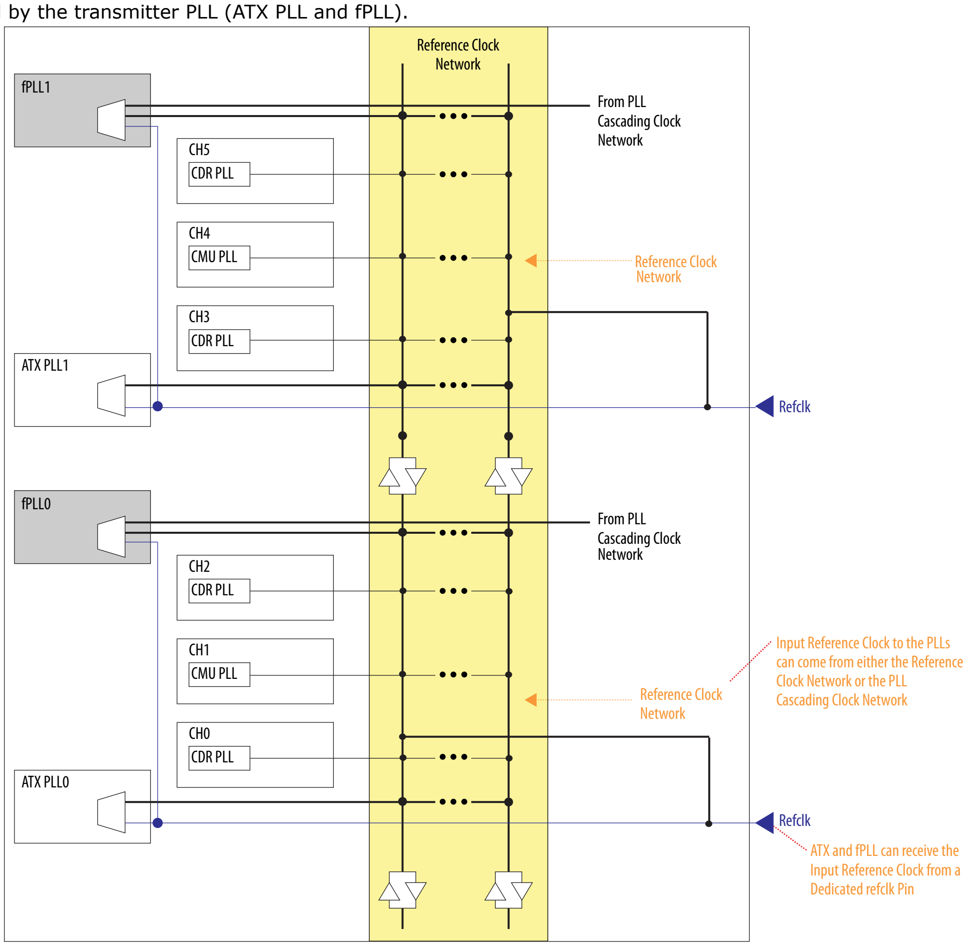
Note : (1) Any RX pin in the same bank can be used as an input reference clock.
(2) The output of another PLL can be used as an input reference clock source during PLL cascading. Intel Stratix 10 transceivers support fPLL to fPLL and ATX PLL to fPLL cascading. Refer to "PLL Cascading Clock Network" for more details on PLL cascading.
(3) Core Clock present only for fPLL.

Note: In Intel Stratix 10 devices, the FPGA fabric core clock network can be used as an input reference source for fPLL only.

The input reference clock is a differential signal. Intel recommends using the dedicated reference clock pin in the same bank as the transmitter PLL for optimal jitter performance. The input reference clock must be stable and free-running at device power-up for proper PLL operation and PLL calibration. If the reference clock is not available at device power-up, then PLL must be recalibrated when the reference clock is available.

Figure 27. Dedicated Reference Clock Pins and Other Reference Clock Sources

In Intel Stratix 10 L-tile and H-tile devices, dedicated reference clock pins and reference clock network can be used by the transmitter PLL (ATX PLL and fPLL).



Related Information

- Input Reference Clock Source
- Implementing PLL Cascading

2.1.5. PLL Placement

2.1.5.1. ATX PLL – fPLL Spacing Requirements

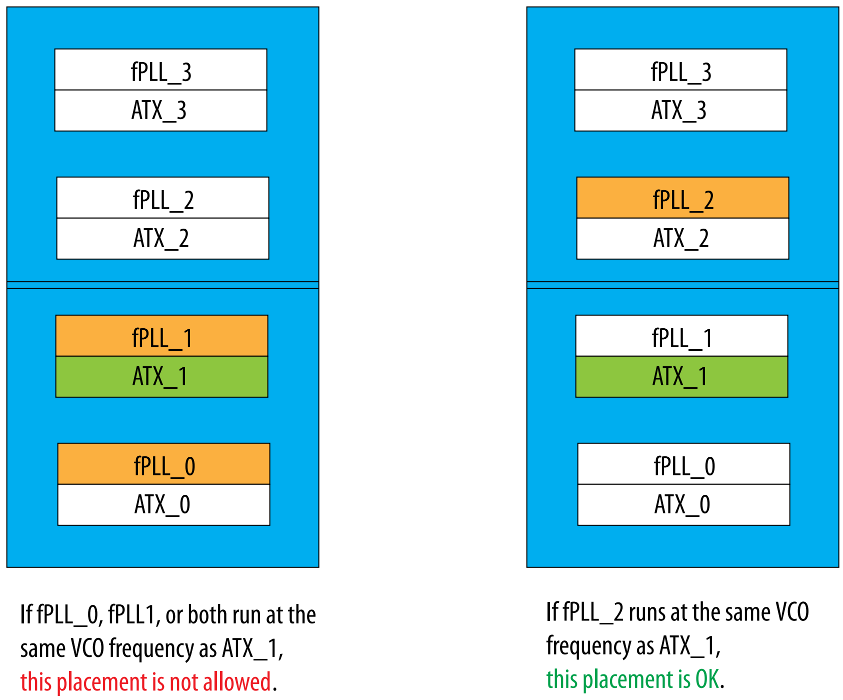
Table 12. ATX PLL - fPLL Spacing Requirements

When using ATX PLL and fPLL operating at the same VCO frequency or within 100 MHz, you must observe the spacing requirements listed in this table.

ATX PLL to fPLL Spacing	Spacing Requirement
ATX PLL to fPLL spacing	• Skip 1 ATX PLL OR • None if fPLL L counter ≥ 2

There are no ATX PLL placement restrictions between two different tiles.

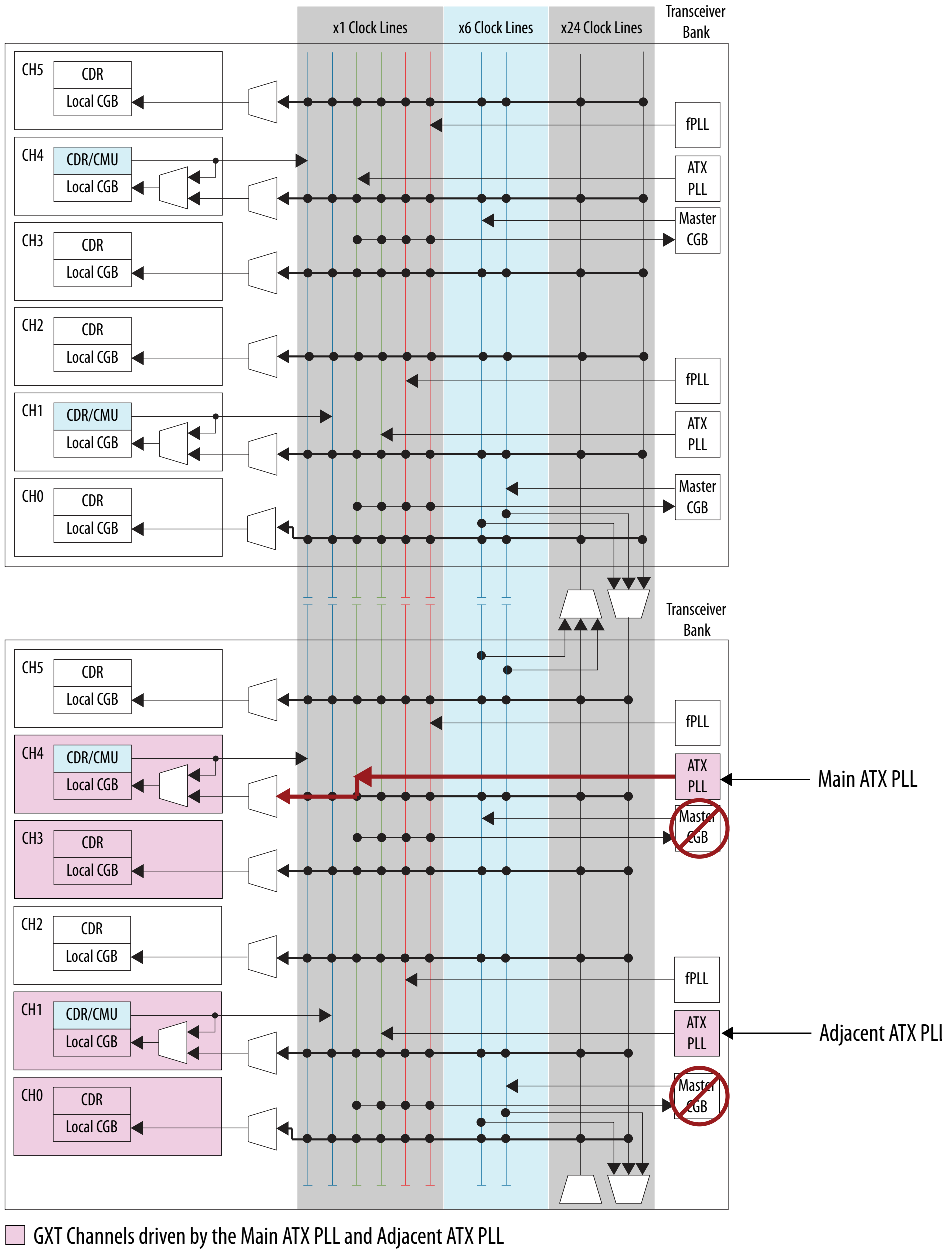
Figure 28. ATX PLL – fPLL Placement Example



2.1.5.2. ATX PLL Usage Model When Driving GXT Channels

- If ATX PLL IP is configured as the "Main ATX PLL" (Local ATX PLL output) the ATX PLL Master Clock Generation Block (MCGB) cannot be used.
- If ATX PLL IP is configured as an "Adjacent ATX PLL" (selecting input from ATX PLL below/above), the MCGB in the 3-pack cannot be used.
  — In the same 3-pack as a Main ATX PLL or Adjacent ATX PLL, the fPLL can be configured to drive the x1 clock lines.

Figure 29. Restrictions for ATX PLL GX and MCGB



Related Information

- Using the ATX PLL for GXT Channels
- GXT Implementation Usage Restrictions for ATX PLL GX & MCGB

2.1.5.3. Simplex Channel Merging

You can merge the following logical instances into a single physical channel:

- RX-only PHY and TX-only PHY instances (RX-only GXT and TX-only GX PHY instances cannot be merged into the same physical channel location.)
- CMU PLL and TX-only PHY instances

Figure 30. Simple Channel Merging: RX-only PHY and TX-only PHY

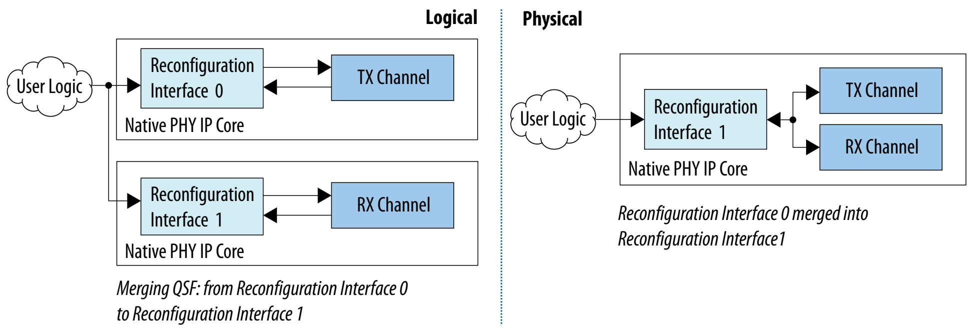
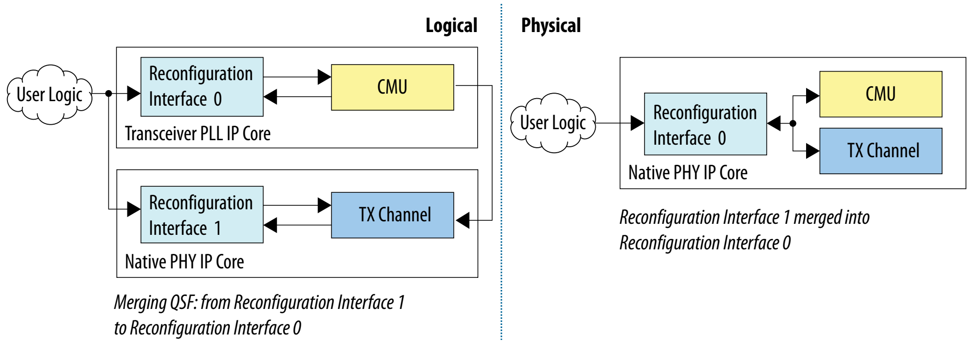


Figure 31. Channel Merging: CMU PLL and TX-only PHY instances



Rules for Merging

- Reconfiguration interface (reconfig_*) of both instances to be merged must be driven by the same source.
- QSF assignments are needed to specify which two reconfiguration interfaces you want to merge.
  — *Option 1: Using reconfiguration interface names*
    - ```
      set_instance_assignment -name XCVR_RECONFIG_GROUP 0 -to
      topdesign:topdesign_inst|<TX only instance
      name>*ct1_hssi_avmm1_if_inst->inst_ct1_xcvr_avmm1
      ```
    - ```
      set_instance_assignment -name XCVR_RECONFIG_GROUP 0 -to
      topdesign:topdesign_inst|<RX only instance
      name>*ct1_hssi_avmm1_if_inst->inst_ct1_xcvr_avmm1
      ```
  — *Option 2: Using pin names*
    - set_instance_assignment -name XCVR_RECONFIG_GROUP 0 –to **tx[0]**
    - set_instance_assignment -name XCVR_RECONFIG_GROUP 0 –to **rx[0]**

- The simplex channels cannot be merged if any of the following options are enabled in one or both simplex instances:
  - Native PHY Debug Master Endpoint (NPDME)
  - Optional reconfiguration logic
  - Embedded reconfiguration streamer
  - Shared reconfiguration interface

Related Information

Reconfiguration Interface and Dynamic Reconfiguration

2.1.5.4. TX PLL Restrictions when Using PCIe

Intel recommends driving the remaining channels of the L-tile by ATX PLL if 4 or more channels of PCIe are used at Gen2 or Gen3 speeds. Using ATX PLL to drive these channels helps achieve better performance. Intel Quartus® Prime issues a critical warning if fPLL is used to drive the remaining channels.

2.2. Unsupported Dynamic Reconfiguration Features

The following is a list of the unsupported dynamic reconfiguration features:

- Reconfiguration from a bonded configuration to a non-bonded configuration, or vice versa
- Reconfiguration from a bonded protocol to another bonded protocol
- Reconfiguration from PCIe (with Hard IP) to PCIe (without Hard IP), or non-PCIe bonded protocol switching
- Master clock generation block (MCGB) reconfiguration
- Switching between two master CGBs
- Serialization factor changes on bonded channels
- TX PLL switching on bonded channels

2.3. Intel Stratix 10 L-Tile Transceiver to H-Tile Transceiver Migration

All of the L-tile transceiver constraints apply to H-tile transceivers as well. The H-tile transceivers have no further restrictions than the L-tile transceivers, with the exception of the GXT channels.

If you plan to use GXT channels in the H-tile, the V_{CCR_GXB} and V_{CCT_GXB} pins on that tile must be set to 1.12 V.

Note: When migrating from L-tile to H-tile transceivers, use the Intel Stratix 10 Power and Thermal Calculator (PTC) tool to validate your regulator sizing.

The placement constraints for the GXT channels are mentioned in the *GXT Channels* section.

Related Information

GXT Channels on page 21

2.4. Thermal Guidelines

Optimal thermal performance can be achieved by reducing the power density within the transceiver tile. Placing many high data rate channels next to each other results in high power density areas within a tile. Following a general guideline of minimizing power density results in a less complex, and cheaper cooling solution for the FPGA.

For best thermal performance you can minimize power density by picking transceiver channel locations early on. Follow these guidelines when placing your transceiver channels within a tile:

- Spread out channels as much as possible
- If all channels in a tile are used, intersperse low and high data rate channels
- The middle of the tile has the best thermal performance, followed by the bottom and then the top of each tile when looking at the Pin Planner

The latest Intel Stratix 10 Power and Thermal Calculator (PTC) contains a Thermal worksheet to help you determine the impact of transceiver placement on your thermal solution requirements. Prior to finalizing your board design you should analyze your transceiver channel placement using the Intel Stratix 10 PTC to ensure it is thermally optimal.

Note: Contact your local FAE to have Intel run a thermal analysis of your board design after you have determined placement of all transceiver channels.

3. PCIe Guidelines

3.1. PCIe Hard IP

There is one PCIe Hard IP available per transceiver tile.

3.1.1. Channel Placement for PCIe Hard IP

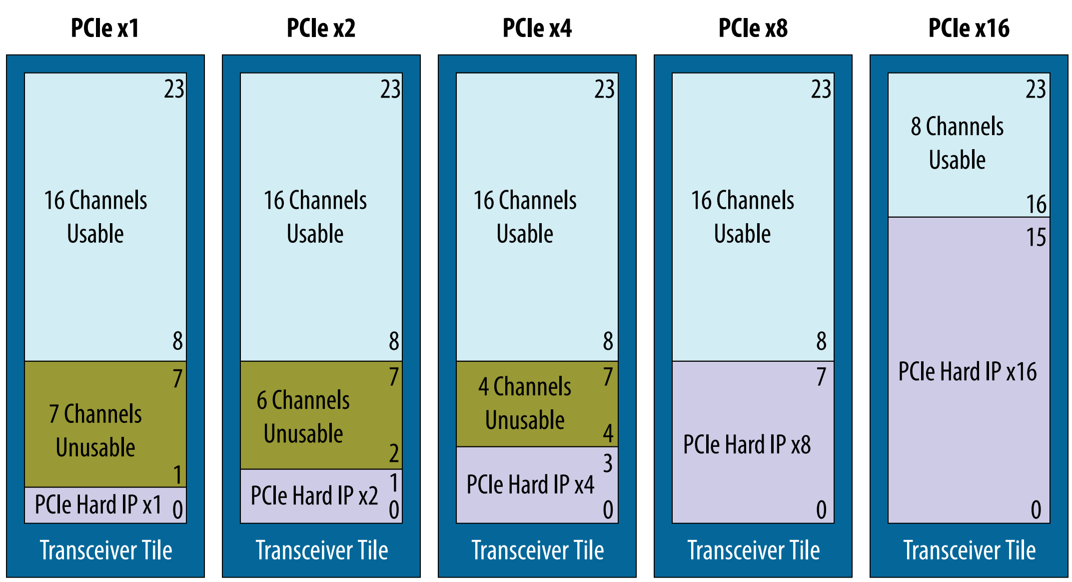
The PCIe lane 0 is always mapped to ch0 of the transceiver tile. Channel 0 of the transceiver tile = Bank 0, Channel 0.

The PCIe x1, x2, x4 and x8 configurations always consume a total of eight transceiver channels.

CvP Support

Only the bottom left transceiver tile supports configuration via protocol (CvP).

Figure 32. Transceiver Channel Usage for PCIe x1, X2, x4, x8 and x16



3.1.2. PLL Placement for PCIe Hard IP

If the PCIe Hard IP is configured as Gen1/Gen2 capable IP, the fPLL is used as a transmitter PLL.

If the PCIe Hard IP is configured as Gen3 capable IP, then

- fPLL is used as a transmitter PLL when running at Gen1/Gen2 speeds.
- ATX PLL is used as a transmitter PLL when running at Gen3 speeds.

Figure 33. PLL Placement for Gen1 and Gen2 x1/ x2/ x4/ x8

fPLL1	PMA Channel 5	PCS Channel 5		
ATXPLL1	PMA Channel 4	PCS Channel 4		
	PMA Channel 3	PCS Channel 3		
fPLL0	PMA Channel 2	PCS Channel 2		
ATXPLL0	PMA Channel 1	PCS Channel 1		
	PMA Channel 0	PCS Channel 0		
fPLL1	PMA Channel 5	PCS Channel 5		
ATXPLL1	PMA Channel 4	PCS Channel 4		
	PMA Channel 3	PCS Channel 3	Ch 15	PCIe Hard IP
fPLL0	PMA Channel 2	PCS Channel 2	Ch 14	
ATXPLL0	PMA Channel 1	PCS Channel 1	Ch 13	
	PMA Channel 0	PCS Channel 0	Ch 12	
fPLL1	PMA Channel 5	PCS Channel 5	Ch 11	
ATXPLL1	PMA Channel 4	PCS Channel 4	Ch 10	
	PMA Channel 3	PCS Channel 3	Ch 9	
fPLL0	PMA Channel 2	PCS Channel 2	Ch 8	
ATXPLL0	PMA Channel 1	PCS Channel 1	Ch 7	
	PMA Channel 0	PCS Channel 0	Ch 6	
fPLL1	PMA Channel 5	PCS Channel 5	Ch 5	
ATXPLL1	PMA Channel 4	PCS Channel 4	Ch 4	
	PMA Channel 3	PCS Channel 3	Ch 3	HRC connects to fPLL0
fPLL0	PMA Channel 2	PCS Channel 2	Ch 2	
ATXPLL0	PMA Channel 1	PCS Channel 1	Ch 1	
	PMA Channel 0	PCS Channel 0	Ch 0	

Figure 34. PLL Placement for Gen1 and Gen2 x16

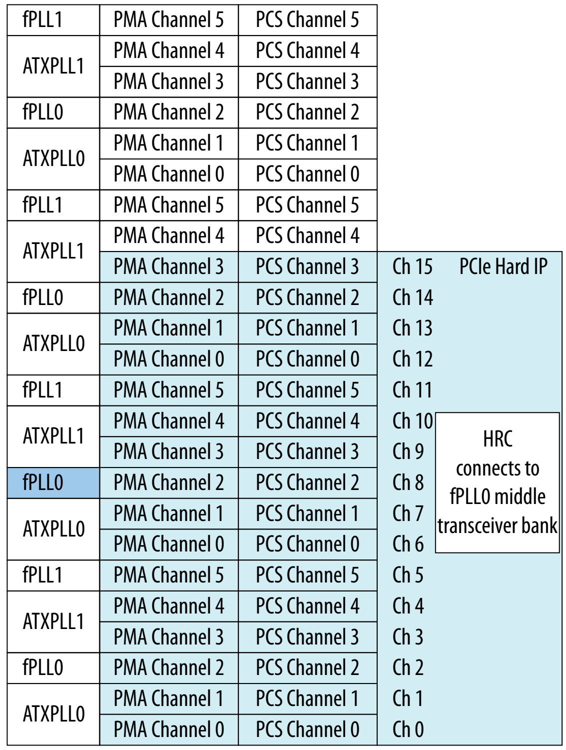


Figure 35. PLL Placement for Gen3 x1/x2/x4/x8

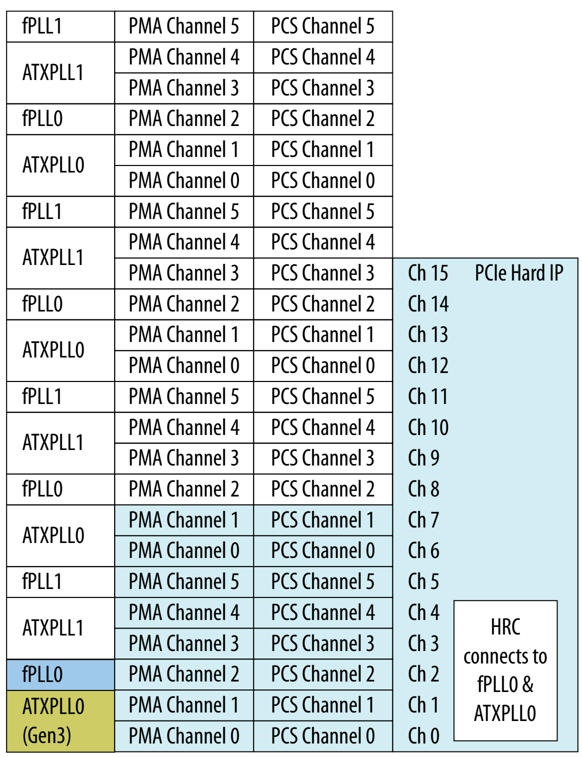


Figure 36. PLL Placement for Gen3 x16

fPLL1	PMA Channel 5	PCS Channel 5		
ATXPLL1	PMA Channel 4	PCS Channel 4		
	PMA Channel 3	PCS Channel 3		
fPLL0	PMA Channel 2	PCS Channel 2		
ATXPLL0	PMA Channel 1	PCS Channel 1		
	PMA Channel 0	PCS Channel 0		
fPLL1	PMA Channel 5	PCS Channel 5		
ATXPLL1	PMA Channel 4	PCS Channel 4		
	PMA Channel 3	PCS Channel 3	Ch 15	PCIe Hard IP
fPLL0	PMA Channel 2	PCS Channel 2	Ch 14	
ATXPLL0	PMA Channel 1	PCS Channel 1	Ch 13	
	PMA Channel 0	PCS Channel 0	Ch 12	
fPLL1	PMA Channel 5	PCS Channel 5	Ch 11	
ATXPLL1	PMA Channel 4	PCS Channel 4	Ch 10	HRC connects to fPLL0 & ATXPLL1 middle transceiver bank
	PMA Channel 3	PCS Channel 3	Ch 9	
fPLL0	PMA Channel 2	PCS Channel 2	Ch 8	
ATXPLL0 (Gen3)	PMA Channel 1	PCS Channel 1	Ch 7	
	PMA Channel 0	PCS Channel 0	Ch 6	
fPLL1	PMA Channel 5	PCS Channel 5	Ch 5	
ATXPLL1	PMA Channel 4	PCS Channel 4	Ch 4	
	PMA Channel 3	PCS Channel 3	Ch 3	
fPLL0	PMA Channel 2	PCS Channel 2	Ch 2	
ATXPLL0	PMA Channel 1	PCS Channel 1	Ch 1	
	PMA Channel 0	PCS Channel 0	Ch 0	

TX PLL Guidelines When Using PCIe

1. The remaining channels of the L-tile are recommended to be driven by ATX PLL if 4 or more channels of PCIe are used at Gen2 or Gen3 speeds. Using ATX PLL to drive these channels helps achieve better performance. Intel Quartus Prime issues a critical warning if fPLL is used to drive the remaining channels.

Table 13. TX PLL Guidelines When Using PCIe

PCIE CONFIG	Recommended PLL selection for remaining channels
PCIE GEN 1 (All lane widths)	Any PLL
PCIE GEN 2 (x4,x8,x16)	ATX PLL(5)
PCIE GEN 3 (x4,x8,x16)	ATX PLL(5)

2. When instantiating PIPE interfaces and PCIe Hard IP in the same transceiver tile, be aware of ATX PLL and ATX-fPLL spacing rules. For more details refer to *PLL Placement* section.

Related Information

PLL Placement on page 29

(5) Quartus issues a critical warning if FPLL is used instead of ATX PLL.

3.2. PHY Interface for PCIe Express (PIPE)

This can be used when you want flexible channel placement or to interface the Intel Stratix 10 PCIe PHY with existing 3rd party PCIe IP cores.

3.2.1. Channel Placement for PIPE

For L-tile, any transceiver channel running at data rate above 6.5 Gbps that shares a tile with an active PCI Express interface that are Gen2 or Gen3 capable and configured with more than 2 lanes (Gen2/3 x4, x8, x16) may observe momentary bit errors (BER) during a PCI Express rate change event (PCIe link training both up and down, i.e., link down and start of link training). Transceiver channels that share a tile with active PCI Express interfaces that are only Gen1 capable are not impacted.

For details on channel placement for PIPE, refer to the section "How to place channels for PIPE configurations" in *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*.

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

3.2.2. PLL Placement for PIPE

When instantiating PIPE interfaces and PCIe Hard IP in the same transceiver tile, be aware of ATX PLL and ATX-fPLL spacing rules. For more details refer to *PLL Placement* section.

TX PLL Guidelines When Using PCIe

1. Intel recommends that the remaining channels of the L-tile are to be driven by ATX PLL if 4 or more channels of PCIe are used at Gen2 or Gen3 speeds. Using ATX PLL to drive these channels helps achieve better performance. Intel Quartus Prime issues a critical warning if fPLL is used to drive the remaining channels.

Table 14. TX PLL Guidelines When Using PCIe

PCIE CONFIG	Recommended PLL selection for remaining channels
PCIE GEN 1 (All lane widths)	Any PLL
PCIE GEN 2 (x4,x8,x16)	ATX PLL(6)
PCIE GEN 3 (x4,x8,x16)	ATX PLL(6)

2. For details on PLL placement for PIPE, refer to the section "How to Connect TX PLLs for PIPE Gen1, Gen2, and Gen3 Modes" in *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*.

Related Information

- PLL Placement on page 29
- How to Connect TX PLLs for PIPE Gen1, Gen2, and Gen3 Modes
- Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

(6) Intel Quartus Prime issues a critical warning if FPLL is used instead of ATX PLL.

4. Document Revision History for AN 778: Intel Stratix 10 L-Tile/H-Tile Transceiver Usage

Document Version	Changes
2020.04.21	Made the following changes: • Changed ADME to NPDME. • Updated PCIe hard IP and PIPE spacing requirements for H-tile. • Updated to apply to Intel Stratix 10 L-tile/H-tile production devices only.
2018.07.13	Made the following changes: • Updated the "ATX PLL Block Diagram" figure to clearly show that cascaded input from an upstream PLL is not supported. • Added "These combinations are only applicable for banks GXB1D/H/L and GXB4D/H/L and GXB1F/J/N and GXB4F/J/N." note to *Possible Combinations of GX and GXT Channels in L-Tile*.
2017.11.06	Made the following changes: • Updated the "Channel Types" table to include L-Tile channels • Updated the "ATX PLL Spacing Requirements" and "ATX PLL-fPLL Spacing Requirements" table • Updated the "Thermal Guidelines" section • Made the following updates in the "Mix and Match GX Channels Design Example" diagram: — Changed PCIe Gen 1/2/3 x8 to PCIe HIP Gen 1/2/3x8 — Changed PCIe Gen 1/2 , 2.5 GHz to PCIe HIP Gen 1/2 , 2.5 GHz — Changed PCIe Gen 3, 4 GHz to PCIe HIP Gen 3, 4 GHz • Updated the description for "TX PLL Restrictions when Using PCIe x16" topic • Updated the description for "PCIe Hard IP Placement" topic • Restrictions stated when one or more channels in a bank are used for PCIe/PIPE Gen3 • Updated steps in "How to Place Channels for PIPE Configurations" topic • Changed value of Logical PCS Master Channel # from 1 to 0 in "Logical PCS Master Channel for PIPE Configuration" table • Added a note "Each core clock network reference clock pin cannot drive fPLLs located on multiple L/H-Tiles" • Added a new diagram "x4 Configuration" in "Bonded GX Channels" topic to explain the ascending order of the channel placement
2017.01.13	Made the following change: • Added a new section: ATX PLL GXT Channels Placement
2016.12.19	Made the following changes: • Clarified the ATX PLL spacing requirements and listed them in the "ATX PLL Spacing Requirements" table.
2016.09.20	Initial release