Altera JESD204B IP Core and ADI AD6676 Hardware Checkout Report

2015.11.02

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The Altera JESD204B IP Core is a high-speed point-to-point serial interface intellectual property (IP).

The JESD204B IP Core has been hardware-tested with a number of selected JESD204B-compliant ADC (analog-to-digital converter) devices.

This report highlights the interoperability of the JESD204B IP Core with the AD6676 converter evaluation module (EVM) from Analog Devices Inc. (ADI). The following sections describe the hardware checkout methodology and test results.

Related Information

- **JESD204B IP Core User Guide**
- **ADI AD6676 Evaluation Module**

Hardware Requirements

The hardware checkout test requires the following hardware and software tools:

- Arria 10 GX FPGA Development Kit
- ADI AD6676 EVM
- Mini-USB cable
- SMA cable
- Clock source card capable of providing external SMA reference clock to the EVM `CLKIN` (J5).

Hardware Setup

An Arria 10 GX FPGA Development Kit is used with the ADI AD6676 daughter card module installed on the development board's FMC connector.

- For FMC port B in the Arria10 GX FPGA Development Kit, apply a jumper at pin 5-6 of J8 to set the adjustable voltage to 1.8 V.
- The AD6676 EVM derives power from the Arria 10 FMC connector.
- An external reference clock can be fed into the ADC EVM for the ADC device clock. To use an external reference clock, remove R95 and R100 on the AD6676 EVM.
- Both the FPGA and ADC device clock must be sourced from the same clock source card.
- The ADC EVM buffers the external reference clock and sends it to the FPGA as the device clock.
- For subclass 1, the FPGA generates SYSREF for the JESD204B IP Core as well as the AD6676 device.

Figure 1: Hardware Setup

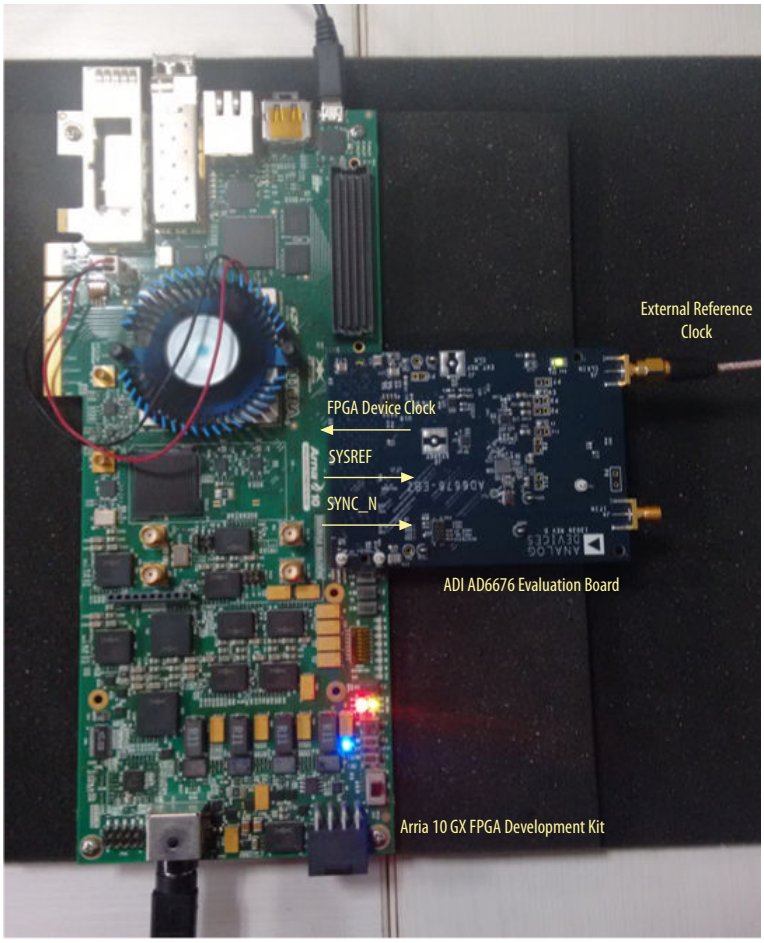
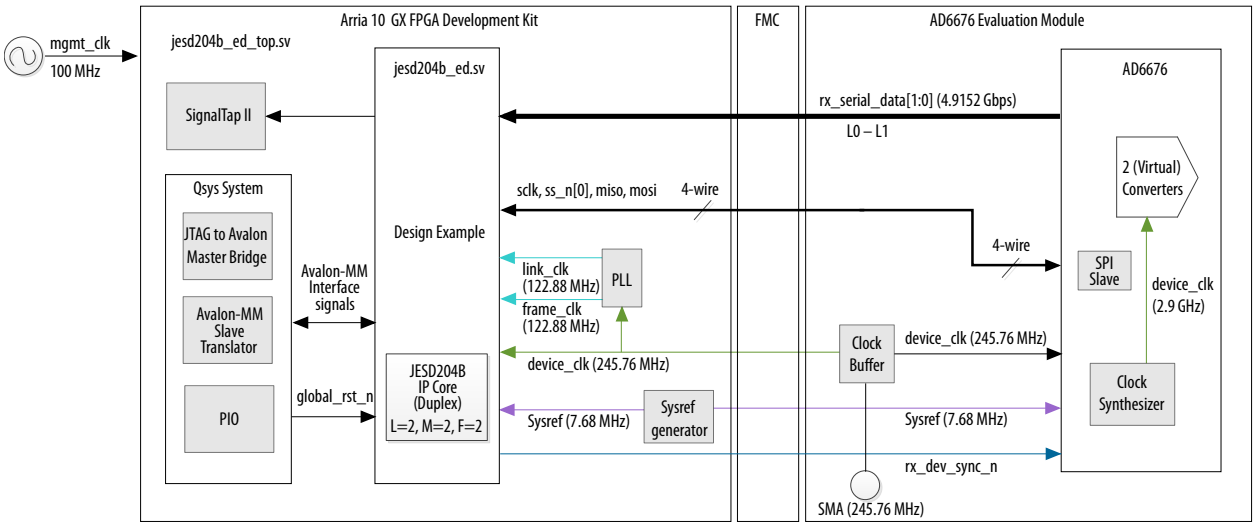


Figure 2: System-Level Block Diagram



The system-level diagram shows how different modules connect in this design.

In this setup, where LMF=222, the data rate of transceiver lanes is 4.9152 Gbps. An external reference clock of 245.76 MHz is sourced to the AD6676 EVM through the SMA. The EVM buffers the reference clock and provides the same device clock to the FPGA and AD6676. The ADC has an on-chip internal clock synthesizer that uses the reference clock to generate a 2.94912-GHz sampling clock to the converter.

Hardware Checkout Methodology

The following sections describe the test objectives, procedure, and the passing criteria. The test covers the following areas:

- Receiver data link layer
- Receiver transport layer
- Descrambling
- Deterministic latency (Subclass 1)

Receiver Data Link Layer

This test area covers the test cases for code group synchronization (CGS) and initial frame and lane synchronization.

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The SignalTap II Logic Analyzer tool monitors the receiver data link layer operation.

Code Group Synchronization (CGS)

Table 1: CGS Test Cases

Test Case	Objective	Description	Passing Criteria
CGS.1	Check whether sync request is deasserted after correct reception of four successive /K/ characters.	The following signals in <*ip_variant_name*>_**inst_phy.v** are tapped: • `jesd204_rx_pcs_data[(L*32)-1:0]` • `jesd204_rx_pcs_data_valid[L-1:0]` • `jesd204_rx_pcs_kchar_data[(L*4)-1:0]` The following signals in <*ip_variant_name*>**.v** are tapped: • `rx_dev_sync_n` • `jesd204_rx_int` The `rxlink_clk` signal is used as the SignalTap II sampling clock. Each lane is represented by a 32-bit data bus in the `jesd204_rx_pcs_data` signal. The 32-bit data bus is divided into 4 octets.	• /K/ character or K28.5 (0xBC) is observed at each octet of the `jesd204_rx_pcs_data` bus. • The `jesd204_rx_pcs_data_valid` signal is asserted to indicate data from the PCS is valid. • The `jesd204_rx_pcs_kchar_data` signal is asserted whenever control characters like /K/, /R/, /Q/ or /A/ characters are observed. • The `rx_dev_sync_n` signal is deasserted after correct reception of at least four successive /K/ characters. • The `jesd204_rx_int` signal is deasserted if there is no error.
CGS.2	Check full CGS at the receiver after correct reception of another four 8B/10B characters.	The following signals in <*ip_variant_name*>_**inst_phy.v** are tapped: • `jesd204_rx_pcs_errdetect[(L*4)-1:0]` • `jesd204_rx_pcs_disperr[(L*4)-1:0]` (1) The following signal in <*ip_variant_name*>**.v** is tapped: • `jesd204_rx_int` The `rxlink_clk` signal is used as the SignalTap II sampling clock.	The `jesd204_rx_pcs_errdetect`, `jesd204_rx_pcs_disperr`, and `jesd204_rx_int` signals should not be asserted during CGS phase.

(1) L indicates the number of lanes.

Initial Frame and Lane Synchronization

Table 2: Initial Frame and Lane Synchronization Test Cases

Test Case	Objective	Description	Passing Criteria
ILA.1	Check whether the initial frame synchronization state machine enters FS_DATA state upon receiving non /K/ characters.	The following signals in <*ip_variant_name*>**_inst_phy.v** are tapped: • `jesd204_rx_pcs_data[(L*32)-1:0]` • `jesd204_rx_pcs_data_valid[L-1:0]` • `jesd204_rx_pcs_kchar_data[(L*4)-1:0]` The following signals in <*ip_variant_name*>**.v** are tapped: • `rx_dev_sync_n` • `jesd204_rx_int` The `rxlink_clk` signal is used as the SignalTap II sampling clock. Each lane is represented by a 32-bit data bus in the `jesd204_rx_pcs_data` signal. The 32-bit data bus is divided into 4 octets.	• /R/ character or K28.0 (0x1C) is observed after /K/ character at the `jesd204_rx_pcs_data` bus. • The `jesd204_rx_pcs_data_valid` signal must be asserted to indicate that data from the PCS is valid. • The `rx_dev_sync_n` and `jesd204_rx_int` signals are deasserted. • Each multiframe in ILAS phase ends with /A/ character or K28.3 (0x7C). • The `jesd204_rx_pcs_kchar_data` signal is asserted whenever control characters like /K/, /R/, /Q/ or /A/ characters are observed.

(2) L indicates the number of lanes.

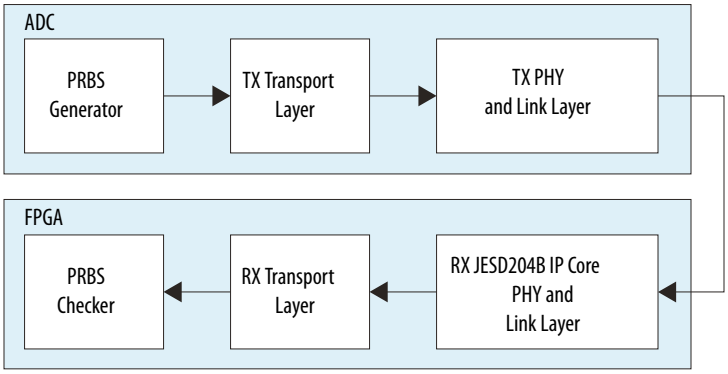
Test Case	Objective	Description	Passing Criteria
ILA.2	Check the JESD204B configuration parameters from the ADC in the second multiframe.	The following signals in <*ip_variant_name*>**_inst_phy.v** are tapped: • `jesd204_rx_pcs_data[(L*32)-1:0]` • `jesd204_rx_pcs_data_valid[L-1:0]` (2) The following signal in <*ip_variant_name*>**.v** is tapped: • `jesd204_rx_int` The `rxlink_clk` signal is used as the SignalTap II sampling clock. The system console access the following registers: • `ilas_octet0` • `ilas_octet1` • `ilas_octet2` • `ilas_octet3` The content of 14 configuration octets in the second multiframe is stored in these 32-bit registers— `ilas_octet0`, `ilas_octet1`, `ilas_octet2`, and `ilas_octet3`.	• /R/ character is followed by /Q/ character or K28.4 (0x9C) at the beginning of the second multiframe. • The `jesd204_rx_int` signal is deasserted if there is no error. • Octets 0–13 read from these registers match with the JESD204B parameters in each test setup.
ILA.3	Check the lane alignment	The following signals in <*ip_variant_name*>**_inst_phy.v** are tapped: • `jesd204_rx_pcs_data[(L*32)-1:0]` • `jesd204_rx_pcs_data_valid[L-1:0]` (2) The following signals in <*ip_variant_name*>**.v** are tapped: • `rx_somf[3:0]` • `dev_lane_aligned` • `jesd204_rx_int` The `rxlink_clk` signal is used as the SignalTap II sampling clock.	• The `dev_lane_aligned` signal is asserted upon the last /A/ character of the ILAS is received, which is followed by the first data octet. • The `rx_somf` signal marks the start of multiframe in user data phase. • The `jesd204_rx_int` is deasserted if there is no error.

Receiver Transport Layer

To check the data integrity of the payload data stream through the RX JESD204B IP Core and transport layer, the ADC is configured to output PRBS-9 test data pattern. The ADC is also set to operate with the same configuration as set in the JESD204B IP Core. The PRBS checker in the FPGA fabric checks data integrity for one minute.

This figure shows the conceptual test setup for data integrity checking.

Figure 3: Data Integrity Check Using PRBS Checker



The SignalTap II Logic Analyzer tool monitors the operation of the RX transport layer.

Table 3: Transport Layer Test Cases

Test Case	Objective	Description	Passing Criteria
TL.1	Check the transport layer mapping using PRBS-9 test pattern.	The following signal in **altera_jesd204_transport_rx_top.sv** is tapped: • `jesd204_rx_data_valid` The following signals in **jesd204b_ed.sv** are tapped: • `data_error` • `jesd204_rx_int` The `rxframe_clk` signal is used as the SignalTap II sampling clock. The `data_error` signal indicates a pass or fail for the PRBS checker.	• The `jesd204_rx_data_valid` signal is asserted. • The `data_error` and `jesd204_rx_int` signals are deasserted.

Descrambling

The PRBS checker at the RX transport layer checks the data integrity of the descrambler.

The SignalTap II Logic Analyzer tool monitors the operation of the RX transport layer.

Table 4: Descrambler Test Cases

Test Case	Objective	Description	Passing Criteria
SCR.1	Check the functionality of the descrambler using PRBS-9 test pattern.	Enable scrambler at the ADC and descrambler at the RX JESD204B IP Core. The signals that are tapped in this test case are similar to test case TL.1	• The `jesd204_rx_data_valid` signal is asserted. • The `data_error` and `jesd204_rx_int` signals are deasserted.

Deterministic Latency (Subclass 1)

Figure below shows a block diagram of the deterministic latency test setup. A SYSREF generator provides a periodic SYSREF pulse for both the AD6676 and JESD204B IP Core. The SYSREF generator is running in link clock domain and the period of SYSREF pulse is configured to the desired multiframe size. The SYSREF pulse restarts the LMFC counter and realigns it to the LMFC boundary.

Figure 4: Deterministic Latency Test Setup Block Diagram

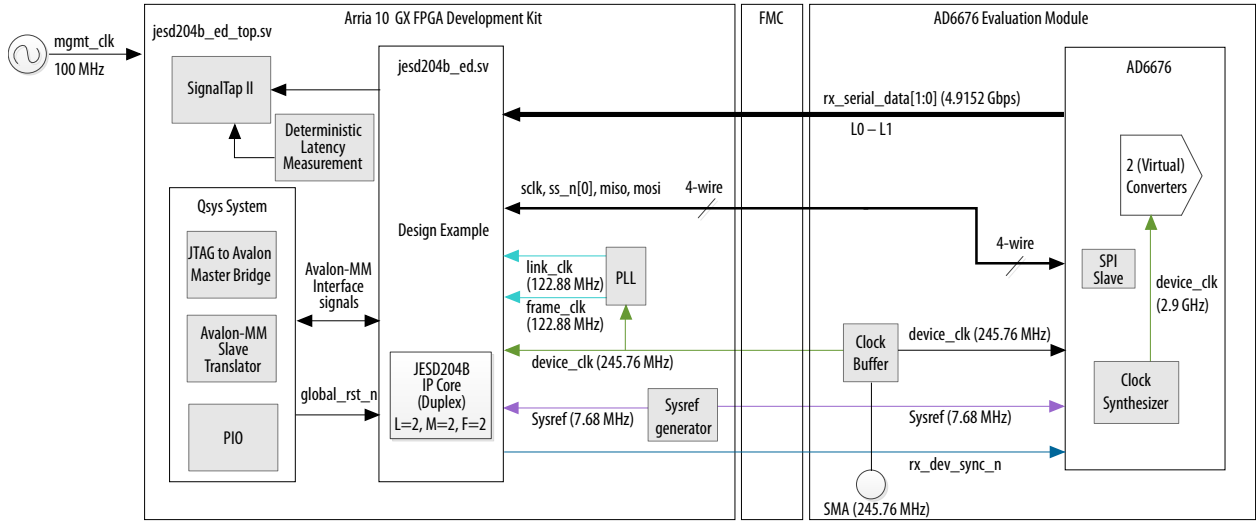
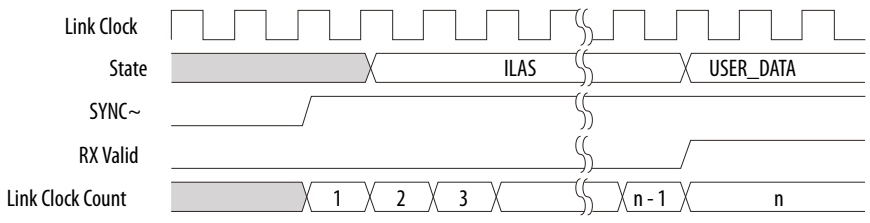


Figure 5: Deterministic Latency Measurement Timing Diagram



With the setup above, three test cases were defined to prove deterministic latency. By default, the JESD204B IP Core detects a single SYSREF pulse. The SYSREF single-shot mode is enabled on the AD6676 for this deterministic measurement.

Table 5: Deterministic Latency Test Cases

Test Case	Objective	Description	Passing Criteria
DL.1	Check the FPGA SYSREF single detection.	Check that the FPGA detects the first rising edge of SYSREF pulse. Read the status of `sysref_singledet (bit[2])` identifier in the `syncn_sysref_ctrl` register at address 0x54.	The value of `sysref_singledet` identifier should be zero.
DL.2	Check the SYSREF capture.	Check that the FPGA and ADC capture SYSREF correctly and restart the LMF counter for every reset and power cycle. Read the value of `rbd_count (bit[10:3])` identifier in `rx_status0` register at address 0x80.	If the SYSREF is captured correctly and the LMF counter restarts, for every reset and power cycle, the `rbd_count` value should only vary by two integers due to word alignment.
DL.3	Check the latency from start of SYNC~ deassertion to the first user data output.	Check that the latency is fixed for every FPGA and ADC reset and power cycle. Record the number of link clocks count from the start of SYNC~ deassertion to the first user data output, which is the assertion of `jesd204_rx_link_valid` signal. The deterministic latency measurement block has a counter to measure the link clock count.	Consistent latency from the start of SYNC~ deassertion to the assertion of `jesd204_rx_link_valid` signal.

JESD204B IP Core and ADC Configurations

The JESD204B IP Core parameters (L, M and F) in this hardware checkout are natively supported by the AD6676. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the AD6676 operating conditions.

The hardware checkout testing implements the JESD204B IP Core with the following parameter configuration.

Table 6: JESD204B IP Core Parameter Configuration

Configuration	Setting	Setting
LMF	222	124
HD	0	0
S	1	1
N	16	16
N'	16	16
CS	0	0
CF	0	0
ADC Sampling Clock (GHz)	2.94912	2.94912
FPGA Device Clock (MHz) (3)	245.76	122.88
FPGA Management Clock (MHz)	100	100
FPGA Frame Clock (MHz)	122.88	122.88
FPGA Link Clock (MHz) (4)	122.88	122.88
Lane Rate (Gbps)	4.9152	4.9152
Character Replacement	Enabled	Enabled
Data Pattern (5)	• PRBS-9 • Ramp	• PRBS-9 • Ramp

(3) The device clock is used to clock the transceiver.
(4) The frame clock and link clock is derived from the device clock using an internal PLL.
(5) The ramp pattern is used in deterministic latency measurement test cases DL.1, DL.2, and DL.3 only.

Test Results

Table 7: Results Definition

This table lists the possible results and their definition.

Result	Definition
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with comments	The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Refer to comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, and SCR.1 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

Table 8: Results

Test	L	M	F	Subclass	SCR	K	Data Rate (Gbps)	Sampling Clock (GHz)	Link Clock (MHz)	Result
1	2	2	2	1	0	16	4.9152	2.94912	122.88	PASS
2	2	2	2	1	1	16	4.9152	2.94912	122.88	PASS
3	2	2	2	1	0	32	4.9152	2.94912	122.88	PASS
4	2	2	2	1	1	32	4.9152	2.94912	122.88	PASS
5	1	2	4	1	0	16	4.9152	2.94912	122.88	PASS
6	1	2	4	1	1	16	4.9152	2.94912	122.88	PASS
7	1	2	4	1	0	32	4.9152	2.94912	122.88	PASS
8	1	2	4	1	1	32	4.9152	2.94912	122.88	PASS

The following table shows the results for test cases DL.1, DL.2, DL.3 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

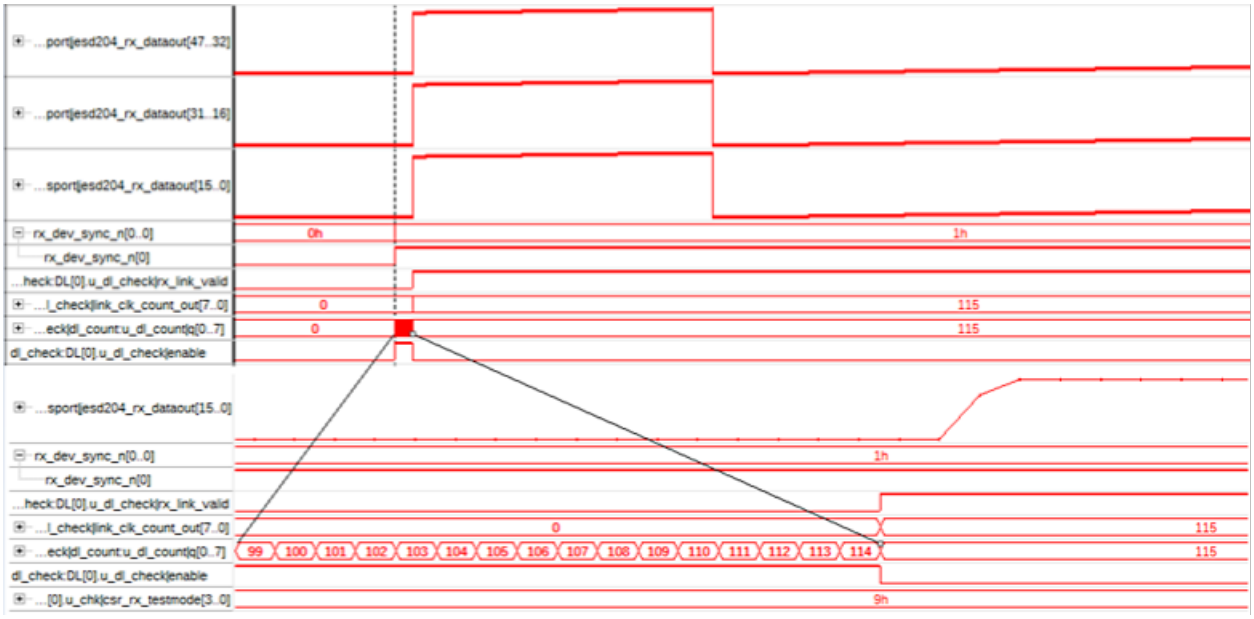
Table 9: Results for Deterministic Latency Test

Test	L	M	F	Subclass	K	Data Rate (Gbps)	Sampling Clock (GHz)	Link Clock (MHz)	Result
DL.1	2	2	2	1	32	4.9152	2.94912	122.88	PASS
DL.2	2	2	2	1	32	4.9152	2.94912	122.88	PASS
DL.3	2	2	2	1	32	4.9152	2.94912	122.88	Pass with comments. Link clock observed = 115 with ADC LMFC offset register set to 0.
DL.1	2	2	2	1	16	4.9152	2.94912	122.88	PASS
DL.2	2	2	2	1	16	4.9152	2.94912	122.88	PASS
DL.3	2	2	2	1	16	4.9152	2.94912	122.88	Pass with comments. Link clock observed = 67 with ADC LMFC offset register set to 0.
DL.1	1	2	4	1	32	4.9152	2.94912	122.88	PASS
DL.2	1	2	4	1	32	4.9152	2.94912	122.88	PASS
DL.3	1	2	4	1	32	4.9152	2.94912	122.88	Pass with comments. Link clock observed = 195 with ADC LMFC offset register set to 0.
DL.1	1	2	4	1	16	4.9152	2.94912	122.88	PASS
DL.2	1	2	4	1	16	4.9152	2.94912	122.88	PASS

Test	L	M	F	Subclass	K	Data Rate (Gbps)	Sampling Clock (GHz)	Link Clock (MHz)	Result
DL.3	1	2	4	1	16	4.9152	2.94912	122.88	Pass with comments. Link clock observed = 99 with ADC LMFC offset register set to 5.

The following figure shows the SignalTap II waveform of the clock count from the deassertion of SYNC~ to the assertion of the `jesd204_rx_link_valid` signal, the first output of the ramp test pattern (DL.3 test case). The clock count measures the first user data output latency.

Figure 6: Deterministic Latency Measurement Ramp Test Pattern Diagram



Test Result Comments

In each test case, the RX JESD204B IP core successfully initialize from CGS phase, ILA phase, and until user data phase. No data integrity issue is observed by the PRBS checker.

In deterministic measurement test case DL.3, the link clock count in the FPGA depends on the board layout and the LMFC offset value set in the ADC register. The link clock count can vary by only one link clock when the FPGA and ADC are reset or power cycled. The link clock variation in the deterministic latency measurement is caused by word alignment, where the control characters fall into the next cycle of data some time after realignment. This makes the duration of ILAS phase longer by one link clock some time after reset or power cycle.

AN 753 Document Revision History

Date	Version	Changes
November 2015	2015.11.02	Initial release.