

AN-731: Simultaneous Switching Noise Guidelines for Intel® Cyclone® 10 LP, Cyclone® IV, and Cyclone® III Devices



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Simultaneous Switching Noise Guidelines for Intel® Cyclone® 10 LP, Cyclone® IV, and Cyclone® III Devices

Intel® Cyclone® 10 LP, Cyclone IV, and Cyclone III devices provide an external clock input option for the global clock network. The input clock can be differential or single-ended.

The advantages of a differential clock over a single-ended clock scheme are:

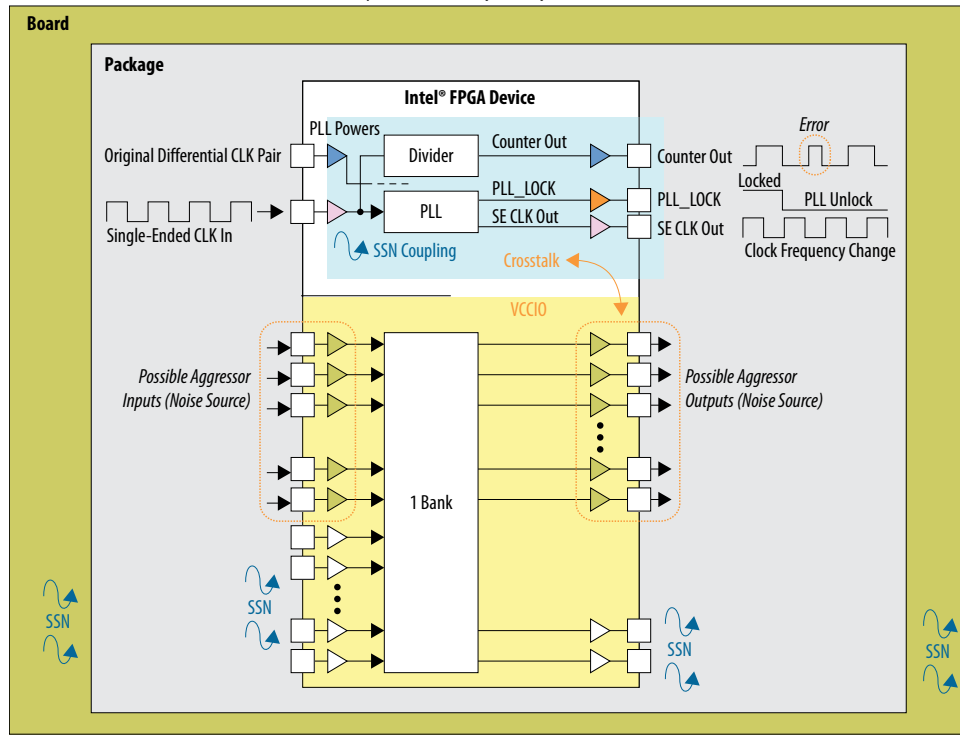
- The differential clock is more immune to the common-mode noise, simultaneous switching noise (SSN) and ground bounce
- The differential clock is more robust for changing reference or discontinuity

For the single-ended clock input option, SSN can impact the clock input, even if the clock frequency is low frequency below 100 MHz. As shown in Figure 1, when the multi-aggressor input or output signals toggle simultaneously in one bank, large SSN is induced, that degrades power and ground integrity. When the input clock is degraded by SSN, it can cause the PLL to lose lock, and cause the counter to malfunction. To limit SSN and crosstalk, you must restrict the number of switching outputs in a single bank. If the single-ended clock input is close to the potential crosstalk aggressor signal, it may also result in crosstalk that can cause a glitch in the victim single-ended clock signal.

Intel Cyclone 10 LP, Cyclone IV, and Cyclone III devices are designed with wire-bond packages. The inductive coupling between adjacent pins of a wire-bonded package can result in a higher noise. The package inductance of a two-layer wire-bond package is much higher compared to that of a 4-layer package, because it does not have a good reference plane.

Figure 1. Example of a Single-Ended Clock Input

If possible use differential external clock input scheme (LVDS).



External Clock Inputs Guidelines

Victim Clock Pin Assignments

Assignments for pins adjacent to the clock input pin affect SSN. SSN is directly proportional to the mutual inductance of the ground path.

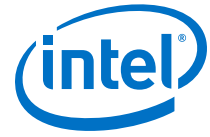
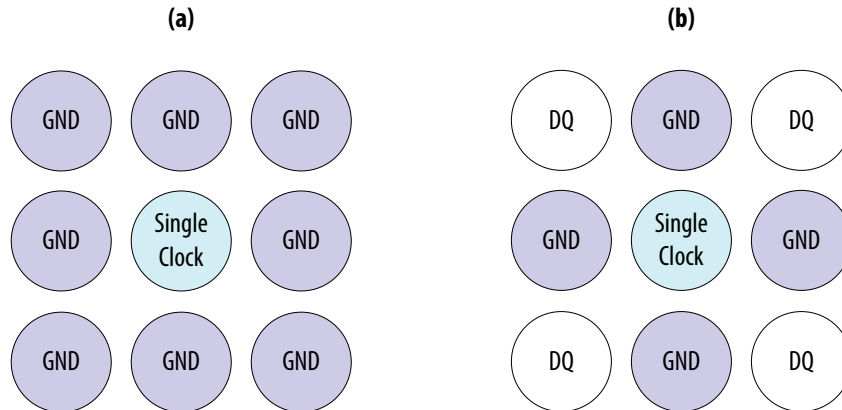


Figure 2. Single-Ended Clock Input Ground Balls Surrounding Victim Clock Input Signals

- As shown in (a), you can reduce the effect of SSN by assigning all of the ground balls surrounding the single-ended clock.
- As shown in (b), if you cannot assign all of the ground balls, then you must try to have a minimum of four ground balls around the single-ended clock path.



The ground balls decrease the mutual inductance of the victim single-ended clock and block crosstalk from adjacent potential aggressor I/O signals.

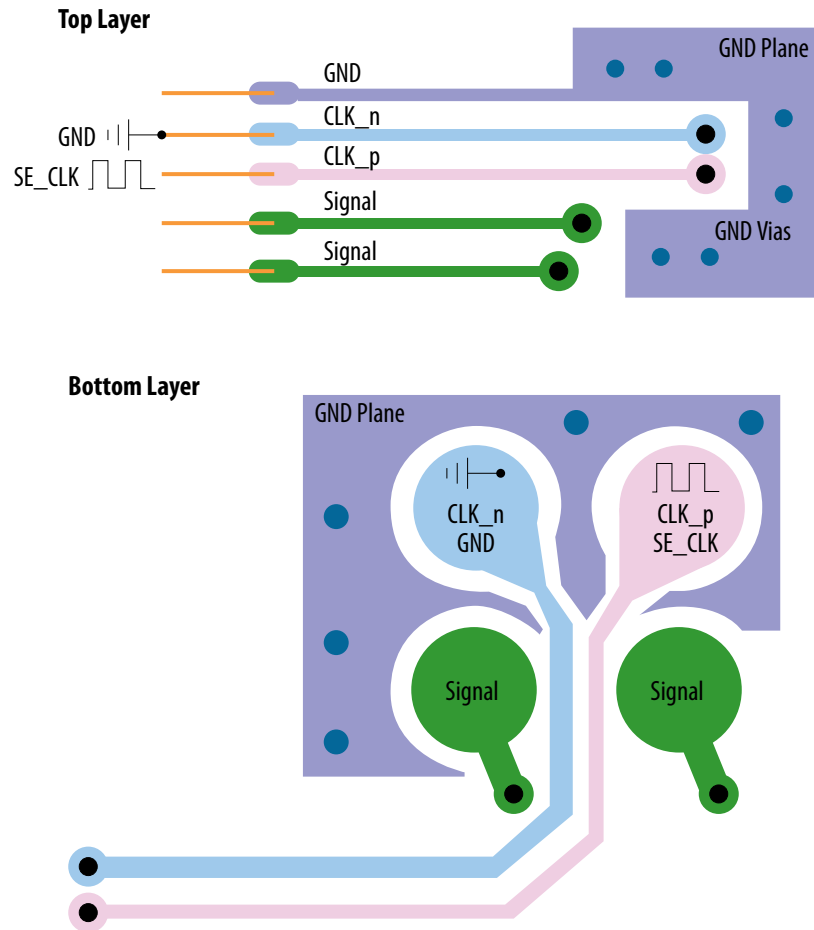
Intel recommends that you do not assign any other clock signal or normal I/O signal on the original differential clock pair. This signal can cause large coupling noise on the single-ended clock input signal.

External Single-Ended Clock Input SSN Requirements

You can assign ground on the original differential clock pair, when you use the external clock input as a single-ended clock. As shown in the following figure, the differential signal pair in the package, is laid out as differential, with a value of 100 Ω . It ensures that the original differential clock pair has a strong coupling structure.

Intel recommends that you do not assign any other clock signal or normal I/O signal on the original differential clock pair, if you assign an external clock input as a single-ended clock. This signal can cause large coupling noise on the single-ended clock input signal.

Figure 3. Package Design Example for a Differential Clock Input Signal Pair



Effects of I/O Termination

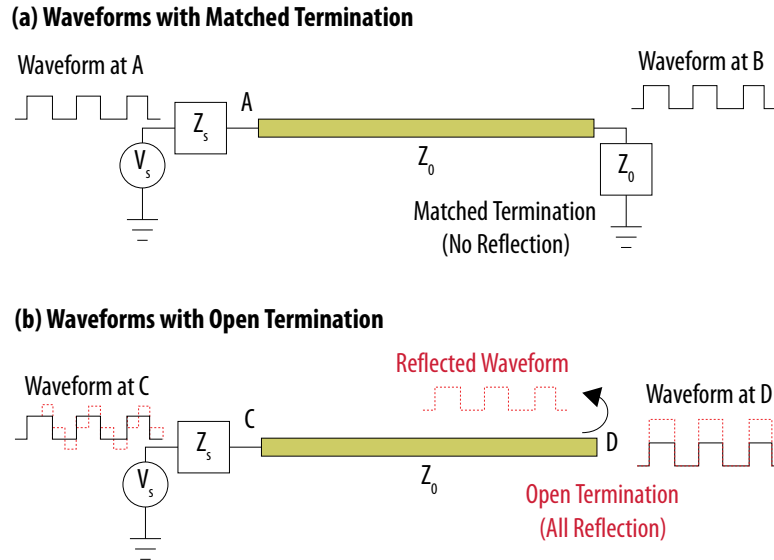
Unterminated signals can cause signal reflection. These reflections can manifest themselves as crosstalk noise on the victim clock signal.

The reflected waveforms in the multi-aggressor signals will transmit back-and-forth and can cause crosstalk noise on the victim clock input signal and can have an effect on power and ground. As shown in Figure 4, terminating potential aggressor signals appropriately will reduce the possibility of degrading the victim clock signal quality and power and ground noise.

In Intel Cyclone 10 LP, Cyclone IV, and Cyclone III devices, signal I/O standard can be selected in terminated or un-terminated mode.



Figure 4. Reflection Due to Matched and Open Termination



Note:

I/O Standards with or without Termination:

- Terminated I/O standards—SSTL, HSTL
- Unterminated I/O standards—LVTTTL, LVCMOS

As per JEDEC, the LVTTTL and LVCMOS, PCI, and PCI-X I/O standards do not specify a recommended termination scheme.

Effect of Slow Aggressor Signal Slew Rate on SSN

Crosstalk is inversely proportional to rise time. There is an increase in crosstalk when the aggressor signal has fast rise and fall time.

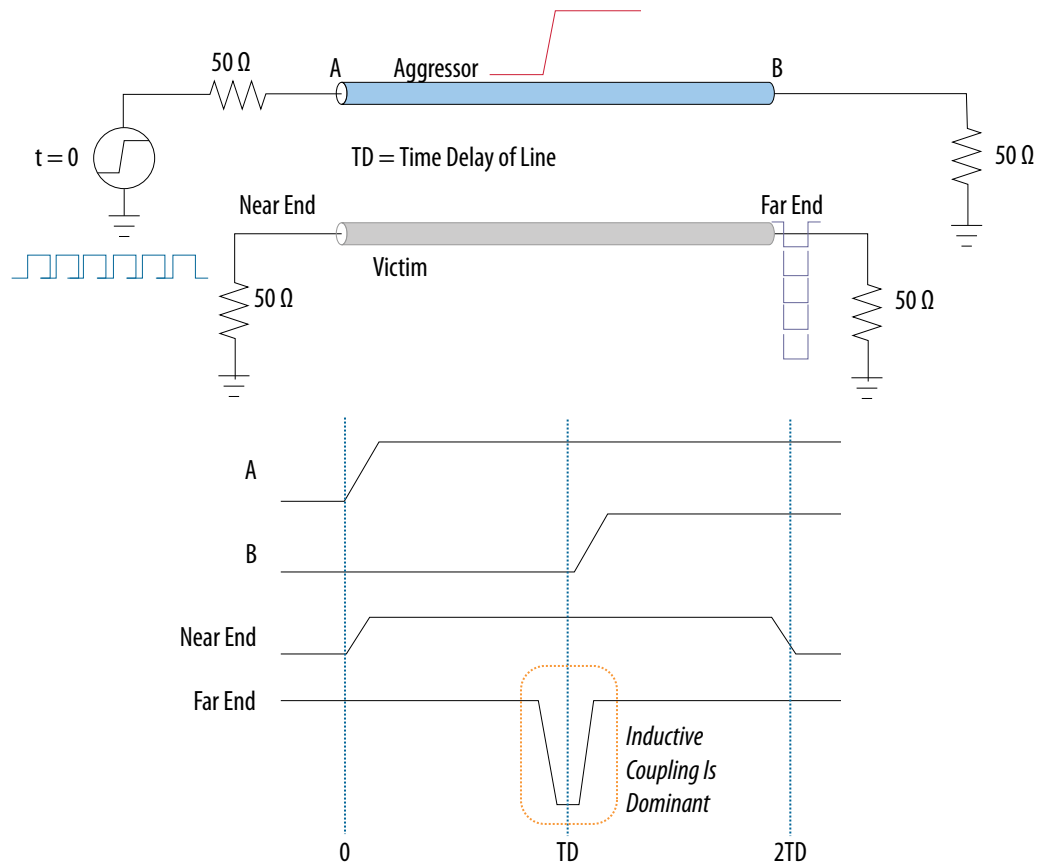
Equation 1. Crosstalk Equation

$$V_{\text{Far-End Crosstalk}} \propto \frac{1}{T_r}$$

To decrease SSN caused by crosstalk, use the slowest slew rate for potential aggressor signals, especially when multiple I/O signals are switching simultaneously.

Figure 5. Crosstalk Mechanism

This figure shows an example of a victim signal that is degraded by crosstalk

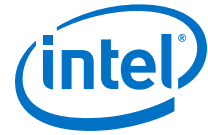


Effect of Fast Slew Rate of Victim Clock on SSN

Crosstalk or SSN on power and ground can induce a glitch or jitter on the victim clock input signal. Increasing the ramp time (V/ns) of the victim clock input signal will mitigate this affect. Fast rise and fall edges reduce the time the clock signal is above V_{IH} and below V_{IL} and can push out the glitch from V_{IH} or V_{IL} zone such that it no longer affects the clock and reset signals.

Figure 6. Benefit of Faster Slew Rate on Victim Clock Input





I/O Restriction Guidelines

To reduce the impact of SSN due to potential aggressor signals, I/O restrictions are essential to control the number of toggling aggressor signals in the same I/O bank.

Table 1. I/O Restriction Guidelines per Bank

This table lists the percentages of the total number of I/O pins that can be toggled without inducing any error on the victim single-ended clock under SSN and/or crosstalk condition. The numbers in the table are based on actual measurements that were done using an Intel characterization system setup. These measurements may vary based on your system design and the board configuration. As shown in the table, crosstalk is the primary cause of attenuation or malfunction of the victim clock input.

Aggressor I/O Standards	Percentage of Simultaneous Switching Pins per Bank			
	4-Layer Wire-bonding Package		2-Layer Wire-bonding Package	
	Forward toggling pattern	Reverse toggling pattern	Forward toggling pattern	Reverse toggling pattern
3.0V LVCMOS 16mA (fast slew rate)	13%	95%	5%	5%
2.5V LVTTTL 16mA (fast slew rate)	55%	95%	27%	84%
2.5V LVTTTL 12mA (fast slew rate)	55%	96%	27%	84%
2.5V LVTTTL 4mA	100%	100%	100%	100%
2.5V SSTL 2.5V Class II 16mA (fast slew rate)	100%	100%	100%	100%

The following tests are performed to better understand crosstalk and the effect of power and/or ground noise on the victim clock inputs:

- Forward toggling pattern test—in this test each aggressor, starting from the closest to the farthest from the victim is switched on one by one, until an error occurs. The main influence of crosstalk on the victim clock input is measured, and the number of switched-on aggressors are noted.
- Reverse toggling pattern test—in this test each aggressor, starting from the farthest to the closest from the victim, is switched on one by one, until an error occurs. The primary influence of power and ground noise on the victim clock input is measured, and the number of switched-on aggressors are noted.

Reverse toggling pattern test confirms that a 2-layer substrate package is more susceptible to SSN than a 4-layer substrate package.

It is difficult to quantify the effect of SSN and crosstalk on the victim clock input separately.

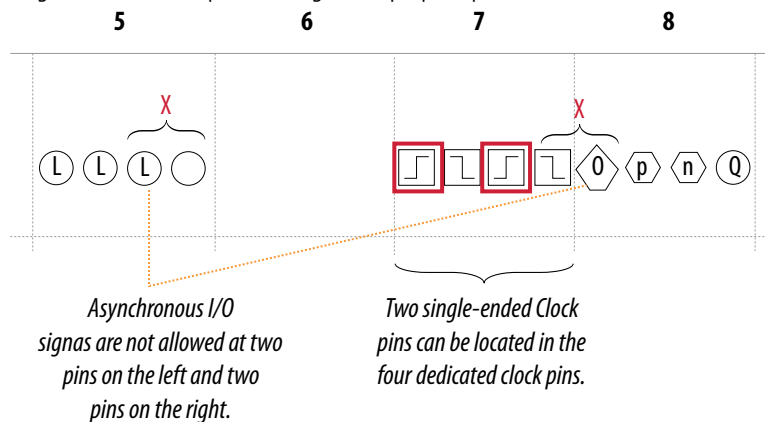
You can prevent the PLL unlock issue or counter malfunction by using the potential aggressor signals with lower current strength and terminated I/O standard.

Single-Ended Clock Input Pad Placement Guideline

- You can put two single-ended clocks on any of the four dedicated pins.
 - Asynchronous input or output signals are not allowed on the two left most and right most pins.
- If you want to put three or four single-ended clocks on the four dedicated pins.
 - Check mutual inductance of these pins
 - Contact Intel FPGA mySupport if you cannot correlate the pad location and mutual inductance
- To avoid crosstalk, do not put the aggressor pin adjacent to the victim clock input pin.
 - Separate the aggressor pin and the victim pin by two or more pins
 - You can check the separation in Intel Quartus® Prime Pad Viewer

Figure 7. Single-Ended Clock Input Pad Placement Guideline

Single-ended input or output signals are not allowed on the two left-most and right-most pins to provide a single-ended clock input on the general-purpose pins.



Related Links

- [Intel Cyclone 10 LP Device Family Pin Connection Guidelines](#)
- [Cyclone IV Device Pin Connection Guideline](#)
- [Cyclone III Device Pin Connection Guideline](#)
- [Cyclone III Simultaneous Switching Noise \(SSN\) Design Guidelines](#)
- [Input Signal Edge Rate Guidance](#)
- [Intel FPGA mySupport](#)



Document Revision History for AN-731: Simultaneous Switching Noise Guidelines for Intel Cyclone 10 LP, Cyclone IV, and Cyclone III Devices

Date	Version	Changes
November 2017	2017.11.06	<ul style="list-style-type: none">• Added Intel Cyclone 10 LP support.• Made editorial text and structure update.• Rebranded as Intel.• Retitle the document.
February 2015	2015.02.04	Initial release.