Serial Digital Interface (SDI) II Implementation in Arria 10 Devices

2014.11.12

AN-723 Subscribe Send Feedback

For Arria 10 devices, the generated Serial Digital Interface (SDI) II IP core does not include the transceiver PHY related blocks. You must instantiate these transceiver components separately and integrate them with the SDI II IP core.

You need to instantiate the following components together with the SDI II IP core.

- Transceiver Native PHY IP core
- Transceiver Phase-Locked Loop (PLL) IP core
- Transceiver PHY Reset Controller IP core
- Transceiver Reconfiguration Controller

You can use the provided SDI II design example files to instantiate, compile, and simulate these IP cores for your design.

Related Information

- **Design Example for AN723**
  Provides the design files for this application note.
- **SDI II IP Core User Guide**
  Provides more information about the SDI II IP core.
- **Arria 10 Transceiver PHY User Guide**
  Provides more information about the Transceiver Native PHY, Transceiver PHY Reset Controller, and Transceiver PLL IP cores.

Instantiate Transceiver Native PHY IP Core

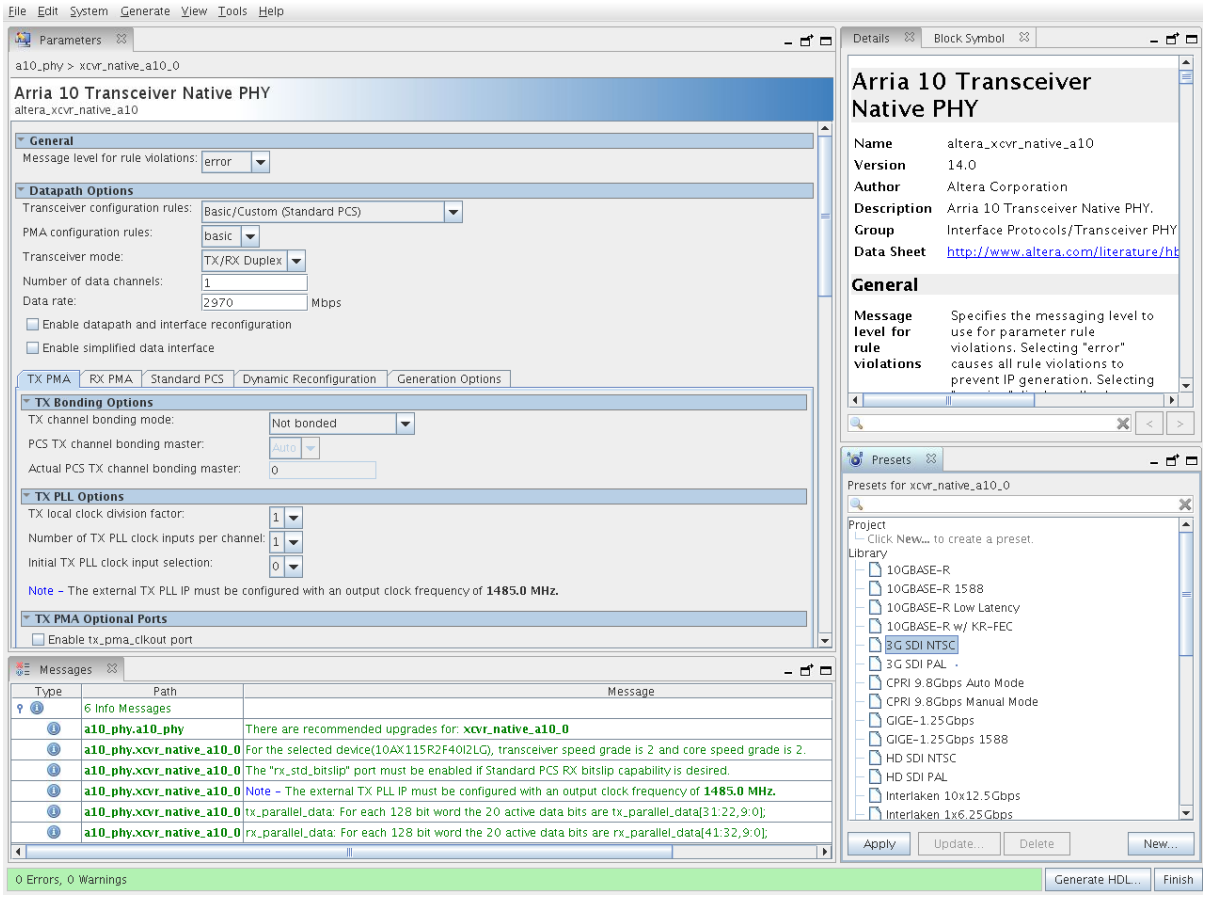
To instantiate the Native PHY IP core, follow these steps:

1. In the **IP Catalog**, click **Interface Protocols** > **Transceiver PHY** > **Arria 10 Transceiver Native PHY IP** .
2. Click **Add**.
3. On the Arria 10 Transceiver Native PHY IP parameter editor, enter the desired name for the Native PHY IP core instance.
4. On the **Presets** search panel, type `SDI` to search for all SDI presets.
   You will see the following presets:

- 3G SDI NTSC: used for multi rates, 3G-SDI single rate and SD-SDI single rate, (2.97 Gbit/s)
- 3G SDI PAL: used for multi rates, 3G-SDI single rate and SD-SDI single rate, (2.97/1.001 Gbit/s)
- HD SDI NTSC: used for HD-SDI single rate and HD-SDI Dual-link, (1.485 Gbit/s)
- HD SDI PAL: used for HD-SDI single rate and HD-SDI Dual-link, (1.485/1.001 Gbit/s)

5. Select the desired SDI preset and click **Apply.**
6. The parameter values in the parameter editor will now be specified to the SDI preset you selected.

Note: The value of the output clock frequency is required for the Tx PLL. You must configure the external Tx PLL IP core to produce the identical clock frequency as specified here.



7. For dual-rate or triple-rate SDI II instances, you must turn on **Enable dynamic configuration** and **Generate System/Verilog package file**. Make sure to match the configuration file prefix to the one in the **rcfg_sdi_cdr.sv** file generated in the design example.

```
//////////////////////////////////////////////////////////////////////////////
// CDR Reconfig Block
// Generates DPRIO address and control signals for a single xcvr interface
//   - Performs RMW for handling logical CDR Reconfiguration
//////////////////////////////////////////////////////////////////////////////
`timescale 1 ns / 1 ps

module rcfg_sdi_cdr #(
    parameter xcvr_rcfg_if_type     = "channel",
    parameter xcvr_rcfg_addr_width  = 10,
    parameter xcvr_rcfg_data_width  = 32,
    parameter xcvr_dprio_addr_width = 9,
    parameter xcvr_dprio_data_width = 8
) (
    input  wire        clk,
    input  wire        reset,

    input  wire        cdr_reconfig_req,
    input  wire [1:0]  cdr_reconfig_sel,
    output reg         cdr_reconfig_busy,

    output reg                                reconfig_write,
    output reg                                reconfig_read,
    output reg  [xcvr_rcfg_addr_width-1:0]    reconfig_address,
    output reg  [xcvr_rcfg_data_width-1:0]    reconfig_writedata,
    input  wire [xcvr_rcfg_data_width-1:0]    reconfig_readdata,
    input  wire                               reconfig_waitrequest
);
  import altera_xcvr_functions::*;
  import altera_xcvr_native_a10_reconfig_parameters::*;
```

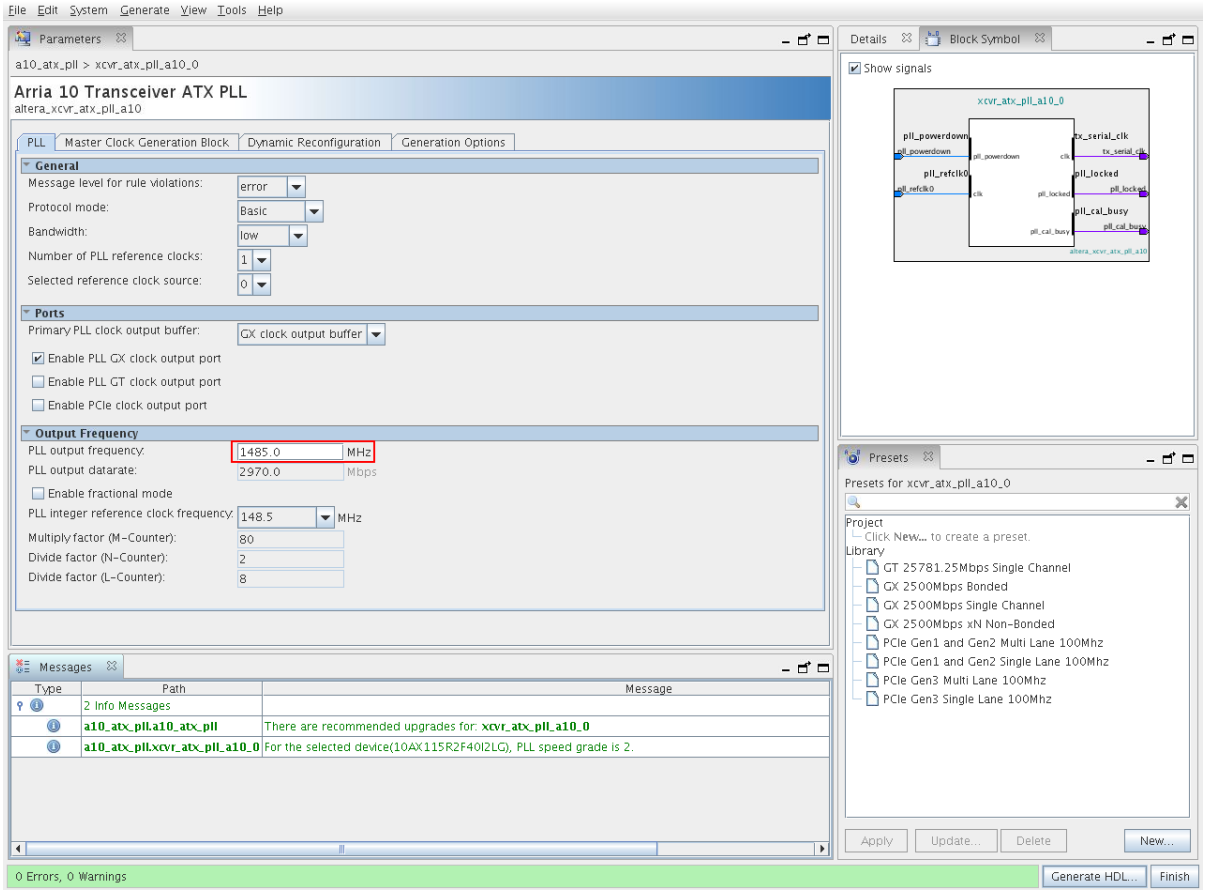
Note: If you want to change the name of the configuration file here, ensure that you use the same name in the **rcfg_sdi_cdr.sv** file located in the **sdi_ii_0_example_design/example_design/sdi_ii_0_example_design_ed/sdi_ii_ed_reconfig_a10_140** folder.

8. After you have specified the desired settings, click **Generate HDL** to generate the corresponding synthesis files and simulation models for the transceiver.
9. You need to manually add the reconfiguration parameter library file, **altera_xcvr_native_a10_reconfig_parameters.sv**, into your project settings. On Project menu, select **Add/Remove Files**. Under **Files Category**, navigate to **<Native PHY IP_instance_name>\altera_xcvr_native_a10_140\synth** directory to locate and add the library file.

Instantiate Transceiver Phase-Locked Loop IP Core

To instantiate the Phase-Locked Loop (PLL) IP core, follow these steps:

1. In the **IP Catalog**, click **Basic Functions** > **Clocks, PLLs, and Resets** > **PLL**, and select the desired PLL IP core: **Arria 10 Transceiver ATX PLL** or **Arria 10 Transceiver CMU PLL**.
2. In the PLL parameter editor, for the PLL output frequency, enter the same output clock frequency value used in the Native PHY IP core, 1485.0 MHz.

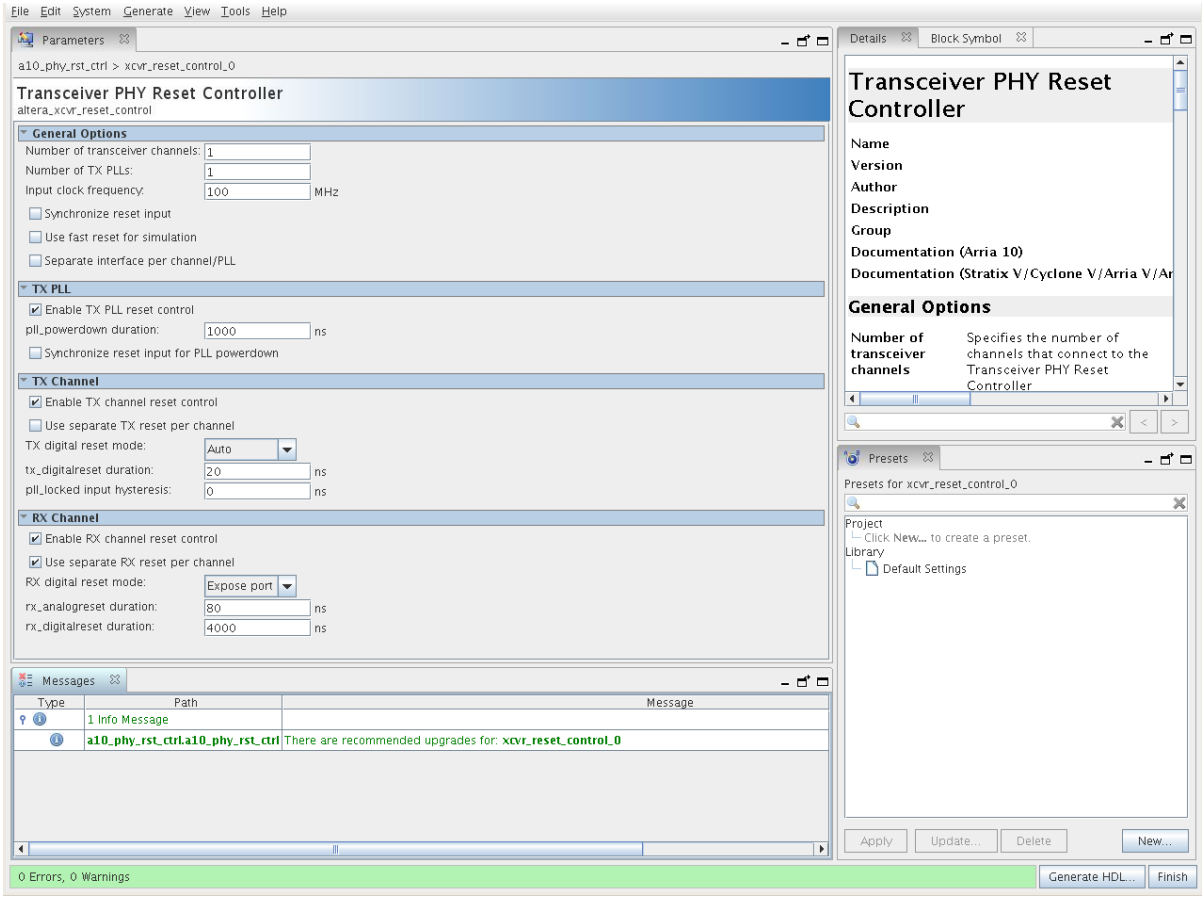


3. After you have specified the desired settings, click **Generate HDL** to generate the corresponding synthesis files and simulation models for the PLL.

Instantiate Transceiver PHY Reset Controller IP Core

To instantiate the Transceiver PHY Reset Controller IP core, follow these steps:

1. In the **IP Catalog**, click **Interface Protocols** > **Transceiver PHY** > **Transceiver PHY Reset Controller**.



2. In the Transceiver PHY Reset Controller parameter editor, specify the following settings.

Number of transceiver channels	For HD-SDI dual link variants, set to **2**, for other SDI variants, set to **1**.
Number of TX PLLs	If TX PLL switching enabled, set to **2**, otherwise set to **1**.
Synchronize reset input	Turn off.
Use fast reset for simulation	Turn off.
Enable TX PLL reset control	Turn on.
Enable TX channel reset control	Turn on.
TX digital reset mode	Set to **Auto**.
Enable RX channel reset control	Turn on.
Use separate RX reset per channel	Turn on.
RX digital reset mode	Set to **Expose port**.
rx_analogreset duration	Set to **80 ns**.

Instantiate Transceiver Reconfiguration Controller

To instantiate the Transceiver Reconfiguration Controller user logic, follow these steps:

1. Generate the design example from the SDI II parameter editor.
2. Copy the **/sdi_ii_0_example_design/example_design/sdi_ii_0_example_design_ed/sdi_ii_ed_reconfig_a10_140** directory to your design project.
3. Locate and instantiate **sdi_ii_ed_reconfig_a10.sv** on your design top level.

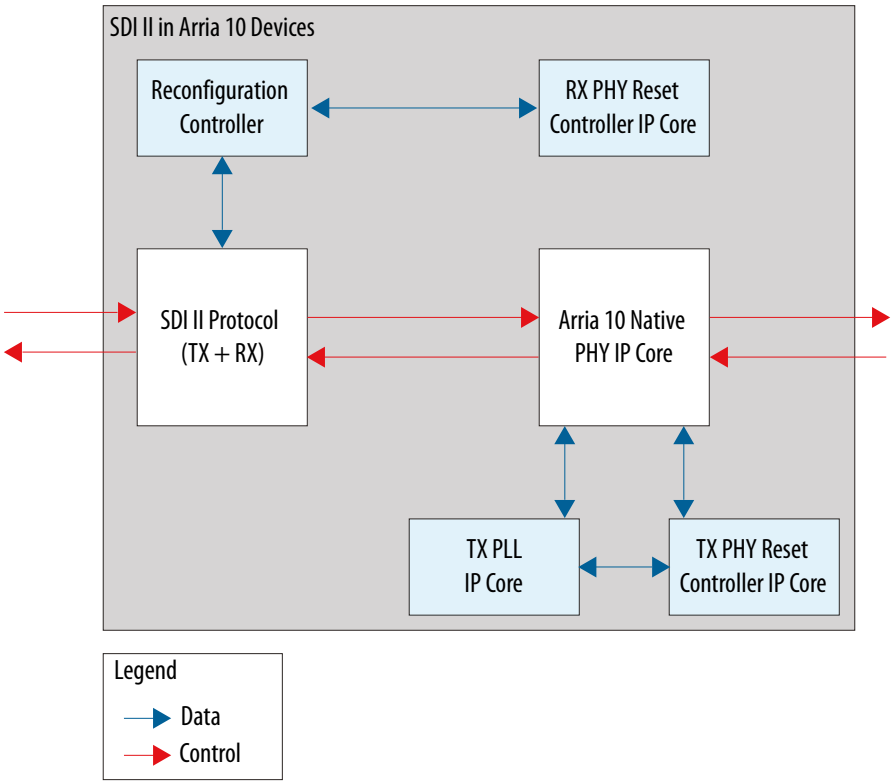
Related Information

SDI II IP Core User Guide
Provides more information about the Transceiver Reconfiguration Controller for Arria 10 devices.

Compile the Design

Figure 1: SDI II IP Core Implementation in Arria 10 Devices

The figure below shows the high-level block diagram of the design implementation.



To compile your design, follow these steps:

1. Select your target Arria 10 device.
2. Instantiate the SDI II IP core.
3. Instantiate the following transceiver IP cores:

- Transceiver Native PHY IP core
- Transceiver ATX PLL IP core
- Transceiver PHY Reset Controller IP core

4. Integrate the tranceiver IP cores with the SDI II IP core. For reference, download the SDI II design files for Arria 10. Compile the design example using version 14.0 Arria 10 of the Quartus II software.
5. Click **Run** to compile the design.

Document Revision History

Date	Version	Changes
November 2014	2014.11.12	Initial release.