Using the Altera Ethernet Design Toolkit

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The Altera Ethernet Design Toolkit is a graphical user interface (GUI) that is built on the system console API. This toolkit helps you to configure and run Ethernet reference designs as well as debug any Ethernet related issues.

The toolkit is verified with the Arria 10 Multi-speed 10M – 10G Ethernet design example using the Quartus® Prime software version 16.0. This document describes the features of the toolkit and how to use the toolkit with the Arria 10 design example.

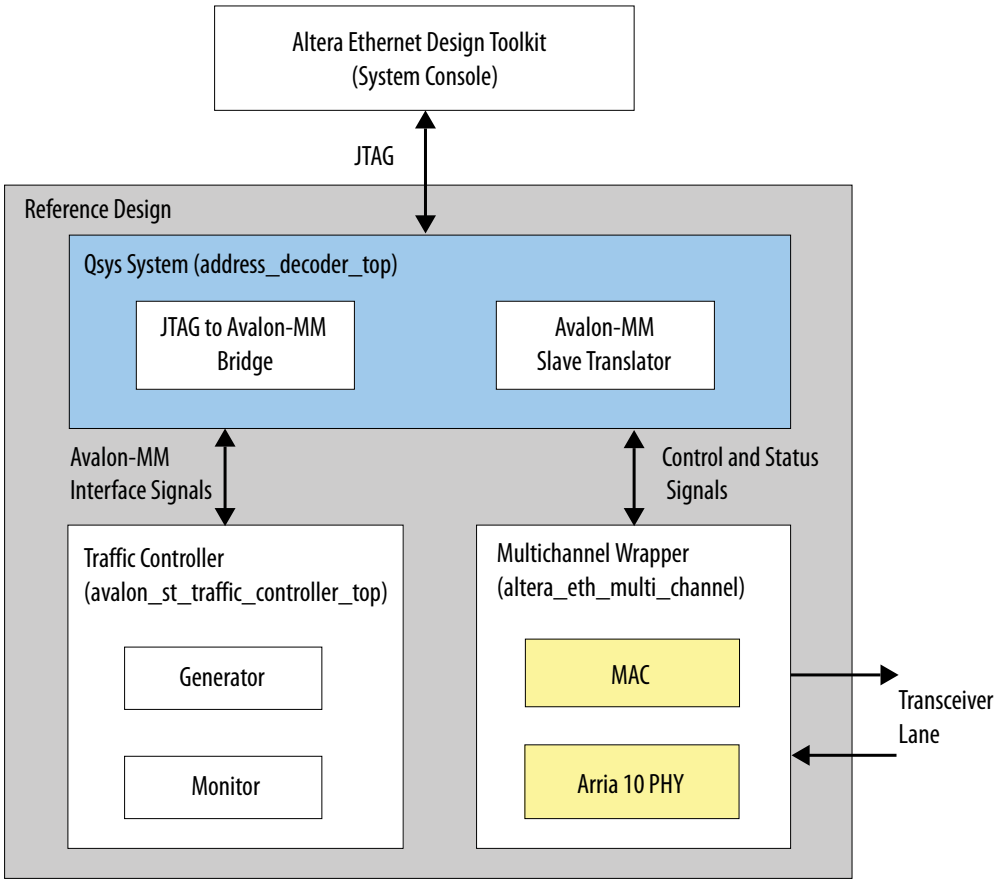
Features

The Ethernet Design toolkit offers the following functions:

- Configure the Altera MAC and PHY IP as well as user logic via JTAG connection.
- Monitor the MAC and PHY IP core status via the GUI LED indicators and statistics counters report.
- Configure the traffic generator to start traffic and also to view the test result from the traffic monitor module.

Figure 1: Arria 10 System Level Design Block Diagram

This diagram shows the connection between the reference design and the design toolkit.



Related Information

- **AN 701: Scalable Low Latency Ethernet 10G MAC using Arria 10 1G/10G PHY**
  For detailed information about the design example.
- **Low Latency Ethernet 10G MAC User Guide**
- **link/nik1398707230472/nik1398706842774**
  For more information about the Arria 10 Transceiver PHY IPs.

Hardware and Software Requirements

To use the Ethernet Design toolkit, the following hardware and software tools are required:

- Arria 10 Signal Intergrity Development Kit
- V13.1 Arria 10 Clock Control software
- Quartus II Altera Complete Design Suite (ACDS) version 16.0 software
- Windows- or Linux-based system console

Getting Started

Before you start using the design toolkit, download the reference design attached with this document.

Related Information

Ethernet Design Example with the Toolkit

Configuring the FPGA and Clock

1. Launch the Quartus II software.
2. Select **Tools** > **Programmer** to configure the FPGA with the generated SOF (**.sof**) file.

   The zip file includes a **.sof** file with a two-channel design:

   - Channel 0 : TX/RX serial signal assigned for board trace serial loopback.
   - Channel 1 : TX/RX serial signal assigned to SFP port.
3. Open the Clock Control tool (**ClockControl.exe**) from development kit's board test system folder . The Clock Control tool is shipped with the "Installation Kit" of the development board.
4. Set the target frequency for Y5 to 644.53125 MHz for 10G reference clock source and Y6 to 125 MHz for 1G reference clock source.

Launching the Ethernet Design Toolkit

Use the system console to launch the design toolkit.

1. Launch the system console from **Tools** > **System Debugging Tools** > **System Console**.
2. In the Tcl Console panel, type the following command to browse to the *SystemConsole_Gui* directory:

   ```
   cd <project directory/systemconsole_gui>
   ```
3. Type the following command to launch the Ethernet Design Toolkit GUI:

   ```
   source main_gui.tcl
   ```

It may take up to a minute to fully load the toolkit in the system console. The toolkit is fully loaded when the % prompt appears after the `% source main_gui.tcl` line.

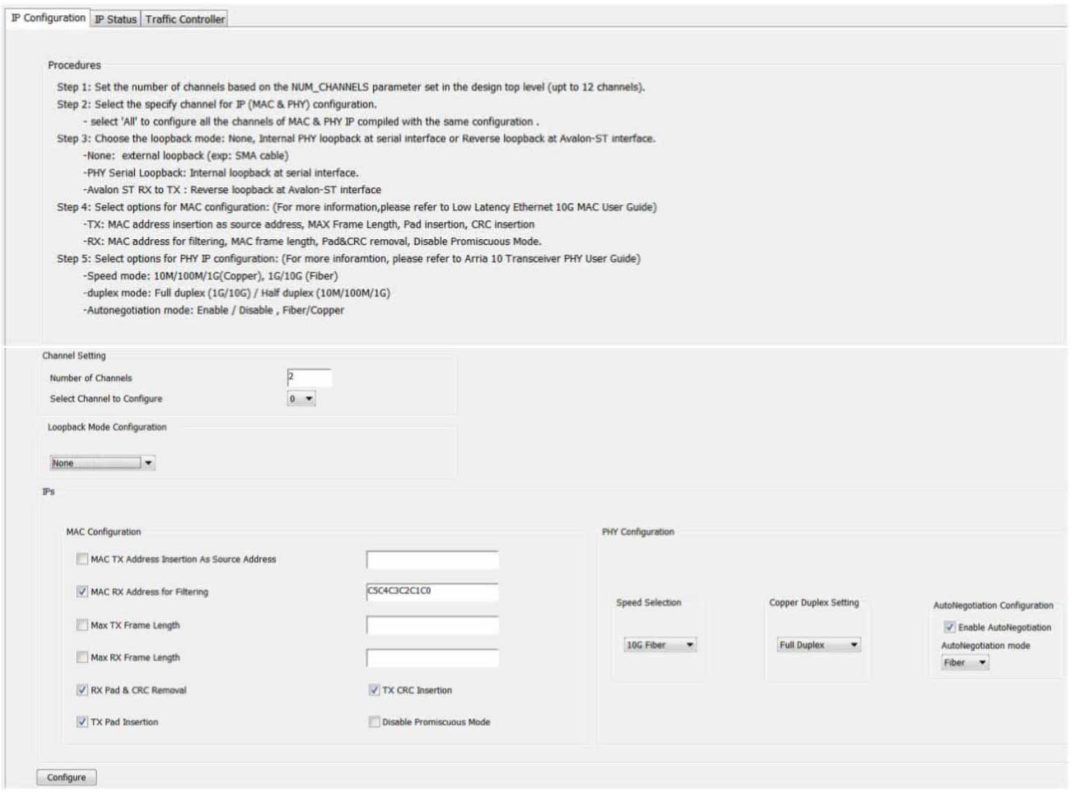
Recommended Flow for Using the Ethernet Design Toolkit

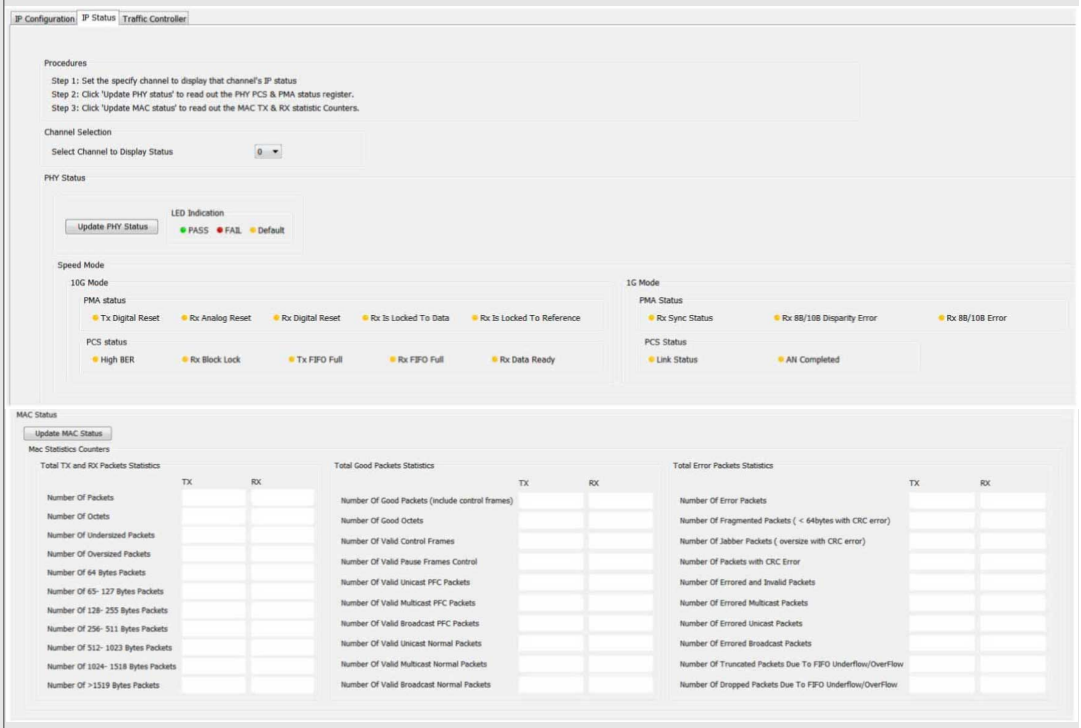
1. Configure the MAC and PHY IP core.
2. Check the MAC and PHY status to verify that the system is ready for traffic.
3. Configure the Traffic Controller Generator Module and start traffic transmission.
4. Check the Traffic Monitor module for information on the received data.
5. For debugging purposes, check the MAC statistics counter for the transmitted and received packets condition after traffic stops.

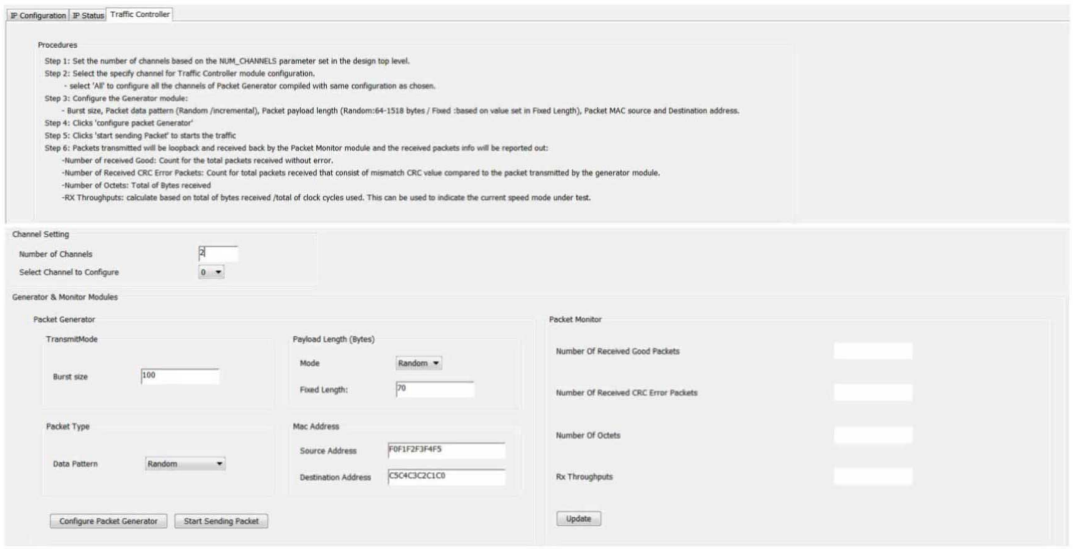
Ethernet Design Toolkit Tabs and Settings

The Ethernet Design toolkit GUI has three tabs. Each tab has a procedure description to help you utilize the tab functions for hardware validation.

Table 1: Ethernet Design Toolkit GUI Tabs

Tab	Function
IP Configurations	 Configures the Altera MAC and PHY IP cores. • MAC configuration: TX pad and CRC insertion, RX pad and CRC removal, and the maximum frame length. • PHY configuration: Speed setting, duplex setting, and auto negotiation.

Tab	Function
IP Status	 Checks the Altera MAC and PHY IP core status. • MAC statistics counters and PHY status register report. • Verify the readiness of the IP cores for traffic.

Tab	Function
Traffic Controller	 Configures the traffic generator to start the traffic and monitor test results. • Packet Generator: Select the burst size, data pattern, payload length, and MAC address. • Packet Monitor: View the results of the RX data and throughput.

IP Configuration Tab

The IP Configuration tab allows you to configure:

- MAC and PHY IP cores
- Number of channels
- Loopback mode

Channel Setting

In this section, the value for `Number of Channels` option must be the same as the `NUM_CHANNELS` parameter you set in the top level design file. The default value is "2" because the design has been pre-compiled with two channels.

When specifying the number of channels, select *All* if you want all the multi-channel IPs to have the same configuration setting.

Loopback Mode Configuration

In this section, you can select *None* for no loopback in external loopback test, *Avalon-ST RX to TX* for reverse loopback at the Avalon-ST interface, or *PHY Serial Loopback* for internal loopback at the serial interface.

IPs

In the *MAC Configuration* section, you can configure the MAC settings:

- MAC TX Address Insertion as Source Address
- MAC RX Address for filtering
- MAC TX/RX Frame Length
- TX CRC insertion
- TX Pad insertion
- RX pad & CRC removal
- Disable promiscuous mode

In the *PHY Configuration* section, you can configure the PHY settings:

- Speed mode (10M/100M/1G/10G)
- Copper duplex setting (Full duplex/Half duplex)
- Autonegotiation (Enable/Disable)
- Autonegotiation mode (Fiber/Copper)

When you are done with the settings, click **Configure** to start the configuration process.

IP Status Tab

After configuring the Altera IP cores, switch to the this tab to check for the MAC and PHY status.

Channel Selection

Because the tested design is a multi-channel design, you need to specify the channel to display the MAC and PHY IP status. The available channel numbers are 0 to 11 based on the *NUM_CHANNELS* parameter set in the top level design file.

PHY Status

This section shows the PHY PCS and PMA status of a particular channel by reading the related channel's PHY status registers. By default, all the status LED are in yellow color. When you click **Update PHY Status**, the status LED changes to red or green to indicate the PHY condition.

For example, during the IP configuration stage, if you configure the PHY IP to 10G speed mode, only the 10G mode PHY status register LED changes color while 1G mode status register LED stay in its default yellow color. A text description for each status LED appears when you set the mouse pointer on the status register name.

MAC Status

When you click **Update MAC Status**, the Ethernet Design toolkit displays the values of the MAC TX and RX statistic counters. The statistic counters are categorized into three sub sections: Total TX & RX Packets Statistics, Total Good Packets Statistics, and Total Error Packets Statistics. From this report, you can check the packets condition on both the TX and RX channels. This information is important during the debugging stage.

Traffic Controller Tab

After checking the IP status and verifying that the system is ready for traffic, use this tab to configure the traffic generator to start the traffic and view the test result.

Channel Setting

Because the tested design is a multi-channel design, you need to specify the channel to configure the traffic generator and monitor modules. The value for `Number of Channels` option must be the same

as the NUM_CHANNELS parameter you set in the top level design file. The default value is "2" because the design has been pre-compiled with two channels.

When specifying the number of channels, select *All* if you want all the packet generator in the channel to have the same configuration setting.

Packet Generator

The available settings include burst size, packet data pattern (Random/Sequential), payload length (Random: 64-1518 bytes /Fixed : based on the value set in fixed length) and also the MAC source and destination address (HEX). Click **Configure Packet Generator** to start the configuration process for the generator. Next, click **Start Sending Packet** to start the packet traffic for a particular channel, which is based on the channel value you set earlier.

Packet Monitor

For design verification, the TX packets in the packet generator goes through a loopback and is received by the packet monitor. When the traffic ends, the packet monitor automatically reports the total good packets received, total CRC error packets received, number of octets received, and also the calculated throughput value.

AN 699 Document Revision History

Date	Version	Changes
May 2016	2016.05.13	• Updated the design example used with the toolkit. • Updated the supported software version. • Added a link to the Arria 10 Transceiver PHY User Guide.
June 2015	2015.06.15	Initial release.