Design Guidelines for HardCopy IV GX Devices

This application note describes the Altera® recommended basic design flow that simplifies HardCopy® IV GX transceiver-based designs.

The design guidelines in this application note provide important factors to consider in high-density, high-performance HardCopy IV GX designs. It is important to follow Altera's recommendations throughout the design process to achieve good results, avoid common issues, and improve your design productivity. The "Design Checklist" on page 30 summarizes the checklist items presented in this document. You can use this checklist to ensure that you have reviewed all the guidelines before completing your HardCopy IV GX design.

The transceiver-based design is divided into phases and is detailed in the following sections:

- "System Specification"

- "Transceiver Configuration" on page 2

- "Dynamic Reconfiguration" on page 3

- "Clocking" on page 3

- "Early System and Board Planning" on page 5

- "Pin Connection Considerations for Board Design" on page 7

- "Implementation and Integration" on page 19

- "Timing Constraints and Analysis" on page 25

For complete details about the HardCopy IV device architecture, refer to the *HardCopy IV Literature* page. For device errata related to HardCopy IV devices, refer to the *Errata Sheet for HardCopy IV E Devices* and the *Errata Sheet for HardCopy IV GX Devices*. For the latest known issues related to HardCopy IV devices, refer to the *Knowledge Database*.

System Specification

The first step in creating a transceiver-based design is to map your system requirements with the HardCopy IV GX device supported features. The HardCopy IV GX device contains multiple transceiver channels that you can configure in multiple data rates and protocols. It also provides multiple transceiver clocking options. For your design, identify the transceiver capabilities and clocking options to ensure that the transceiver meets your system requirements.

This section describes the critical parameters that you must identify as part of this architecture phase.

ISO
9001:2008
Registered

Subscribe

Creating Design Specifications

Use the following steps to ensure that your design specifications are met:

☐ 1. Refer to the device data sheet to ensure that the transceivers meet the data rate and electrical requirements for your target high-speed interface application; for example, the jitter specification and voltage output differential (V_{OD}) range.

☐ 2. Check that the device family you select supports your design requirements; for example, the number of transceiver channels, HCell logic density, memory elements, and DSP blocks.

For information about device characteristics, refer to the "Transceiver Performance Specifications" section in the *DC and Switching Characteristics of HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.
For information about transceiver resources, refer to the *HardCopy IV Device Family Overview* chapter of the *HardCopy IV Device Handbook*.

Device Family Variant and High-Speed Transceivers

HardCopy IV GX devices provide up to 24 full-duplex CDR-based transceivers with physical coding sublayer (PCS) and physical medium attachment (PMA), at serial data rates between 600 Mbps and 6.5 Gbps. Up to 12 additional full duplex CDR-based transceivers with PMA, supporting serial data rates between 600 Mbps and 6.5 Gbps, are also provided.

For more information about HardCopy IV devices, refer to the *HardCopy IV Device Family Overview* chapter of the *HardCopy IV Device Handbook*.

Transceiver Configuration

In a Stratix® device setting, you must select a HardCopy companion device to show the available options for the HardCopy device.

Altera recommends enabling the HardCopy Advisor for successful migration to a HardCopy device. The HardCopy Advisor guides you through the FPGA prototype phase by providing a series of recommendations. The HardCopy Advisor includes major checkpoints in the design process. You can run the HardCopy Advisor anytime during the HardCopy design flow.

To configure the Hardcopy IV transceiver channel's features and options, use the ALTGX MegaWizard™ Plug-In Manager interface.

When selecting a transceiver configuration, use for the following parameters:

☐ 3. Select a HardCopy IV companion device for your HardCopy IV design project in the Quartus® II software.

☐ 4. Check that the transceiver PCS and PMA functional blocks comply with your system requirements.

For more information about transceiver specifications, refer to the "Transceiver Performance Specifications" section in the *DC and Switching Characteristics of HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

For more information about the ALTGX MegaWizard Plug-in Manager, refer to the *ALTGX Transceiver Setup Guide for Stratix IV Devices* chapter of the *Stratix IV Device Handbook*.

☐ 5. Check whether the Quartus II software might impose any restrictions on combining different transceiver configurations within the same transceiver block.

For more information about transceiver configuration restrictions, refer to the *Configuring Multiple Protocols and Data Rates in Stratix IV Devices* chapter of the *Stratix IV Device Handbook*.

Dynamic Reconfiguration

Use the HardCopy IV transceivers in multiple interconnect environments by dynamically reconfiguring the PMA controls (for example, V_{OD}, Pre-emphasis, Equalization, DC gain, and the transceiver channel configuration).

Use the transceiver channel reconfiguration to dynamically switch a transceiver channel to multiple protocols and data rates. The Quartus II software allows you to generate a memory initialization file (**.mif**) that stores unique transceiver settings and provides a dynamic reconfiguration controller, which is soft logic that controls the transceiver reconfiguration with minimal user interface logic. You can generate this soft logic using the ALTGX_RECONFIG MegaWizard interface.

For more information about the ALTGX_RECONFIG interface, refer to the *HardCopy IV GX ALTGX_RECONFIG Megafunction User Guide* chapter of the *HardCopy IV Device Handbook*.

All receiver channels in the HardCopy IV GX device require offset cancellation to counter offset variations in process, voltage, and temperature (PVT) in the receiver. The dynamic reconfiguration controller initiates the sequence to perform offset cancellation on the receiver channels. Therefore, if you configure the HardCopy IV GX transceiver channel in **Receiver only** or the **Transmitter and Receiver** configuration, you must instantiate a dynamic reconfiguration controller.

For more information about offset cancellation or dynamic reconfiguration of the PMA controls or channel configuration, refer to the "Offset Cancellation Feature" section in the *HardCopy IV GX Dynamic Reconfiguration* chapter of the *HardCopy IV Device Handbook*.

Clocking

The HardCopy IV GX transceiver can be clocked by various input reference clocks.

Consider refclk pins for the input reference clock source to provide the best jitter performance.

For more information about the input reference clock source, refer to the *Input Reference Clock Source* section in the *Transceiver Clocking in Stratix IV Devices* chapter of the *Stratix IV Device Handbook*.

Identify the transceiver channel's input reference clock sources:

☐ 6. Ensure that your selected device has the required number of input reference clock resources to implement your design.

☐ 7. Ensure that the transceiver clock input supports the required I/O standards.

☐ 8. Ensure that the clocking restrictions work with your selected device.

☐ 9. Check whether the allowed frequencies for the transceiver input reference clocks meet your system requirements.

☐ 10. Understand the restrictions for the PLL cascade clock.

☐ 11. If you are using the auxiliary transmit (ATX) PLL, understand the recommendations for the input reference clock sources and the restrictions on data rate ranges supported by the ATX PLL.

For transceiver-HCell logic interface clocking:

☐ 12. Ensure that the transceiver-HCell logic interface clock frequency limits meet your system requirements.

For information about transceiver specifications, refer to the *DC and Switching Characteristics of HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

☐ 13. Identify the clocking scheme to clock the transceiver data to the logic in the HCell fabric. If your design has multiple transceiver channels that run at the same data rate and are connected to the one upstream link, you might be able to use a single transceiver-HCell interface clock to provide clocks to the transceiver datapath, which can conserve clock routing resources.

☐ 14. If you are using Basic (PMA direct) mode, determine whether you require a core PLL to provide phase-shifted clocks to the HCell fabric. The core PLL clocks the data received and transmitted between the transceiver and the HCell fabric interface, and may be required to meet the timing requirements of the data transfer.

After you identify the required transceiver parameters, start the implementation and integration phase.

I/O Pin Count, LVDS Channels, and Package Offering

HardCopy IV devices are available in FineLine BGA packages with various I/O pin counts between 368 and 1,104 user I/O pins. Determine the required number of I/O pins for your application, considering the design's interface requirements with other system blocks.

Larger densities and package pin counts offer more full-duplex LVDS channels for different signaling, so ensure that your device density-package combination includes enough LVDS channels. Other factors can also affect the number of I/O pins required for a design, including simultaneous switching noise (SSN) concerns, pin placement guidelines, pins used as dedicated inputs, I/O standard availability for each I/O bank, differences between I/O standards and speed for row and column I/O banks, and package migration options.

For more details about choosing pin locations, refer to the *High-Speed Differential I/O Interfaces and DPA in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook.*

You can compile any existing designs in the Quartus II software with the **Auto device**, selected by the **Fitter** option in the **Settings** dialog box, to determine how many input and output pins are used.

HardCopy IV ASIC Design Considerations

The following section describes design considerations for HardCopy IV ASICs.

☐ 15. Review HardCopy IV ASIC specific design considerations.

Among the main design considerations, review the following:

■ Timing constraints—It is especially important to use complete timing constraints if you want to migrate to a HardCopy device because of the rigorous verification requirements for ASICs.

■ RAM contents—RAM cannot be initialized to a known value in the HardCopy ASIC as it can in an HCell. Therefore, if you plan to migrate to a HardCopy device, your design must write RAM contents during device operation instead of relying on memory initialization values.

■ PLL settings—Altera recommends adding the PLL reconfiguration megafunction to your design so that you can change the PLL settings in-system on the HardCopy IV device.

For more information, refer to the *Phase-Locked Loops Reconfiguration (ALTPLL_RECONFIG) Megafunction User Guide*.

In addition, review the HardCopy Readiness Report that is generated during compilation when a HardCopy companion device is selected in the Device Settings. This advises you about any incomplete I/O assignments and provides recommendations for clock pin locations.

Early System and Board Planning

System information related to the HardCopy IV ASIC should be planned early in the design process, before designers have completed the design in the Quartus II software. Early planning allows the HardCopy IV ASIC designers to provide early information to PCB board and system designers. This section includes the following topics:

■ "Early Power Estimation"

■ "Power Supplies" on page 6

■ "Plan for On-Chip Debugging" on page 7

Early Power Estimation

HardCopy IV ASIC power consumption is an important design consideration. Power consumption must be estimated to develop an appropriate power budget and to design the power supplies, voltage regulators, decoupling, heat sink, and cooling system. Power analysis has two significant planning requirements:

■ Thermal planning—The cooling solution sufficiently dissipates the heat generated by the device. In particular, the computed junction temperature must fall within normal device specifications.

■ Power supply planning—Power supplies must provide adequate current to support device operation.

☐ 16. Estimate power consumption with the Early Power Estimator spreadsheet to plan the cooling solution and power supplies before the logic design is complete.

Power Supplies

The HardCopy IV GX device requires multiple power supplies. The pin connection guidelines provide specific recommendations about the type of power supply regulator (linear or switching) and the voltage supply options and restrictions. For example, the transmitter buffer supply VCCHTx has two options—1.5 V and 1.4 V. There are specific data rate restrictions when using 1.5 V. You must understand these restrictions when you select a power supply value.

For more information about power supply options and restrictions, refer to the *HardCopy IV Device Family Pin Connection Guidelines*.

Estimate the power required to run your design. This estimation allows you to select the appropriate power supply modules and to design the power distribution network on your board. Use the Early Power Estimator tool to estimate the transient current requirements.

For more information about the Early Power Estimation tool, refer to the *HardCopy IV PowerPlay Early Power Estimator User Guide*.

If your design is already complete, use the power optimization features available in the HardCopy IV devices.

Board Design Requirements

For improved signal integrity on the high-speed serial interface, follow the best design practices for your power distribution network, PCB design, and stack up.

For detailed guidelines and recommendations about your power distribution network, PCB design, and stack up, refer to the *Board Design Resource Center*.

Plan for On-Chip Debugging

Evaluate on-chip debugging options early in your design process to ensure that your system board, Quartus II project, and design incorporate the appropriate debug tools available with the Stratix IV and HardCopy IV devices. Planning can reduce time spent debugging, and eliminates any need to make changes later to accommodate your preferred debugging methodologies.

For information about using the "Planning Guidelines for Debugging Tools," refer to the *Stratix IV Design Guidelines* Application Note.

Planning Guidelines for Debugging Tools

If you intend to use any of the on-chip debugging tools, plan for the tool when developing the system board, Quartus II project, and the design.

☐ 17. Check whether the loopback features are available for your selected functional mode. The HardCopy IV device provides diagnostic loopback features between the transmitter channel and the receiver channel at the transceiver PCS and PMA interfaces. These loopback features help in debugging your design.

☐ 18. Select an on-chip debugging scheme or schemes early to plan memory and logic requirements, I/O pin connections, and board connections.

☐ 19. If you want to use the On-Chip debugging tools, plan your system and board wit JTAG connections that are available for debugging.

☐ 20. Plan for the small amount of additional logic resources used to implement the JTAG hub logic for JTAG debugging features.

☐ 21. For debugging with the SignalTap II Embedded Logic Analyzer, reserve device memory resources to capture data during system operation.

☐ 22. When designing with HardCopy IV GX transceivers, check whether the loopback features are available for your selected functional mode. HardCopy IV GX devices provide diagnostic loopback features between the transmitter channel and the receiver channel at the transceiver PCS and PMA interfaces. These loopback features help in debugging your design.

Pin Connection Considerations for Board Design

When designing the interfaces to the HardCopy IV device, various factors can affect the PCB design. This section includes important guidelines for the following topics:

■ "Device Power-Up"

■ "Power Pin Connections and Power Supplies" on page 8

■ "Signal Integrity Considerations" on page 9

■ "Board-Level Simulation and Advanced I/O Timing Analysis" on page 10

Device Power-Up

HardCopy IV devices support hot socketing, also known as hot plug-in or hot swap and power sequencing. You can power up a HardCopy IV device without causing undesirable effects to the system.

Although power sequencing is not a requirement for correct operation, you should consider the power-up timing of each rail to prevent problems with long-term device reliability when designing a multi-rail powered system.

☐ 23. Design voltage supply power ramps to be monotonic.

☐ 24. Set the required power supply ramp time (T_{RAMP}) to ensure that the power supplies are stable.

☐ 25. Ensure that all power supply voltages rise monotonically within T_{RAMP}. This ensures that the voltage levels do not remain inderterminate for extended periods during power-up.

👣 For more information about power supply requirements, refer to the *Hot Socketing and Power-On Reset in HardCopy IV Devices* chapter of the HardCopy IV Device Handbook.

Altera uses GND as a reference for hot-socketing operations and I/O buffer designs. Connecting the GND between boards before connecting the power supplies prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND could otherwise cause an out-of-specification I/O voltage or current condition with the Altera device.

Power Pin Connections and Power Supplies

The HardCopy IV core voltage V_{CC} is 0.9 V and the PLL digital power supply V_{CCD_PLL} is also 0.9 V. For HardCopy IV GX devices, the transceiver voltages require additional power supplies at 0.9 V, 1.1 V, 3.0/2.5 V, and 1.4/1.5 V, depending on the data rate.

The I/O voltage V_{CCIO} connections depend on the design's I/O standards and support 1.2, 1.5, 1.8, 2.5, and 3.0 V. I/O standards at 3.3 V are supported with a 3.0-V V_{CCIO} supply.

☞ The device output pins will not meet the I/O standard specifications if the V_{CCIO} level is out of the recommended operating range for the I/O standard. The VCCPD pin must be connected to 3.0-V for a 3.0-V V_{CCIO} and 2.5-V for 2.5 or lower I/O voltages.

👣 For a list of the supply voltages required for the HardCopy IV device and their recommended operation conditions, refer to the *DC and Switching Characteristics of HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

Voltage reference (V_{REF}) pins serve as voltage references for certain I/O standards. The V_{REF} pin is used mainly for a voltage bias and does not source or sink much current. The voltage can be created with a regulator or a resistor divider network.

👣 For details about I/O power pin connections, refer to the *HardCopy IV Device Family Pin Connection Guidelines*.

Decoupling Capacitors

HardCopy IV GX devices include embedded on-package and on-die decoupling for high-frequency decoupling. The built in decoupling reduces the number of external PCB decoupling capacitors, which simplifies PCB design. However, additional external PCB decoupling is still required to design a robust power delivery network.

Altera has created an easy-to-use power distribution network (PDN) design tool that optimizes the board-level PDN graphically. For each power supply, PDN designers must choose a network of bulk and ceramic decoupling capacitors. The PDN design tool provides a fast and interactive way to determine the right number of decoupling capacitors for optimal cost and performance trade-offs.

Board decoupling becomes more significant to improve overall power supply signal integrity with increased power supply requirements.

HardCopy IV GX devices include embedded on-package and on-die decoupling for high-frequency decoupling. The built in decoupling reduces the number of external PCB decoupling capacitors, which simplifies the PCB design. However, additional external PCB decoupling is still required to design a robust power delivery network.

Altera has created an easy-to-use power distribution network (PDN) design tool that optimizes the board-level PDN graphically. For each power supply, PDN designers must choose a network of bulk and ceramic decoupling capacitors. The PDN design tool provides a fast and interactive way to determine the right number of decoupling capacitors for optimal cost and performance trade-offs.

For more information about the PDN design and optimization process, refer to the *Device-Specific Power Delivery Network (PDN) Tool User Guide*.

☐ 26. Use the PDN tool to plan your power distribution netlist and decoupling capacitors.

Signal Integrity Considerations

This section contains references to detailed board design guidelines, as well as a few guidelines related to voltage reference pins, simultaneous switching noise, and I/O termination.

High-Speed Board Design

Board design impacts signal integrity of high speed signals in a system. Altera provides the following application notes that offer information about high-speed board stack-up and signal routing layers:

- *PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing*

- *Via Optimization Techniques for High-Speed Channel Designs*

- *Optimizing Impedance Discontinuity Caused by Surface Mount Pads for High-Speed Channel Designs*

For detailed information about signal integrity and board design, refer to the Board Design Resource Center.

Voltage Reference Pins

Voltage deviation on a V_{REF} pin can affect the threshold sensitivity for inputs.

☐ 27. Design the V_{REF} pins to be noise-free.

For more information about voltage reference pins and I/O standards, refer to "I/O Features and Pin Connections" on page 11.

Simultaneous Switching Noise

Simultaneous switching noise (SSN) becomes a concern when too many pins (in close proximity) change voltage levels at the same time. Noise generated by SSN can reduce noise margin and cause captured data to be incorrect.

For board layout recommendations that can help reduce some of the noise, refer to the PCB guidelines in Altera's Board Design Resource Center.

I/O Termination

Impedance matching is necessary to reduce reflections and improve signal integrity. HardCopy IV on-chip series and parallel termination provide the convenience of no external components. Alternatively, you can use external pull-up resistors to terminate the voltage-referenced I/O standards such as SSTL and HSTL.

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the signal line. HardCopy IV devices provide an optional differential on-chip resistor when using LVDS.

☞ Certain dedicated clock input pairs do not support differential termination.

☐ 28. Check I/O termination and impedance matching for the chosen I/O standards, especially for voltage-referenced standards.

For more information about on-chip termination features and limitations, refer to "I/O Features and Pin Connections" on page 11.

Board-Level Simulation and Advanced I/O Timing Analysis

To ensure that the I/O signaling meets receiver threshold levels on your board setup, perform full board routing simulation with third-party board-level simulation tools using an IBIS model.

When this feature is available in the Quartus II software, select **IBIS** under **Board-level signal integrity analysis** on the **EDA Tool Settings** page of the **Settings** dialog box.

☐ 29. Perform board-level simulation using IBIS models (when available).

For more information about this simulation flow, refer to the *Signal Integrity with Third-Party Tools* chapter of the *Quartus II Handbook*.

You should analyze board level timing as part of I/O and board planning, especially for high-speed designs.

☐ 30. Configure board trace models for Quartus II advanced I/O timing analysis.

You can configure board trace models of selected I/O standards and generate "board-aware" signal integrity reports with the Quartus II software. When **Enable Advanced I/O Timing** is turned on, the TimeQuest Timing Analyzer uses simulation results for the I/O buffer of the output and bidirectional pins in the Pin Planner. The TimeQuest Timing Analyzer also uses the simulation results for the package and board trace model to generate more accurate I/O delays and extra reports to give insight into signal behavior at the system level. You can use these advanced timing reports as a guide to make changes to the I/O assignments and board design to improve timing and signal integrity.

Early Pin Planning and I/O Assignment Analysis

Both HardCopy IV and Stratix IV devices support the same speed, performance, I/O standards, and implementation guidelines. You must set the HardCopy IV companion device for your HardCopy IV design project in the Quartus II software. Otherwise, you may not be able to map to a HardCopy IV device because of the varying amounts of resource availability.

For information about using the early pin planning and I/O assignment analysis, refer to the *I/O Features for HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

Early in the design process, the system architect typically has information about the standard I/O interfaces (such as memory and bus interfaces), IP cores to be used in the design, and any other I/O-related assignments defined by system requirements. The Pin Planner **Create/Import Megafunction** feature interfaces with the MegaWizard Plug-In Manager, and enables you to create or import custom megafunctions and IP cores that use I/O interfaces. Enter PLL and LVDS blocks, including options such as dynamic phase alignment (DPA), because options affect the pin placement rules. When you have entered as much I/O-related information as possible, generate a top-level design netlist file using the **Create Top-Level Design File** command. You can use the I/O analysis results to change pin assignments or IP parameters and repeat the checking process until the I/O interface meets your design requirements and passes the pin checks in the Quartus II software.

When planning is complete, the preliminary pin location information can be passed to PCB designers as described in the previous section. When the design is complete, use the reports and messages generated by the Quartus II Fitter for the final sign-off of pin assignments.

For more information about I/O assignment and analysis, refer to the *I/O Management* chapter of the *Quartus II Handbook*.

I/O Features and Pin Connections

This section provides guidelines related to I/O features and pin connections. It describes support for different I/O signal types and I/O standards in device I/O banks, as well as other I/O features available for your design. It also provides information about memory interfaces, pad placement guidelines, and special pin connections.

For a list of I/O pin locations and connection guidelines, refer to the *HardCopy IV Device Family Pin Connection Guidelines*.

I/O Signaling Type

HardCopy IV devices support a wide range of industry I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards. This section provides general guidelines for selecting a signaling type.

Single-ended I/O signaling provides a simple rail-to-rail interface. Its speed is limited by the large voltage swing and noise. Single-ended I/Os do not require termination, unless reflection in the system causes undesirable effects.

Voltage-referenced signaling provides an improved logic transition rate with a reduced voltage swing, and minimizes noise caused by reflection with a termination requirement. Additional termination components are required for the reference voltage source, V_{TT}.

Differential signaling eliminates the interface performance barrier of single-ended and voltage-referenced signaling, with superior speed using an additional inverted closely-coupled data pair. Differential signaling does not require a voltage reference signal.

HardCopy IV I/O pins are organized in pairs to support differential standards. Each I/O pin pair can support differential input or output operations, with the exception of certain clock pins that support differential input operations only. In your design source code, define just one pin to represent a differential pair, and make a pin assignment for this positive end of the pair. When you specify a differential I/O standard, the Quartus II software automatically places the corresponding negative pin.

☐ 31. Plan signaling type based on system requirements.

☐ 32. Allow the Quartus II software to assign locations for the negative pin in differential pin pairs.

Selectable I/O Standards and Flexible I/O Banks

HardCopy IV I/O pins are arranged in groups called modular I/O banks. Depending on the device package, the number of I/O banks can vary. The size of each bank can also vary.

☐ 33. Select a suitable signaling type and I/O standard for each I/O pin.

☐ 34. Ensure that appropriate I/O standard support is supported in the targeted I/O bank.

Certain I/O banks on the top and bottom or left and right of the device support different I/O standards and voltage levels. You can assign I/O standards and make other I/O-related settings in the Pin Planner. Be sure to use the correct dedicated pin inputs for signals such as clocks and global control signals, as described in "Clock and PLL Selection" on page 16.

☐ 35. Place I/O pins that share voltage levels in the same I/O bank.

☐ 36. Verify that all output signals in each I/O bank are intended to drive out at the bank's V_{CCIO} voltage level.

☐ 37. Verify that all voltage-referenced signals in each I/O bank are intended to use the bank's V_{REF} voltage level.

The board must supply each bank with one V_{CCIO} voltage level for every V_{CCIO} pin in the bank. Each I/O bank is powered by the V_{CCIO} pins of that particular bank, and is independent of the V_{CCIO} of other I/O banks. A single I/O bank supports output signals that are driving at the same voltage as the V_{CCIO}. An I/O bank can simultaneously support any number of input signals with different I/O standards.

To accommodate voltage-referenced I/O standards, each HardCopy IV I/O bank supports multiple V_{REF} pins feeding a common V_{REF} bus. Set the V_{REF} pins to the correct voltage for the I/O standards in the bank. Each I/O bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. If the V_{REF} pins are not used as voltage references, they cannot be used as generic I/O pins and should be tied to V_{CCIO} of that same bank or GND.

An I/O bank including single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting. For performance reasons, voltage referenced input standards use their own V_{CCPD} level as the power source, so you can place voltage-referenced input signals in a bank with a V_{CCIO} of 2.5 V or below. Voltage-referenced bi-directional and output signals must drive out at the I/O bank's V_{CCIO} voltage level.

☐ 38. Check the I/O bank support for LVDS and transceiver features.

Different I/O banks include different support for LVDS signaling, and the HardCopy IV GX device banks include additional support.

For information about the number of channels available for the LVDS I/O standard, refer to the *High-Speed Differential I/O Interface with DPA in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*. For more information about transceiver bank-related features, refer to the *Transceiver Architecture in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

For more information about I/O, refer to the *I/O Features for HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*. Refer to the HardCopy IV I/O banks figure that shows the location of each I/O bank and what each bank supports. The figures describing the number of I/Os in each bank provide bank information specific to each device density. Refer to the section describing I/O bank restrictions for information about which I/O standards can be combined in each bank, and the section describing I/O placement guidelines for details about LVDS restrictions.

For the electrical characteristics of each I/O standard, refer to the *DC and Switching Characteristics of HardCopy IV Devices* chapter the *HardCopy IV Device Handbook*.

HardCopy IV I/O Features

Table 1 lists HardCopy IV I/O features, provides usage information and design considerations, and provides references for more information about the features.

Table 1. HardCopy IV I/O Features [1] **(Part 1 of 3)**

Feature	Usage	Guidelines and More Information
MultiVolt I/O Interface	Allows all packages to interface with systems of different supply voltages. V_{CCIO} pins can be connected to a 1.2-, 1.5-, 1.8-, 2.5-, or 3.0-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply. V_{CCPD} power pins must be connected to 3.0-V for 3.0-V V_{CCIO}, and 2.5-V for other I/O voltages.	Refer to the previous sections and the *I/O Features for HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook* for a summary of MultiVolt I/O support and a list of the supported I/O standards and the typical values for input and output V_{CCIO}, V_{CCPD}, V_{REF}, and board termination voltage (V_{TT}). Altera recommends that you use an external clamp diode on the column I/O pins when the input signal is 3.0 V or 3.3 V.
3.3-V I/O Interface	HardCopy IV I/O buffers support 3.3-V I/O standards as transmitters or receivers in your system. The output high voltage (V_{OH}), output low voltage (V_{OL}), input high voltage (V_{IH}), and input low voltage (V_{IL}) levels meet the 3.3-V I/O standards specifications when the Stratix IV V_{CCIO} voltage is powered by 3.0 V.	To ensure device reliability and proper operation when interfacing with a 3.3 V I/O system, it is important to make sure that the absolute maximum ratings of the HardCopy IV devices are not violated. Altera recommends performing IBIS simulation to determine that the overshoot and undershoot voltages are within the guidelines. For more guidelines, refer to the *I/O Features for HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.
Programmable Output Current Strength	Can mitigate the effects of high signal attenuation due to a long transmission line or a legacy backplane. A higher current strength increases I/O performance, but also increases noise on the interface, so you can use current strength control to manage noise.	Ensure that the output buffer current strength is sufficiently high, but does not cause excessive overshoot or undershoot that violates voltage threshold parameters for the I/O standard. Altera recommends performing IBIS or SPICE simulations to determine the right current strength setting for your specific application. For a list of standards and settings, refer to the *I/O Features for HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.
Programmable Slew Rate Control	Configure each pin for low-noise or high-speed performance. A faster slew rate provides high speed transitions. You can use faster slew rates to improve the available timing margin in memory-interface applications or when the output pin has a high-capacitive loading. A slow slew rate can help reduce system noise, but adds a nominal delay to rising and falling edges. You can use slew rate to reduce SSN.	Confirm that your interface meets its performance requirements if you use slower slew rates. Altera recommends performing IBIS or SPICE simulations to determine the right slew rate setting for your specific application.
Programmable IOE Delay	Programmable delay chains can ensure zero hold times, minimize setup times, or increase clock-to-output times. You can use delays as deskewing circuitry to ensure that all bits of a bus have the same delay going into or out of the device.	This feature helps read and time margins because it minimizes the uncertainties between signals in the bus. For the delay specifications, refer to the *DC and Switching Characteristics of HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

Table 1. HardCopy IV I/O Features [1] **(Part 2 of 3)**

Feature	Usage	Guidelines and More Information
Programmable Output Buffer Delay	Delay chains in the single-ended output buffer can independently control the rising and falling edge delays of the output buffer.	You can use delays to adjust the output buffer duty cycle, compensate channel-to-channel skew, reduce SSO noise by deliberately introducing channel-to-channel skew, and improve high-speed memory-interface timing margins.
Open-Drain Output	When configured as open-drain, the logic value of the output is either high-Z or 0. Used in system-level control signals that can be asserted by multiple devices in the system.	Typically, an external pull-up resistor is required to provide logic high.
Bus Hold	Weakly holds the signal on an I/O pin at its last driven state until the next input signal is present, using a resistor with a nominal resistance (RBH) of approximately 7 kΩ . With this feature, an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated is not required. The circuitry also pulls non-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching.	If the bus-hold feature is enabled, you cannot use the programmable pull-up option. Disable the bus-hold feature if the I/O pin is configured for differential signals. Refer to the *DC and Switching Characteristics of HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook* for the specific sustaining current driven through this resistor and the overdrive current used to identify the next driven input level for each V_{CCIO} voltage level.
Programmable Pull-Up Resistor	Pull-up resistor (typically 25 kΩ) weakly holds the I/O to the V_{CCIO} level when in user mode. Can be used with open-drain output to eliminate the requirement for an external pull-up resistor.	If the programmable pull-up option is enabled, you cannot use the bus-hold feature.
PCI Clamping Diode	Can be used to protect the pin from excessive overshoot voltage in PCI/PCI-X I/O standard interfaces.	Available only in column I/O pins.
On-Chip Termination (OCT)	Driver-impedance matching provides the I/O driver with controlled output impedance that closely matches the impedance of the transmission line to significantly reduce reflections. OCT maintains signal quality, saves board space, and reduces external component costs. Support for on-chip series (RS) with or without calibration, parallel (RT) with calibration, and dynamic series and parallel termination for single-ended I/O standards and on-chip differential termination (RD) for differential LVDS I/O standards.	OCT RS and RT are supported in the same I/O bank for different I/O standards if they use the same V_{CCIO} supply voltage. Each I/O in an I/O bank can be independently configured to support OCT RS, programmable current strength, or OCT RT. You cannot configure both OCT RS and programmable current strength or slew rate control for the same I/O buffer. Differential on-chip termination RD is available in row I/O pins and SERDES block clock pins (CLK 0, 2, 9, 11); it is not supported on column I/O pins, high speed clock pins CLK 1,3,8,10, or the corner PLL clock inputs. Refer to the *I/O Features for HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook* for details about the support and implementation of this feature.
Programmable Pre-Emphasis	Increases the amplitude of the high frequency component of the output signal, and thus helps to compensate for the frequency dependent attenuation along the transmission line.	Refer to the *High-Speed Differential I/O Interfaces and DPA in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

Table 1. HardCopy IV I/O Features [1] **(Part 3 of 3)**

Feature	Usage	Guidelines and More Information
Programmable Differential Output Voltage	Allows you to adjust output eye height to optimize trace length and power consumption. A higher VOD swing improves voltage margins at the receiver end while a smaller VOD swing reduces power consumption.	Refer to the *High-Speed Differential I/O Interfaces and DPA in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.
Dedicated Differential I/O SERDES Circuitry with DPA and Soft-CDR Support	Row I/Os (right and left side) in both HardCopy IV GX devices and E devices have built-in SERDES circuitry that supports high-speed LVDS interfaces at data rates between 150 Mbps and 1.6 Gbps. Dynamic Phase Alignment (DPA) circuitry automatically chooses the best phase to compensate the skew between source synchronous clock and received serial data. Soft-CDR mode provides the opportunity for synchronous/asynchronous applications for chip-to-chip and short reach board-to-board applications for SGMII protocols.	If you want to use DPA, be sure to enable the feature in the MegaWizard Plug-In Manager so that the design uses the correct PLLs on the right and left sides of the device. (Column input buffers are true LVDS buffers. Column output buffers are single-ended, and must have external termination schemes to support LVDS, mini-LVDS, and RSDS standards.) DPA usage adds some constraints on the placement of high-speed differential channels. Refer to the feature description and placement guidelines in the *High-Speed Differential I/O Interfaces and DPA in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

Note to Table 1:

(1) HardCopy I/O Features are masked programmed into the HardCopy device and cannot be changed on Silicon. "Programmable" denotes this can be selected at the Quartus II design phase. It does not imply it is programmable on the HardCopy device.

Consider the following checklist items and refer to the appropriate documentation for detailed guidelines:

☐ 39. Check available device I/O features that can help I/O interfaces: current strength, slew rate, I/O delays, open-drain, bus hold, programmable pull-up resistors, PCI clamping diodes, programmable pre-emphasis, and VOD.

☐ 40. Consider on-chip termination features to save board space.

☐ 41. Check that the required termination scheme is supported for all pin locations.

☐ 42. Choose the appropriate mode of DPA, non-DPA, or soft-CDR for high-speed LVDS interfaces.

☐ 43. If you want to use DPA, be sure to enable the feature so that the design uses the correct PLLs on the right and left sides of the device, and follow the DPA placement guidelines.

Clock and PLL Selection

The first stage in planning your clocking scheme is to determine your system clock requirements. Understand your device's available clock resources and correspondingly plan the design clocking scheme. Consider your requirements for timing performance, and how much logic is driven by a particular clock.

☐ 44. Use the correct dedicated clock pins and routing signals for clock and global control signals.

The dedicated clock pins drive the clock network directly, ensuring lower skew than other I/O pins. Use the dedicated routing network to have a predictable delay with less skew for high fan-out signals. You can also use the clock pins and clock network to drive control signals, such as the asynchronous reset.

☐ 45. Use the device PLLs for clock management.

Specific clock inputs connect to specific PLLs, which can drive specific low-skew routing networks. Analyze the global resource availability for each PLL and the PLL availability for each clock input pin.

Use the following descriptions to help determine which clock networks are appropriate for the clock signals in your design:

■ The global clock (GCLK) networks can drive throughout the entire device, serving as low-skew clock sources for device logic. This clock region has the maximum delay compared to other clock regions, but allows the signal to reach everywhere within the device. This option is good for routing global reset/clear signals or routing clocks throughout the device.

■ The regional clock (RCLK) networks only pertain to the quadrant they drive into. The RCLK networks provide the lowest clock delay and skew for logic contained within a single device quadrant.

■ I/O elements (IOEs) and internal logic can also drive GCLKs and RCLKs to create internally generated global or regional clocks and other high fan-out control signals; for example, synchronous or asynchronous clears and clock enables.

■ PLLs cannot be driven by internally-generated GCLKs or RCLKs. The input clock to the PLL must come from dedicated clock input pins or pin/PLL-fed GCLKs or RCLKs.

■ Periphery clock (PCLK) networks are a collection of individual clock networks driven from the periphery of the HardCopy IV device. Clock outputs from the DPA block, PLD-transceiver interface, row I/O pins, and internal logic can drive the PCLK networks. These PCLKs have higher skew compared to GCLK and RCLK networks and can be used instead of general purpose routing to drive signals into and out of the HardCopy IV device.

☐ 46. Analyze the input and output routing connections for each PLL and clock pin. Ensure PLL inputs come from dedicated clock pins or from another PLL.

For more information about these features and detailed clock connection information, refer to the *Clock Networks and PLLs in HardCopy IV Devices* chapter in the *HardCopy IV Device Handbook*.

If your system requires more clock or control signals than are available in the target device, consider cases where the dedicated clock resource could be spared, particularly low fan-out and low-frequency signals where clock delay and clock skew do not have a significant impact on the design performance. Use the **Global Signal** assignment in the Quartus II Assignment Editor to select the type of global routing, or set the assignment to **Off** to specify that the signal should not use any global routing resources.

PLL Feature Guidelines

Based on your system requirements, define the required clock frequencies for your design, and the input frequencies that will be available to the HardCopy IV ASIC. Use these specifications to determine your PLL scheme. Use the Quartus II MegaWizard Plug-In Manager to enter your settings for the ALTPLL megafunction, and check the results to verify whether particular features and input/output frequencies can be implemented in a particular PLL.

☐ 47. Enable the PLL features and check the settings in the MegaWizard Plug-In Manager.

For more information about setting up your timing constraints to work with the PLL, refer to *AN 471: High-Performance FPGA PLL Analysis with TimeQuest*.

HardCopy IV PLLs provide robust clock management and synthesis for device clock management, external system clock management, and high speed I/O interfaces. HardCopy IV device PLLs are feature rich, supporting advanced capabilities such as clock switchover, dynamic phase shifting, PLL reconfiguration, and reconfigurable bandwidth. HardCopy IV PLLs also support external feedback mode, spread-spectrum tracking, and post scale counter cascading features. All HardCopy IV PLLs have the same core analog structure with only minor differences in supported features. You can use some of the additional features described in the following sections when planning your PLL design.

For more information about the features in the top, bottom, and side PLLs, refer to the *Clock Networks and PLLs in HardCopy IV Devices* chapter in the *HardCopy IV Device Handbook*.

For information about designing your PLL and using the ALTPLL megafunction to take advantage of the features described in this section, refer to the *Phase-Locked Loops Megafunction User Guide (ALTPLL)*.

Clock Outputs

You can connect clock outputs to dedicated clock output pins or dedicated clock networks. PLLs on the top and bottom of the device provide more dedicated clock outputs than the left and right PLLs.

☐ 48. Check that the PLL offers the required number of clock outputs and use dedicated clock output pins.

Clock Switchover

The clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy or for a dual clock domain application, such as a system that turns on the redundant clock if the previous clock stops running. The design can perform clock switchover automatically when the clock is no longer toggling or based on a user control signal (`clkswitch`).

☞ If you use the clock switchover feature to switch between two different reference clocks, ensure that your design is timing closed to both reference clocks.

Dynamic Reconfiguration

You can reconfigure PLL settings to update the output-clock frequency and the PLL bandwidth and to phase-shift in real time, without reconfiguring the entire HardCopy IV device. The ability to reconfigure the PLL in real time is useful in applications that operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output-clock phase dynamically. You can also use this feature to adjust clock-to-out (t_{CO}) delays in real time by changing the PLL output clock phase shift. This approach eliminates the need to regenerate a configuration file with the new PLL settings.

Enable the dynamic reconfiguration feature with the ALTPLL megafunction. You can then make the feature easier to use by instantiating the ALTPLL_RECONFIG megafunction.

For more information about the ALTPLL_RECONFIG megafunction, refer to the *Phase-Locked Loops Reconfiguration (ALTPLL_RECONFIG) Megafunction Users Guide*.

Clock Control Block

Every global and regional clock network has its own clock control block. The control block provides the following features:

■ Clock source selection (with dynamic selection for global clocks)

■ Global clock multiplexing

■ Clock power down (with static or dynamic clock enable or disable)

Use these features to select different clock input signals, or to power-down clock networks to reduce power consumption, without using any combinational logic in your design. In HardCopy IV devices, the clock enable signals are supported at the clock network level instead of the PLL output counter level, so you can turn off a clock even when a PLL is not being used.

☐ 49. Use the clock control block for clock selection and power-down.

For information about using the ALTCLKCTRL megafunction to set up the clock control block, refer to the *Clock Control Block Megafunction User Guide (ALTCLKCTRL)*.

Implementation and Integration

There are three steps to the implementation and integration phase:

■ "Creating Transceiver Instances" on page 20

■ "Creating Reset and Control Logic" on page 23

■ "Creating Data Processing and Other User Logic" on page 23

Creating Transceiver Instances

Use the ALTGX MegaWizard Plug-In Manager to create the transceiver instance. In the architecture phase, you identified the transceiver configuration for your design. Using the ALTGX MegaWizard Plug-In Manager, select the appropriate parameters that apply to your architecture requirements.

Reset and Status Signals

The ALTGX MegaWizard Plug-In Manger provides various reset and status signals:

- Reset signals—`tx_digitalreset`, `rx_digitalreset`, `rx_analogreset`, and `pll_powerdown` are required to reset the transceiver PCS and PMA functional blocks.

- Status signals—`rx_freqlocked` and `pll_locked` indicate the state of the receiver CDR and transmitter PLL, respectively.

☐ 50. Use the reset and status signals to implement the transceiver reset control logic in the HCell fabric.

For more information, refer to "Creating Reset and Control Logic" on page 23. If you determine that your application requires dynamic reconfiguration, select the options in the **Reconfig** screen of the ALTGX MegaWizard interface.

If you intend to dynamically reconfigure the channel into other protocol modes or data rates, the **Reconfig** screen provides multiple options (for example, the **channel interface** and **Use alternate PLL** options) to enable this feature.

👣 To understand the **logical channel addressing, logical PLL index**, and **type of reconfiguration to select** options in the **Reconfig** screen, refer to the "Channel and CMU PLL Reconfiguration Mode Details" section in the *HardCopy IV Dynamic Reconfiguration in Devices* chapter of the *HardCopy IV Device Handbook*.

Depending on your system, when you use multiple transceiver channels, you might be able to share the transmitter and receiver parallel clocks of one channel with the other channels. If your design requires sharing a clock resource, select the `tx_coreclk` and `rx_coreclk` ports.

👣 For information about transceiver-HCell fabric interface clock sharing conditions, refer to the *Transceiver Architecture in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

👣 For more information about using the ALTGX MegaWizard Plug-In Manager and the functionality of the different options and signals available, refer to the *ALTGX Transceiver Setup Guide for Stratix IV Devices* chapter of the *Stratix IV Device Handbook*.

Creating Dynamic Reconfiguration Controller Instances

☐ 51. Use the `ALTGX_RECONFIG` MegaWizard interface to create the dynamic reconfiguration controller instance.

If you intend to use the channel and CMU PLL reconfiguration feature, select the relevant options in the ALTGX_RECONFIG Megawizard Plug-In Manager.

For descriptions of the options in the ALTGX_RECONFIG megafunction, refer to the *HardCopy IV GX ALTGX_RECONFIG Megafunction User Guide* in the *HardCopy IV Device Handbook*.

For more information about using the signals, refer to the *HardCopy IV Dynamic Reconfiguration* chapter of the *HardCopy IV Device Handbook*.

Guidelines for Multiple Data Rate Operation

ALTGX Dynamic Reconfiguration allows you to configure transceivers with different data rates and functional modes. The Quartus II fitter places HCell fabric based on default data rate, protocol, and user constraints.

It is important to define all clock rates and data paths on the transceiver core interface. If you are operating a transceiver with multiple data rates, timing must be constrained and closed on all data rates. This ensures optimal logic placement for all data rates switched by ALTGX Dynamic Reconfiguration.

☞ You cannot dynamically reconfigure from Deterministic Latency mode to any other functional mode or vice-versa. Within Deterministic Latency mode, the following reconfigurations are not allowed:

■ Phase Comp FIFO register mode <– –> non-register mode

■ PFD feedback mode <– –> non-PFD feedback mode

For example, you can dynamically change the data rate for Common Public Radio Interface (CPRI) mode. However, you cannot configure from the CPRI mode to a non-CPRI mode.

Constraining a multiple data rate design requires the following steps:

■ Generating a Synopsys Design Constraint (SDC) file with internal constraints.

■ Defining additional clock rates.

■ Setting clock groups with the Exclusive option.

Use the following sections to complete these steps.

Generating an SDC File with Internal Constraints

Based on the SDC constraints you set, the TimeQuest Timing Analyzer generates a set of SDC constraints, which includes the user constraints and constraints for internal IP nodes. The Quartus II fitter makes logic placements that will meet the timing requirements.

To create full SDC constraints, complete the following steps:

1. Compile a design, which includes the user SDC constraints, default protocol, and data rate settings.

2. Open the TimeQuest Timing Analyzer and run **Netlist Setup**. In the tcl console type `tcl command`, `write_sdc -expand` <*file name*>. This generates a full SDC file, which includes user constraints and embedded constraints for internal nodes.

Defining Additional Clock Rates

To find the specific clock node names for additional clock rates, do the following:

■ In the **Task** window of the TimeQuest Timing Analyzer, open **Diagnostic** and locate the node names for the transceiver boundary in **Report Clock Transfers**.

Node names are either "From Clock" or "To Clock" in the **Setup Transfers** report and listed as: *<node name>*|receive_pcs*<channel>*|clkout or *<node name>*|transmit_pcs*<channel>*|clkout. Take special notice of the entire node name.

☞ The Basic PMA Direct mode has different transceiver-HCell fabric boundaries. The following node names are used: *<node name>*|atx_clk_div0|refclkout for the transmitter and *<node name>*|receive_pma*<channel>*|deserclock[channel number] for the receiver.

Setting Clock Groups with the Exclusive Option

To set the clock groups with the Exclusion option:

1. After you know the node names, open the entire SDC file and locate the nodes you identified in the Clock Transfer Report.

2. Copy the node names and make the modifications shown in Figure 1:

Figure 1. Creating a New Clock Rate *(1)*, *(2)*, *(3)*

Notes to Figure 1:

(1) All modifications are shown in the blue callouts.

(2) Any name can be used.

(3) The multiplication or division factor is a ratio between the original transceiver core interface frequencies and the new frequency.

Insert additional constraints anywhere in the full SDC file and recompile the design. Check for any warnings in the TimeQuest Timing Analyzer. Confirm that the additional clocks have been correctly generated in the clocks report.

Creating Reset and Control Logic

The reset sequence is important for initializing the transceiver functional blocks to proper operating condition. Altera recommends a reset sequence for different transceiver configurations and protocol functional modes.

☐ 52. Use the proper reset sequence for initializing the transceiver functional blocks.

The ALTGX MegaWizard Plug-In Manager provides the `tx_digitalreset`, `rx_analogreset`, `rx_digitalreset`, and `pll_powerdown` signals to reset the different functional blocks of the transceiver. You can reset the CMU PLL or the ATX PLL (based on your selection) using the `pll_powerdown` signal.

The `pll_powerdown` port of transceiver instances that share the same CMU PLL or ATX PLL must be driven by the same logic.

For more information about reset sequences, refer to the *Transceiver Architecture in HardCopy IV Devices* chapter of the *HardCopy IV Device Handbook*.

Creating Data Processing and Other User Logic

A typical transceiver-based design consists of custom data processing and other user logic that must be implemented in the HCell logic fabric, based on your application requirements. In addition to application-specific logic, for specific transceiver configurations you may need additional logic to interface with the transceivers. This section provides examples of such logic.

☐ 53. Ensure that the proper PPM detector value is entered when the receiver CDR is used in manual lock mode.

Each receiver channel contains a CDR that you can use in automatic or manual lock mode. If you use the receiver CDR in manual lock mode, you can control the timing of the CDR to lock to the input reference clock using the `rx_locktorefclk` port or lock to the recovered data using the `rx_locktodata` port. When you use the receiver CDR in manual lock mode, you may need to implement the PPM detector in the HCell fabric to determine the PPM difference between the upstream transmitter and the HardCopy IV GX receiver.

☐ 54. Use the synchronization state machine in manual word alignment mode.

Each receiver channel contains a synchronization state machine in the PCS that you can enable in certain functional modes. The synchronization state machine triggers the loss of synchronization status to the HCell fabric based on invalid 8B/10B code groups. However, the synchronization state machine in the PCS is not available in some functional modes. You may need to implement custom logic in the HCell fabric to indicate the loss-of-synchronization status of the received data.

☐ 55. Implement gear box logic to meet the interface width requirements.

Some protocols require a wider data path than provided by the transceiver interface. For example, the Interlaken Protocol requires 64/67-bit encoding and decoding, but the maximum data path interface in the HardCopy IV GX transceiver is 40 bits. Therefore, you must implement gear box logic to interface the 64/67-bit encoder-decoder with the transceiver interface.

☐ 56. Ensure functional Blocks interface with the transceiver configured in Basic (PMA Direct) mode.

In Basic (PMA direct) mode, all the PCS functional blocks in the transceiver channel are disabled. Therefore, you may need to implement the following blocks and options in the HCell fabric:

■ Word Alignment—To align the byte boundary on the received data.

■ Byte Deserializer—To increase the data path width to the rest of the user logic and to reduce the clock frequency of the data path by two.

■ Phase Compensation FIFO (for bonded channel applications)—Used in bonded channel applications, in which multiple transceiver channels are connected to the same upstream system. For example, one Interlaken Protocol link using 18 transceiver channels. To minimize the global clock routing resources you use, implement a phase compensation FIFO to interface the receiver side of the transceiver interface with the logic in the HCell Fabric.

■ Write side—Use the recovered clock from each channel to clock the write side of the phase compensation FIFO.

■ Read side—Use the recovered clock from any of the channels to clock the read side of the phase compensation FIFO. With this method, you only use one clock resource and the subsequent receive-side logic in the HCell fabric can operate in this single clock domain.

■ Deskew Logic (for bonded channel applications)—In bonded channel applications in which multiple transceiver channels are connected to the same upstream system, the data received between multiple channels are not aligned due to potential skew in the interconnect and the upstream transmitter system. To compensate for the skew, use deskew logic in the HCell fabric.

■ Encoding/Decoding or Scrambling/Descrambling—Many protocols require the transmitter data to be encoded or scrambled to maintain signal integrity. This logic may be required in the HCell fabric based on your application requirements.

Timing Constraints and Analysis

In a HardCopy IV ASIC design flow, accurate timing constraints allow timing-driven synthesis software and place-and-route software to obtain optimal results. Timing constraints are critical to ensure designs meet their timing requirements, which represent actual design requirements that must be met for the device to operate correctly. The Quartus II software optimizes and analyzes your design using different timing models for each device speed grade, so you must perform timing analysis for the correct speed grade. The final programmed device might not operate as expected if the timing paths are not fully constrained, analyzed, and verified to meet requirements.

The Quartus II software includes the Quartus II TimeQuest Timing Analyzer, a powerful ASIC-style timing analysis tool that validates the timing performance of all logic in your design. It supports the industry standard Synopsys Design Constraints (SDC) format timing constraints, and has an easy-to-use GUI with interactive timing reports. It is ideal for constraining high-speed source-synchronous interfaces and clock multiplexing design structures.

The software also supports static timing analysis in the industry-standard Synopsys Primetime software. Specify the tool in the New Project Wizard or the **EDA Tools Settings** page of the **Settings** dialog box to generate the required timing netlist.

A comprehensive static timing analysis includes analysis of register to register, I/O, and asynchronous reset paths. It is important to specify the frequencies and relationships for all clocks in your design. Use input and output delay constraints to specify external device or board timing parameters. Specify accurate timing requirements for external interfacing components to reflect the exact system intent. The TimeQuest Timing Analyzer performs static timing analysis on the entire system, using data required times, data arrival times, and clock arrival times to verify circuit performance and detect possible timing violations. It determines the timing relationships that must be met for the design to correctly function.

You can use the `report_datasheet` command to generate a datasheet report that summarizes the I/O timing characteristics of the entire design.

- ☐ 57. Ensure timing constraints are complete and accurate, including all clock signals and I/O delays.
- ☐ 58. Review the TimeQuest Timing Analyzer reports after compilation to ensure there are no timing violations.
- ☐ 59. Ensure that the input I/O times are not violated when data is provided to the HardCopy IV device.

For more information about timing analysis, refer to the *Quartus II TimeQuest Timing Analyzer* and *Synopsys PrimeTime Support* chapters of the *Quartus II Handbook*.

Recommended Timing Optimization and Analysis Assignments

The assignments and settings described in this section are important for large designs, such as those in HardCopy IV devices.

☐ 60. Turn on **Optimize fast-corner timing** on the **Fitter Settings** page in the **Settings** dialog box.

When the Optimize fast-corner timing option is set, the design is optimized to meet its timing requirements at the Fast Timing process corner and operating condition, as well as at the Slow Timing corner. Therefore, setting this option helps create a design implementation that is more robust across process, temperature, and voltage variations.

In your TimeQuest Timing Analyzer **.sdc** constraints file, use the following recommended constraints as applicable to your design:

☐ 61. Use `create_clock`, `create_generated_clock` to specify the frequencies and relationships for all clocks in your design.

☐ 62. Use `set_input_delay`, `set_output_delay` to specify the external device or board timing parameters.

☐ 63. Use `derive_pll_clocks` to create generated clocks for all PLL outputs, according to the settings in the PLL megafunctions.

☐ 64. Specify the multicycle relationships for LVDS transmitters or receiver deserialization factors for non-Altera IP.

☐ 65. Use `derive_clock_uncertainty` to automatically apply inter-clock, intra-clock, and I/O interface uncertainties.

☐ 66. Use `check_timing` to generate a report on any problem with the design or applied constraints, including missing constraints.

For more guidelines about timing constraints, refer to the *Best Practices for the Quartus II TimeQuest Timing Analyzer* chapter of the *Quartus II Handbook*.

Defining Transceiver Clock Groups

For proper timing analysis, it is important to constrain all transceiver clock groups in the design. This section describes how the transceiver clock relation could vary, and how clocks are needed to be associated or not, according to the transceiver configurations.

Receiver (RX) Clock Association Guidelines

When a PLL is powered up, a phase alignment between the reference clocks and generated clocks can vary.

Similarly, the phase alignment between `rx_clkout` (parallel clock) and the rx refclk of the receiver CDR can also vary. Therefore, they should not be configured to be the same clock group.

If you are using the rx refclk to clock a core logic, it should not be associated with `rx_clkout` in the same clock domain.

If a transceiver is configured in a non-bonded mode, rx_clkout for each RX channel should not be associated with other RX channels because the CDR recovered clock is asynchronous between individual channels.

If a transceiver is configured as bonded mode, rx_coreclkout can be associated with tx_clkout because both clocks share the same clock source from the CMU/ATX PLL.

Rate Matcher Implementation

When a rate matcher is enabled, rx_clkout does not use the recovered clock from the CDR in its own channel and uses the corresponding CMU/ATX PLL clock instead. Therefore, the rx_clkout and CDR recovered clock are not synchronous. Table 2 lists the clock sources for bonded and non-bonded modes with, or without the rate matcher.

Table 2. Clock Sources for HardCopy IV Devices [1]

	Non-Bonded Mode		Bonded Mode	
	tx_clkout	rx_clkout	tx_coreclkout	rx_coreclkout
Rate Matcher	TX CMU / ATX PLL	TX CMU / ATX PLL	TX CMU / ATX PLL	TX CMU / ATX PLL
Without Rate Matcher		CDR recovered clock		

Note to Table 2:

(1) tx_clkout and rx_clkout are used to drive core logic for the non-bonded mode. tx_coreclkout and rx_coreclockout are used to drive core logic for bonded mode.

For a non-bonded mode with the rate matcher, both tx_clkout and rx_clkout are sourcing the clock output from the TX CMU/ATX PLL. When disabled, rx_clkout and tx_clkout are no longer sharing the common clock source, thus they are in different clock domains.

Transmitter (TX) Clock Association Guidelines

Figure 2 shows two clock domains, clock domain 1 from refclk and clock domain 2 from tx_clkout. Similar to the PLL refclk and its output, refclk in clock domain 1 and tx_clkout in clock domain 2 should be treated as different clock domains.

Figure 2. TX Clock Associations
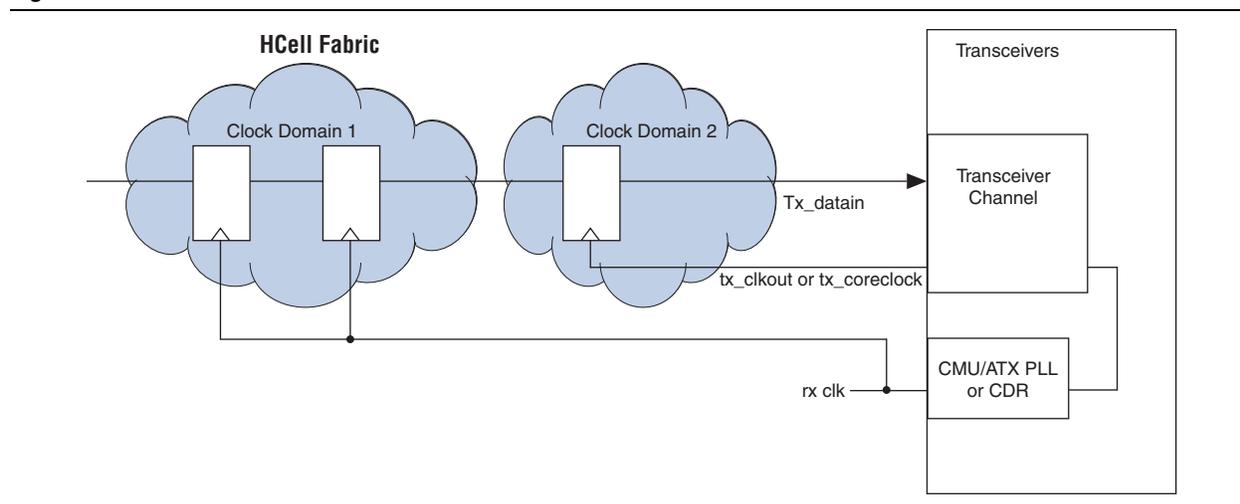
Bonded and Non-Bonded Modes

Regardless of whether the TX channels are configured as bonded or non-bonded mode, the CMU/ATX PLL clock drives all tx channels, thus it can be associated as a single clock group.

xN Line Mode for the Transmitter and Receiver

The ALTGX MegaWizard TX/RX coreclk option allows you to choose the driving source for core logic, so you need only one global or regional clock resource.

When the common clock driver is used to drive core logic, the common clock driver and tx_coreclk[3:0] do not belong to the same clock domain.

The figures below show the two scenarios. Figure 3 shows tx_clkout[0] driving the core logic. Figure 4 shows a common clock driver clocking core logic.

Figure 3. tx_clkout[0] and tx_coreclk[3:0] in the Same Clock Domain
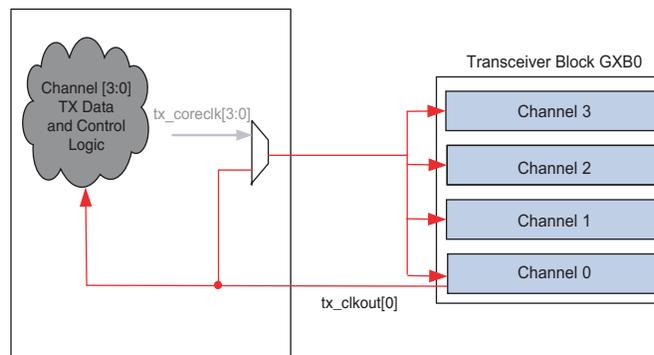
Figure 4. Common Clock Driver and tx_coreclk[3:0] not in the Same Clock Domain
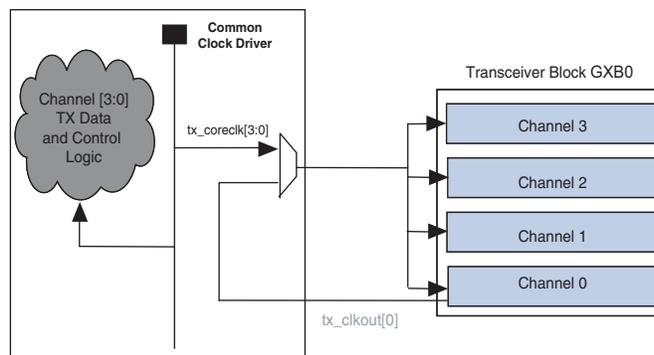
For more information about common clock driver, refer to the *FPGA Fabric-Transceiver Interface Clocking* section in the *Transceiver Clocking in Stratix IV Devices* chapter of the *Stratix IV Device Handbook*.

Document Revision History

Table 3 lists the revision history for this application note.

Table 3. Revision History

Date	Version	Changes
December 2011	1.0	Initial release.

Design Checklist

This checklist provides a summary of the guidelines described in this application note. Use the checklist to verify that you have followed the guidelines for each stage of your design.

Done	N/A	
☐	☐	1. Refer to the device data sheet to ensure that the transceivers meet the data rate and electrical requirements for your target high-speed interface application; for example, the jitter specification and voltage output differential (V_{OD}) range.
☐	☐	2. Check that the device family you select supports your design requirements; for example, the number of transceiver channels, HCell logic density, memory elements, and DSP blocks.
☐	☐	3. Select a HardCopy IV companion device for your HardCopy IV design project in the Quartus II software.
☐	☐	4. Check that the transceiver PCS and PMA functional blocks comply with your system requirements.
☐	☐	5. Check whether the loopback features are available for your selected functional mode. The HardCopy IV device provides diagnostic loopback features between the transmitter channel and the receiver channel at the transceiver PCS and PMA interfaces. These loopback features help in debugging your design.
☐	☐	6. Check whether the Quartus II software might impose any restrictions on combining different transceiver configurations within the same transceiver block.
☐	☐	7. Ensure that your selected device has the required number of input reference clock resources to implement your design.
☐	☐	8. Ensure that the transceiver clock input supports the required I/O standards.
☐	☐	9. Ensure that the clocking restrictions work with your selected device.
☐	☐	10. Check whether the allowed frequencies for the transceiver input reference clocks meet your system requirements.
☐	☐	11. Understand the restrictions for the PLL cascade clock.
☐	☐	12. If you are using the auxiliary transmit (ATX) PLL, understand the recommendations for the input reference clock sources and the restrictions on data rate ranges supported by the ATX PLL.
☐	☐	13. Ensure that the transceiver-HCell logic interface clock frequency limits meet your system requirements.
☐	☐	14. Identify the clocking scheme to clock the transceiver data to the logic in the HCell fabric. If your design has multiple transceiver channels that run at the same data rate and are connected to the one upstream link, you might be able to use a single transceiver-HCell interface clock to provide clocks to the transceiver datapath, which can conserve clock routing resources.
☐	☐	15. If you are using Basic (PMA direct) mode, determine whether you require a left/right PLL to provide phase-shifted clocks to the HCell fabric. The left/right PLL clocks the data received and transmitted between the transceiver and the HCell fabric interface, and may be required to meet the timing requirements of the data transfer.
☐	☐	16. Review the HardCopy IV ASIC specific design considerations.
☐	☐	17. Estimate power consumption with the Early Power Estimator spreadsheet to plan the cooling solution and power supplies before the logic design is complete.
☐	☐	18. Select on-chip debugging scheme or schemes early to plan memory and logic requirements, I/O pin connections, and board connections.
☐	☐	19. If you want to use the On-Chip debugging tools, plan your system and board wit JTAG connections that are available for debugging.
☐	☐	20. Plan for the small amount of additional logic resources used to implement the JTAG hub logic for JTAG debugging features.

Done	N/A	
☐	☐	21. For debugging with the SignalTap II Embedded Logic Analyzer, reserve device memory resources to capture data during system operation.
☐	☐	22. When designing with HardCopy IV GX transceivers, check whether the loopback features are available for your selected functional mode. HardCopy IV GX devices provide diagnostic loopback features between the transmitter channel and the receiver channel at the transceiver PCS and PMA interfaces. These loopback features help in debugging your design.
☐	☐	23. Design voltage supply power ramps to be monotonic.
☐	☐	24. Set the required power supply ramp time (TRAMP) to ensure that the power supplies are stable.
☐	☐	25. Ensure that all power supply voltages rise monotonically within $T_{RAMP.}$ This ensures that the voltage levels do not remain inderterminate for extended periods during power-up.
☐	☐	26. Use the PDN tool to plan your power distribution netlist and decoupling capacitors.
☐	☐	27. Design the V_{REF} pins to be noise-free.
☐	☐	28. Check I/O termination and impedance matching for the chosen I/O standards, especially for voltage-referenced standards.
☐	☐	29. Perform board-level simulation using IBIS models (when available).
☐	☐	30. Configure board trace models for Quartus II advanced I/O timing analysis.
☐	☐	31. Plan signaling type based on system requirements.
☐	☐	32. Allow the Quartus II software to assign locations for the negative pin in differential pin pairs.
☐	☐	33. Select a suitable signaling type and I/O standard for each I/O pin.
☐	☐	34. Ensure that appropriate I/O standard support is supported in the targeted I/O bank.
☐	☐	35. Place I/O pins that share voltage levels in the same I/O bank.
☐	☐	36. Verify that all output signals in each I/O bank are intended to drive out at the bank's V_{CCIO} voltage level.
☐	☐	37. Verify that all voltage-referenced signals in each I/O bank are intended to use the bank's V_{REF} voltage level.
☐	☐	38. Check the I/O bank support for LVDS and transceiver features.
☐	☐	39. Check the available device I/O features that can help I/O interfaces: current strength, slew rate, I/O delays, open-drain, bus hold, programmable pull-up resistors, PCI clamping diodes, programmable pre-emphasis, and VOD.
☐	☐	40. Consider on-chip termination features to save board space.
☐	☐	41. Check that the required termination scheme is supported for all pin locations.
☐	☐	42. Choose the appropriate mode of DPA, non-DPA, or soft-CDR for high-speed LVDS interfaces.
☐	☐	43. If you want to use DPA, be sure to enable the feature so that the design uses the correct PLLs on the right and left sides of the device, and follow the DPA placement guidelines.
☐	☐	44. Use the correct dedicated clock pins and routing signals for clock and global control signals.
☐	☐	45. Use the device PLLs for clock management.
☐	☐	46. Analyze the input and output routing connections for each PLL and clock pin. Ensure PLL inputs come from dedicated clock pins or from another PLL.
☐	☐	47. Enable the PLL features and check the settings in the MegaWizard Plug-In Manager.
☐	☐	48. Check that the PLL offers the required number of clock outputs and use dedicated clock output pins.
☐	☐	49. Use the clock control block for clock selection and power-down.

Done	N/A	
☐	☐	50. Use the reset and status signals to implement the transceiver reset control logic in the HCell fabric.
☐	☐	51. Use the ALTGX_RECONFIG MegaWizard interface to create the dynamic reconfiguration controller instance.
☐	☐	52. Use the proper reset sequence for initializing the transceiver functional blocks.
☐	☐	53. Ensure that the proper PPM detector value is entered when the receiver CDR is used in manual lock mode.
☐	☐	54. Use the synchronization state machine in manual word alignment mode.
☐	☐	55. Implement gear box logic to meet the interface width requirements.
☐	☐	56. Ensure functional Blocks interface with the transceiver configured in Basic (PMA Direct) mode.
☐	☐	57. Ensure timing constraints are complete and accurate, including all clock signals and I/O delays.
☐	☐	58. Review the TimeQuest Timing Analyzer reports after compilation to ensure there are no timing violations.
☐	☐	59. Ensure that the input I/O times are not violated when data is provided to the HardCopy IV device.
☐	☐	60. Turn on **Optimize fast-corner timing** on the **Fitter Settings** page in the **Settings** dialog box.
☐	☐	61. Use `create_clock`, `create_generated_clock` to specify the frequencies and relationships for all clocks in your design.
☐	☐	62. Use `set_input_delay`, `set_output_delay` to specify the external device or board timing parameters.
☐	☐	63. Use `derive_pll_clocks` to create generated clocks for all PLL outputs, according to the settings in the PLL megafunctions. Specify multicycle relationships for LVDS transmitters or receiver deserialization factors.
☐	☐	64. Specify the multicycle relationships for LVDS transmitters or receiver deserialization factors.
☐	☐	65. Use `derive_clock_uncertainty` to automatically apply inter-clock, intra-clock, and I/O interface uncertainties.
☐	☐	66. Use `check_timing` to generate a report on any problem with the design or applied constraints, including missing constraints.