

This application note describes using differential I/O standards in MAX[®] V devices.

High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over the single-ended I/O standards. The Altera[®] MAX V device family supports the emulated LVDS output (LVDS_E_3R) and emulated reduced swing differential signaling (RSDS) output (RSDS_E_3R) I/O standards using two single-ended outputs and external resistor networks, with the second output programmed as an inverted output.

This application note contains the following sections:

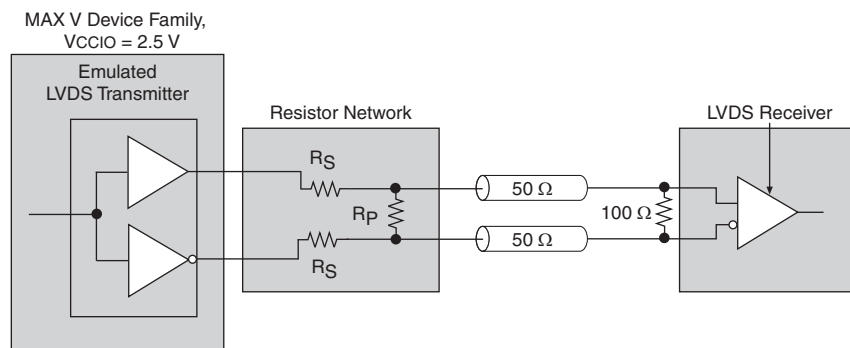
- “Emulated LVDS Output (LVDS_E_3R) I/O Standard” on page 1
- “Emulated RSDS Output (RSDS_E_3R) I/O Standard” on page 2
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Emulated LVDS Output (LVDS_E_3R) I/O Standard

MAX V devices support the emulated LVDS transmitter with a data rate up to 304 Mbps using two single-ended output buffers with external resistors. One of the single-ended output buffers is programmed to have an opposite polarity. The LVDS receiver requires an external 100 Ω termination resistor between the two signals at the input buffer.


Figure 1 shows a point-to-point LVDS interface with a MAX V device using two single-ended output buffers and external resistors.


Figure 1. LVDS Interface with the External Resistor Network for MAX V Devices (Note 1)



Note to Figure 1:

(1) $R_S = 120 \Omega$; $R_P = 170 \Omega$

 MAX V devices meet the ANSI/TIA/EIA-644 requirement standard.

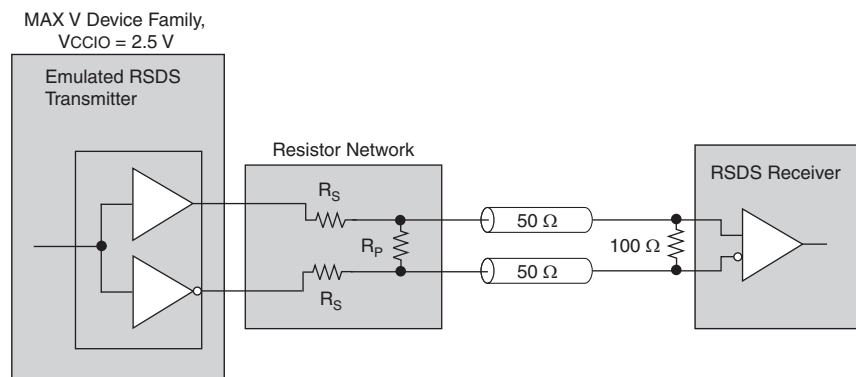
 For more information about the emulated LVDS output electrical specifications for MAX V devices, refer to the *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.

Emulated RSDS Output (RSDS_E_3R) I/O Standard

MAX V devices support emulated RSDS transmitter with a data rate up to 200 Mbps using two single-ended output buffers with external resistors. The two single-ended output buffers are programmed to have an opposite polarity.

Figure 2 shows a point-to-point RSDS interface with a MAX V device using two single-ended output buffers and external resistors.


Figure 2. RSDS Interface with the External Resistor Network for MAX V Devices (Note 1)



Note to Figure 2:

(1) $R_S = 120 \Omega$; $R_P = 170 \Omega$

 MAX V devices meet the National Semiconductor Corporation RSDS Interface Specification.

 For more information about the emulated RSDS output electrical specifications for MAX V devices, refer to the *DC and Switching Characteristics for MAX V Devices* chapter in the *MAX V Device Handbook*.

When using emulated transmitters, you must use a resistor network to attenuate the output voltage swing to meet RSDS specifications. You can modify the resistor network values to reduce power or improve the noise margin.

The resistor values chosen must satisfy [Equation 1](#).

Equation 1.

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50 \Omega$$



Altera recommends performing simulations using MAX V devices IBIS models to validate that custom resistor values meet the RSDS specifications.

I/O Resources

The number of differential output channels varies across device densities and packages. [Table 1](#) lists the number of emulated LVDS and RSDS channels in MAX V devices across various device densities and packages.

Table 1. LVDS and RSDS Channels Supported in MAX V Devices (Note 1)

Device	64-Pin MBGA	64-Pin EQFP	68-Pin MBGA	100-Pin TQFP	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	324-Pin FBGA
5M40Z	10 eTx	20 eTx	—	—	—	—	—	—
5M80Z	10 eTx	20 eTx	20 eTx	33 eTx	—	—	—	—
5M160Z	—	20 eTx	20 eTx	33 eTx	33 eTx	—	—	—
5M240Z	—	—	20 eTx	33 eTx	33 eTx	49 eTx	—	—
5M570Z	—	—	—	28 eTx	28 eTx	49 eTx	75 eTx	—
5M1270Z	—	—	—	—	—	42 eTx	90 eTx	115 eTx
5M2210Z	—	—	—	—	—	—	83 eTx	115 eTx

Note to Table 1:

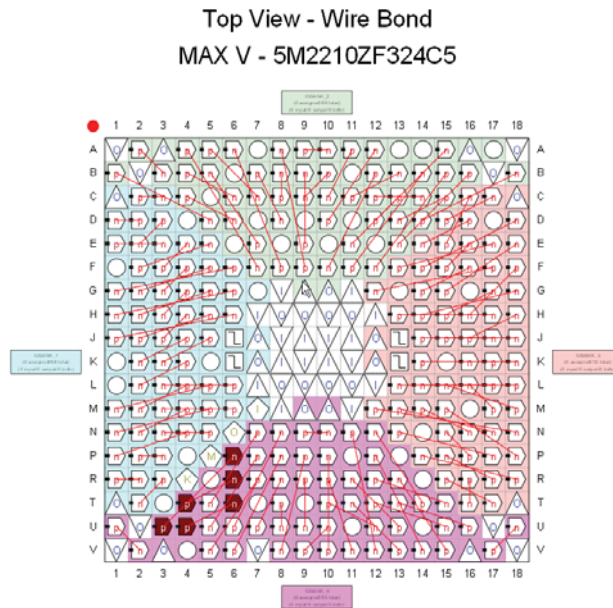
(1) eTx = emulated LVDS output buffers (LVDS_E_3R) or emulated RSDS output buffers (RSDS_E_3R).

Emulated differential output channels are identified as the DIFFIO_<channel_number> [p/n] pins in the **Emulated LVDS Output Channel** column in the [MAX V Device Pin-Out](#).

You can also use the Quartus® II Pin Planner Package view to ease differential I/O assignment planning. On the View menu, click **Show Differential Pin Pair Connections** to highlight the differential pin pairing. The differential pin pairs are connected with red lines. For the differential pins, you only need to assign the signal to a positive pin. If the positive pin is assigned with a differential I/O standard, the negative pin is automatically assigned by the Quartus II software.


Figure 3 shows the differential pin pair connections in the Quartus II Pin Planner for MAX V devices.

Figure 3. Differential Pin Pair Connections in the Quartus II Pin Planner for MAX V Devices



Software Overview

MAX V devices high-speed I/O system interfaces are created in the core logic by the Quartus II software megafunction. The Quartus II software allows you to design your high-speed transmitter using the ALTLVDS_TX megafunction. This megafunction is optimized to use the MAX V device family resources to create high-speed I/O interfaces in the most effective manner.

 When you are using MAX V devices with the ALTLVDS_TX megafunction, the interface always sends the MSB of your parallel data first.

In MAX V devices, one ALTLVDS_TX instance can support up to 18 channels with a deserialization factor of 1 to 10. The ALTLVDS_TX instance in MAX V devices is supported in external phase-locked loop (PLL) mode. A synchronization register must be added before the transmitter megafunction.

Table 2 lists the details of clock generated by the external PLL.


Table 2. Clock Generated by the External PLL

Clock Name	Clock Frequency	
	Odd Deserialization Factor	Even Deserialization Factor
Fast clock, connected to the tx_inclk port (1)	Data rate/2	
Slow clock, connected to the tx_syncclock port	Data rate/(2 × Deserialization factor)	Data rate/Deserialization factor
Clock for synchronization register	Data rate/Deserialization factor	

Note to Table 2:

(1) When the deserialization factor of 1 is selected, the tx_inclk port is not generated. Therefore, the fast clock is not required.

The slow clock requirement is different for the even and odd deserialization factors. All the clock signals must originate from the dual-purpose clock pins, CLK[0..3], that connects to the global clock network.

 You must not use an internally generated clock to clock the fast clock, slow clock, or synchronization register.


 To remove the board skew between the clock signals, Altera recommends having an equal trace length on the clock path from the external PLL to the CLK pin for MAX V devices.

Figure 4 shows an example setup for the ALTLVDS_TX megafunction in MAX V devices for an even deserialization factor.

Figure 4. Example Setup for an Even Deserialization Factor Using the ALTLVDS_TX Megafunction in MAX V Devices

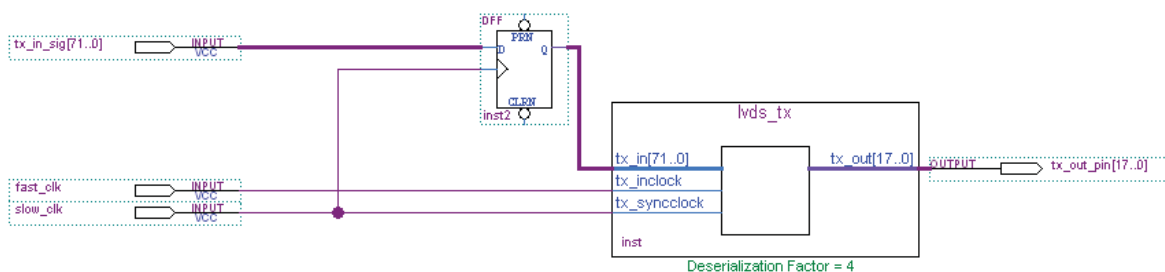
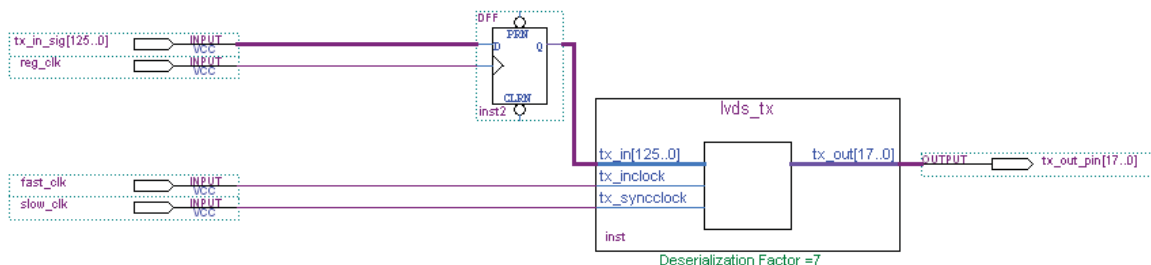


Figure 5 shows an example setup for the ALTLVDS_TX megafunction in MAX V devices for an odd deserialization factor.

Figure 5. Example Setup for an Odd Deserialization Factor Using the ALTLVDS_TX Megafunction in MAX V Devices




You can customize several transmitter settings using the MegaWizard™ Plug-In Manager for MAX V devices, as listed in Table 3.


Table 3. Transmitter Settings Using the MegaWizard Plug-In Manager for MAX V Devices

Option	Description
What is the number of channels?	Number of output channels available for the LVDS transmitter. For example, if the number of channels is 18 , a <code>tx_out[17..0]</code> port is created. One ALTLVDS_TX instance can support up to 18 channels.
What is deserialization factor?	Determines the number of parallel bits from the core which the transmitter serializes and sends out. For example, if the deserialization factor is 10 and the number of output channels is 1 , the transmitter serializes every 10 parallel bits into a single output channel. If the deserialization factor is 5 and the number of output channels is 18 , a <code>tx_in[89..0]</code> port is created.
Use tx_data_reset input port	This option is selectable when the LVDS is implemented in the logic. When you select this option, it adds an input port to the ALTLVDS_TX megafunction, which, when asserted, performs an asynchronous reset for all the logics in the ALTLVDS_TX megafunction.

Constraining the Transmitter Channel-to-Channel Skew

In the TimeQuest Timing Analyzer tool, the `report_tccs` and `report_rskm` commands are not available for MAX V devices. You can use the `set_max_skew` command in the Synopsys Design Constraints File (`.sdc`) to constrain the transmitter channel-to-channel skew. After compilation completes, check the timing report in the TimeQuest Timing Analyzer to ensure your design is able to achieve the maximum skew you have specified in the `.sdc` file and there are no timing violations on the clock setup and hold paths.

 Altera recommends placing all the transmitter outputs in the same I/O bank and close to each other.

 For more information about the `set_max_skew` command, refer to *The Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Document Revision History

Table 4 lists the revision history for this application note.

Table 4. Document Revision History

Date	Version	Changes
January 2011	1.0	Initial release.

