SOPC Builder to Qsys Migration Guidelines

AN-632-2.0 Application Note

This application note describes guidelines and issues for migrating your design from SOPC Builder to Qsys.

Opening an SOPC Builder System in Qsys

To launch Qsys in the Quartus II software, perform the following steps:

1. Click **Qsys** on the Tools menu.
2. Open your SOPC Builder file (**.sopc**) by clicking **Open** on the **File** menu.

   When you open an existing **.sopc** file, Qsys prompts you to clean up SOPC Builder files in your project directory. This option moves SOPC Builder-generated files to a backup subfolder in your project directory, but does not move SOPC Builder-generated HDL files. Altera recommends that you enable this option to back-up your old files.

SOPC Builder to Qsys Transformations

When you open your SOPC Builder system in Qsys, several transformations occur to convert SOPC Builder components into a Qsys-compatible system. This section describes those transformations.

Avalon-MM Bridges

Qsys offers a different set of Avalon® Memory-Mapped (Avalon-MM) Pipeline and Avalon-MM Clock Crossing bridges. If your system uses either type of bridge, Qsys automatically updates them to the new bridges. The parameterization settings for each bridge differ between SOPC Builder and Qsys; however, Qsys migrates all your bridge parameters into the new bridge.

For more information about Qsys Avalon-MM Bridges, refer to the *Qsys Interconnect* chapter in the *Quartus II Handbook*.

Custom Instructions

Qsys transforms Nios® II custom instructions. Following the transformation, your custom instructions appear in the **System Contents** tab. If any custom instructions remain unconnected after the transformation, perform the following steps:

1. Remove the unconnected custom instructions and any associated interconnect components.

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2. Manually add the custom instructions from the Component Library and connect them to their corresponding custom instruction masters.

   The Interrupt Vector and Endian Converter custom instructions have been removed from Qsys. You are able to generate your design, which uses those custom instructions. However, you are not able to locate them in the Component Library. Do not remove these custom instructions if you need them in your design.

Alternatively, you can replace the Interrupt Vector functionality with Vectored Interrupt Controller (VIC).

For more information about the Vectored Interrupt Controller, refer to Vectored Interrupt Controller Core chapter of the *Embedded Peripherals IP User Guide* and *AN 595: Vectored Interrupt Controllers Usage and Applications*.

Tristate Components

For interfacing to off-chip tristate components, Qsys offers a new tristate controller scheme and no longer uses the Avalon-MM Tristate Bridge. In Qsys, tristate interfaces are accessed through an Avalon Tristate Conduit Interface. The implementation has the following three components:

- Generic Tristate Controller
- Tristate Conduit Pin Sharer
- Tristate Conduit Bridge

For more information about Qsys tristate components, refer to the *Avalon Tri-State Conduit Components User Guide*.

Saving the Qsys System

You can rename your SOPC Builder system after opening it in Qsys by saving the system using a different file name. Do not start the name of your system with a device name, for example **cycloneiii_system.sopc**, because you might cause errors during compilation in the ModelSim simulator.

Qsys Components Support

Qsys may display warnings that components are not supported. You can remove unsupported components from the system and replace them with similar components.

User Custom Components

Qsys supports only Tcl-based custom components, in **hw.tcl** format. Qsys does not support peripheral template file (**.ptf**)-based components built with the Component Editor in SOPC Builder version 7.1 or earlier. If you have **.ptf**-based components, you should convert them to Tcl format in SOPC Builder before migrating your design to Qsys.

For more information, refer to *Updating Your Component with SOPC Builder Component Editor Version 7.2 and Later*.

DDR/DDR2/DDR3 SDRAM Controller with ALTMEMPHY

For Stratix III, Stratix IV and Stratix V designs, you cannot use DDR/DDR2/DDR3 SDRAM Controllers with ALTMEMPHY in your design. You should upgrade the design to use DDR2/DDR3 SDRAM Controller with UniPHY.

For more information, refer to *UniPHY Design Tutorials* section in the *External Memory Interface Handbook*.

Phase-Locked Loop

The status signals, such as **locked** and **pdfena**, for the legacy SOPC Builder phase-locked loop (PLL) component are not exported to the top level of Qsys design. If you have a design using this component, you should upgrade it to Avalon ALTPLL (for pre-Stratix V devices) or Altera PLL (for Stratix V and newer devices).

Nios II Processor CPUID

In Qsys, the Nios II processor CPUID value doesn't get assigned automatically. You should manually assign a unique CPUID for each processor in your system by entering it in the **cpuid control register value** field under **Advanced Features** in the parameterization interface.

System ID Peripheral

In your migrated system which uses the system ID peripheral, the software C macro name has been change from `__ALTERA_AVALON_SYSID` to `__ALTERA_AVALON_SYSID_QSYS`. You should update any of your software code, which uses this macro name. This name change does not affect downloading Nios II code to the FPGA.

Qsys Module and Instance Name Changes

In Qsys, the names that you assign to components are the HDL instance names, and Qsys assigns the module names containing the hierarchy path name for the prefix. For example, if you add a parallel I/O component and name it `pio_0` a system named `my_system`, the instance name is `pio_0` and the module name assigned by Qsys is `my_system_pio_0`.

You should verify any file or assignment with dependency on the module and instance names to ensure that they are updated with the new names. Table 1 lists examples of the files affected.

Table 1. Examples of Files Affected by Instance Name Changes

File Type	Example
Synopsys Design Constraints (SDC) timing constraints	If you refer to instance names in timing path constraints, you must update the timing constraints with the new instance names.

Avalon Interface and Interconnect

There are several considerations for Avalon interfaces that require your attention during migration.

Deprecated Avalon-MM Flow Control Signals

The Avalon-MM flow control signals are deprecated. Qsys may report that it cannot find roles for `dataavailable` and `readyfordata`. If your custom component uses Avalon-MM flow control signals, you should redesign the interfaces of your component. Consider adding an Avalon Streaming (Avalon-ST) interface to your component to handle the streaming data while using the Avalon-MM interface for the nonstreaming data. If the signals are not required for the component, you can ignore warnings about these signals.

Deprecated Avalon-MM Flush Signals

Qsys does not support the flush signal in master components. For resolution, any master that relies on flush signals should monitor the read requests, stop issuing read requests when flushing is needed, and ignore all the pending read data returning. When all the data has returned, the flush is complete and the master can begin posting transactions again.

Avalon-MM wait-request Signal

If your Avalon-MM master component is configured to wait until the wait-request signal is deasserted before starting a transaction, the transaction may become deadlocked. You must configure your component to start transactions independent of the status of the wait-request signal.

Avalon-MM Burst Transfers and Arbitration Shares

In SOPC Builder, arbitration shares have no effect on burst-capable masters. In SOPC Builder, a master gains arbitrator grant access based on the burst count that it issues.

In Qsys, you can set arbitration shares to control the number of burst transactions that the arbitrator grants to each burst master. For example, if the arbitration shares value is four and the master burst count is eight, the master is granted four burst transfers over the slave. This is true only for uninterrupted burst accesses; if the bursting master becomes idle, arbitrator access is not locked for all the arbitration shares allocated to the master.

Project Settings

This section discusses system-level parameters on the **Project Settings** tab in Qsys.

Device Family

The device family parameter in Qsys is the same as in SOPC Builder.

Clock Crossing Adapter type

By default, Qsys sets the Clock Crossing Adapter type to **Handshake**; this is the same type of clock crossing adapter as in SOPC Builder. You can change the clock crossing adapter to FIFO, or to the Auto selection that selects between Handshake and FIFO depending on the type of transfer.

Limit Interconnect Pipeline Stages

For a migrated system, Qsys sets the interconnect pipeline stages to zero, to match the latency of SOPC Builder , which does not pipeline the system interconnect fabric. The default setting for new systems is one, which differs from SOPC Builder.

Post System Generation

This section describes post-system generation changes that you must be aware of regarding your migrated system.

IP Variation (.qip) file

Qsys does not add source files to the Quartus II project automatically. Qsys generates an IP variation file (**.qip**) that should be added to your Quartus II project.

Instantiating Qsys System in Quartus II Project

Qsys maintains the same port names for the system that is migrated from SOPC Builder whenever possible. However, for the DDR/DDR2/DDR3 SDRAM Controller with ALTMEMPHY, the `global_reset_n` port name is not migrated when the system is generated in Qsys. For example, if the controller instance name is `altmemddr_0` then the global `reset_n` port is named `altmemddr_0_reset_n`. You should rename your top level instantiation according to this change.

If you are instantiating the Qsys system by block symbols, you should right-click the existing block symbol and click **Update Symbol or Block**. The port layout around the Qsys system symbol differs from the SOPC Builder-generated symbol, so you must rearrange the connections to the symbol accordingly.

You can connect pins to the block symbol generated by Qsys by right-clicking on the block and selecting **Generate Pins for Symbol Ports**. Do not manually connect pins to the block symbol because this causes a Quartus II compilation error.

Reset Input Ports

Your system's top-level file might contain multiple reset input ports for each of the clock inputs in your Qsys system. You can connect all reset input ports to a single reset source in your design. To create a single global reset signal by connecting all reset interfaces together, on the System menu, click Create Global Reset Network.

Document Revision History

Table 2 lists the revision history for this application note.

Table 2. Document Revision History

Date	Version	Changes
May 2011	2.0	Initial release.
December 2010	1.0	Initial Beta release.