




The architecture of the Altera® Stratix® IV GX FPGA is designed to accommodate the widest range of protocol standards spread over multiple data rates and data rate ranges. This application note helps you implement the protocols shown in [Table 1](#) using specific configurations of Stratix IV GX FPGAs with transceivers that are not shown in the ALTGX MegaWizard™ Plug-In Manager of Quartus® II software version 8.0 and later.

**Table 1. Protocol Configurations for Stratix IV GX FPGAs**

Protocols	Refer to
Fibre Channel	"Recommended Configuration to Achieve Fibre Channel Protocol Implementation" on page 2
Interlaken	"Recommended Configuration to Achieve Interlaken Protocol Implementation" on page 4
SF1-5.1	"Recommended Configuration to Achieve SFI-5.1 Protocol Implementation" on page 7
Gigabit-capable passive optical network (GPON)	"Recommended Configuration to Achieve GPON Protocol Implementation" on page 9
Advanced switching interconnect (ASI)	"Recommended Configuration to Achieve ASI Protocol Implementation" on page 11
Serial data converter (SDC) (JESD204)	"Recommended Configuration to Achieve SDC (JESD204) Protocol Implementation" on page 13
SerialLite II	"Recommended Configuration to Achieve SerialLite II Protocol Implementation" on page 15
Serial ATA (SATA) and Serial attached SCSI (SAS)	"Recommended Configuration to Achieve SATA and SAS Protocols Implementation" on page 16

-  The protocol implementations shown in this application note are the recommended implementations. You have the freedom to implement these protocols in any other configurations appropriate to your specific custom implementations according to your system design constraints, requirements, or both.
-  The recommended configurations described in this application note are used by Altera to characterize the respective protocols.
-  Detailed functional descriptions of all the blocks shown in the flow charts that follow are available in the *Transceiver Architecture for Stratix IV Devices* chapter in volume 2 of the *Stratix IV Device Handbook*.

## Recommended Configuration to Achieve Fibre Channel Protocol Implementation

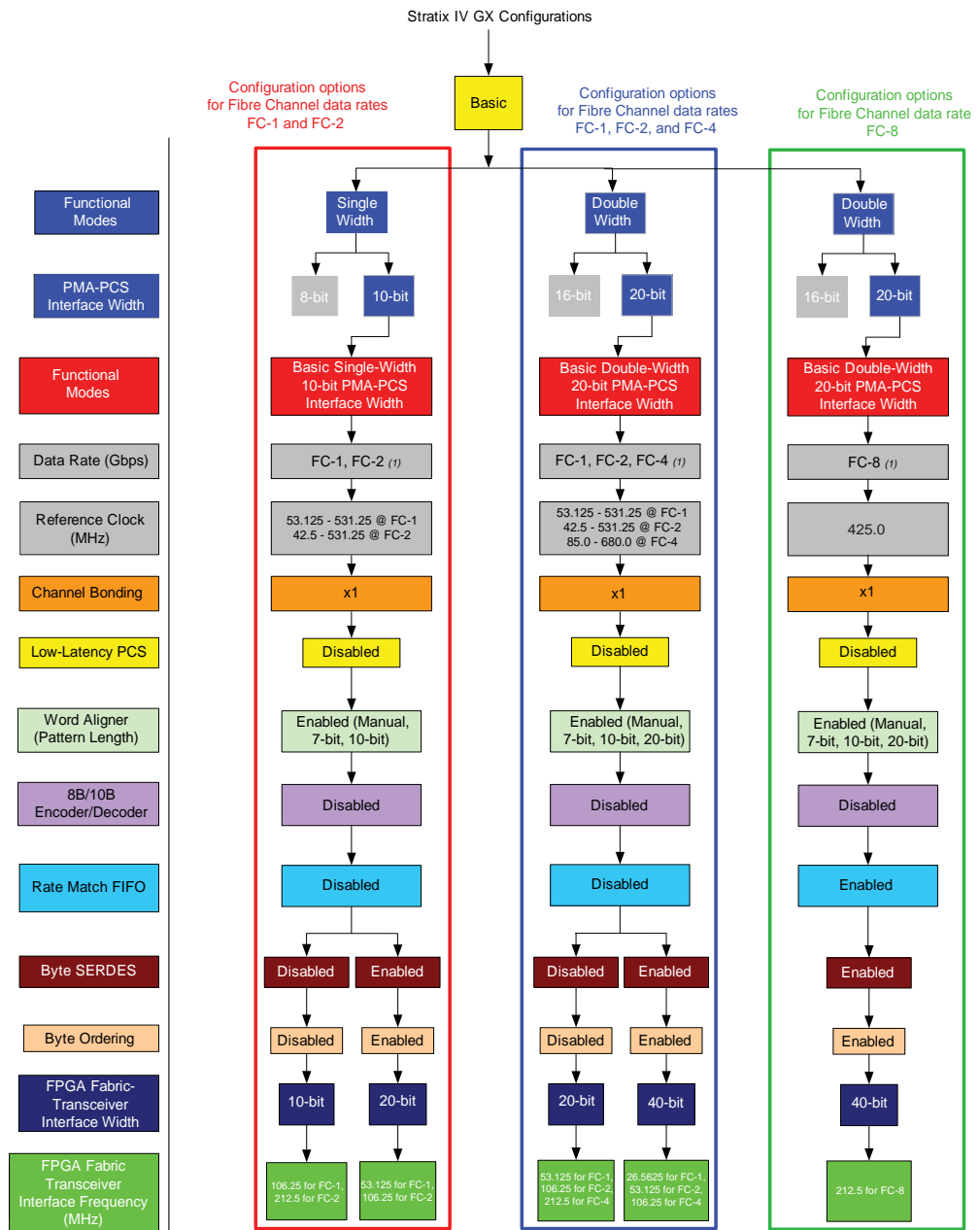
The Fibre Channel protocol manages the transfer of information between different entities within a storage area network (SAN) using a point-to-point link. [Table 2](#) shows the four supported Fibre Channel specifications and their data rates.

**Table 2. Fibre Channel Data Rates for Stratix IV GX Devices**

Fibre Channel Specification	Data Rate (Gbps)
FC-1	1.0625
FC-2	2.125
FC-4	4.25
FC-8	8.5

Although dependent on the system requirements and data rate of the application, any one of the recommended configurations shown in [Figure 1](#) can implement the Fibre Channel protocol in Stratix IV GX transceivers. To use the Fibre Channel protocol, you must add the 8B/10B encoder/decoder to the FPGA fabric.

**Figure 1. Recommended Configurations to Implement the Fibre Channel Protocol in a Stratix IV GX FPGA**



**Note for Figure 1:**

(1) FC-1 = 1.0625 Gbps, FC-2 = 2.125 Gbps, FC-4 = 4.25 Gbps, and FC-8=8.5 Gbps.

## Recommended Configuration to Achieve Interlaken Protocol Implementation

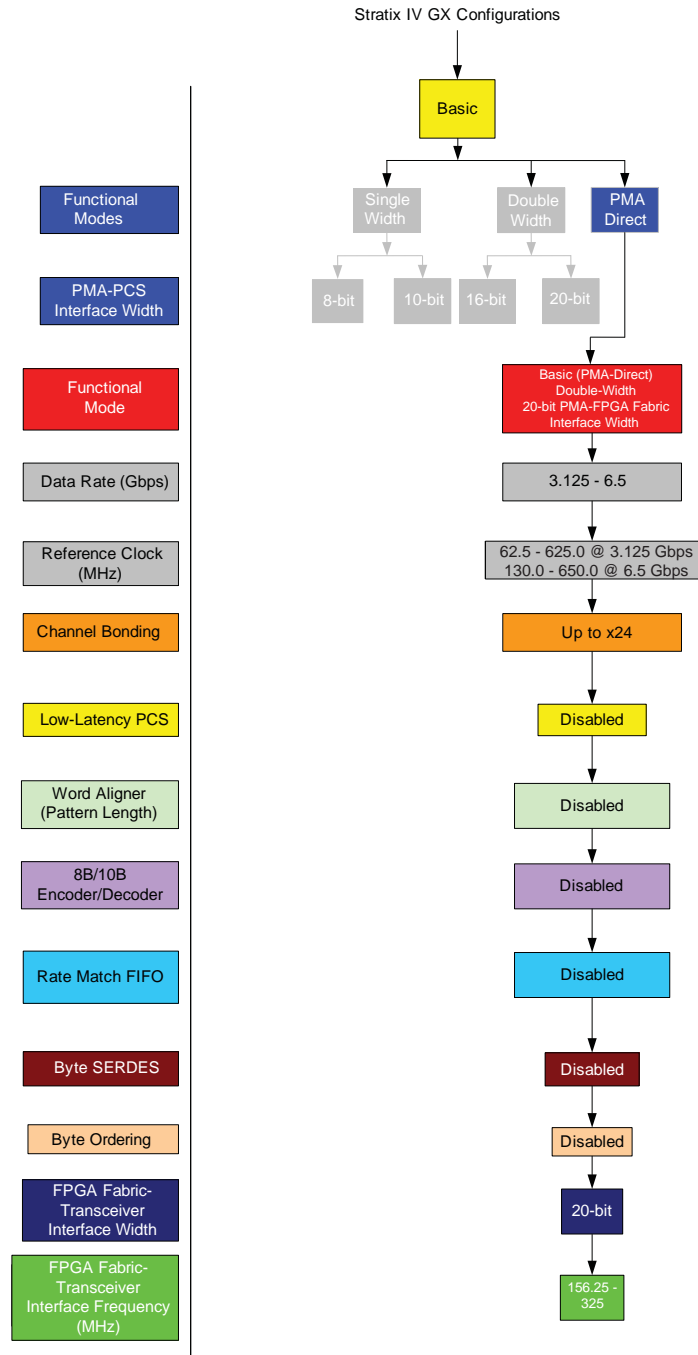
The Interlaken protocol is a serial protocol capable of achieving 10 Gbps to 100 Gbps throughput. Stratix IV GX FPGAs support an Interlaken data rate range of 3.125 Gbps to 6.5 Gbps.

This application note describes the recommended configuration for 24 Interlaken channels on one side of the device. In this configuration, all 24 transmitter channels are configured in Basic (PMA-Direct) double-width mode (Figure 2). All 24 receiver channels are also configured in Basic (PMA-Direct) double-width mode (Figure 3 on page 6).

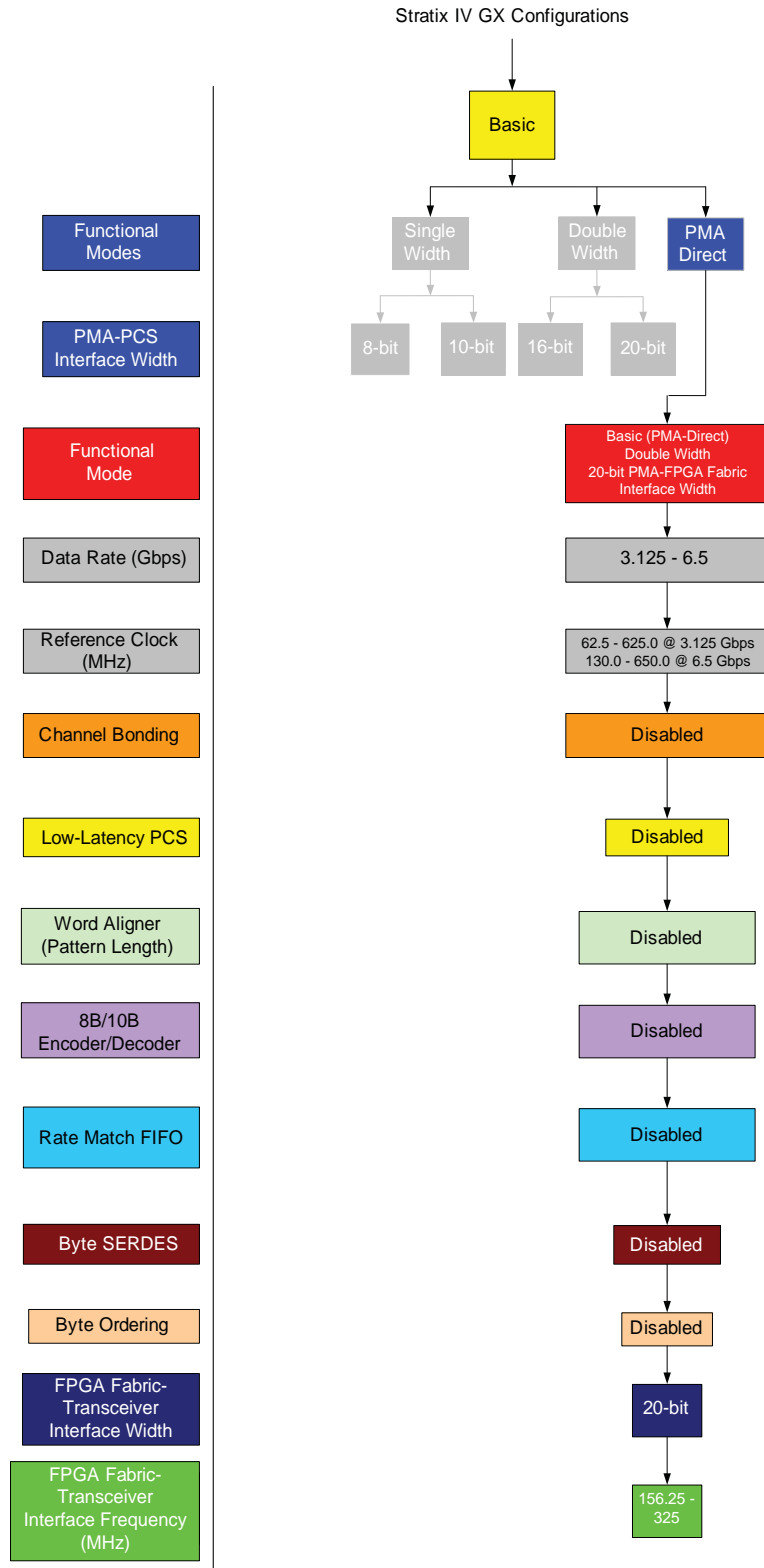
This configuration requires two ALTGX instantiations:

1. Twenty-four **Transmitter-only** channels in Basic (PMA-Direct) double-width mode
2. Twenty-four **Receiver-only** channels in Basic (PMA-Direct) double-width mode

**Figure 2. Recommended Configuration to Implement 24 Transmitter Channels in PMA-Direct Mode for the Interlaken Protocol in a Stratix IV GX FPGA**



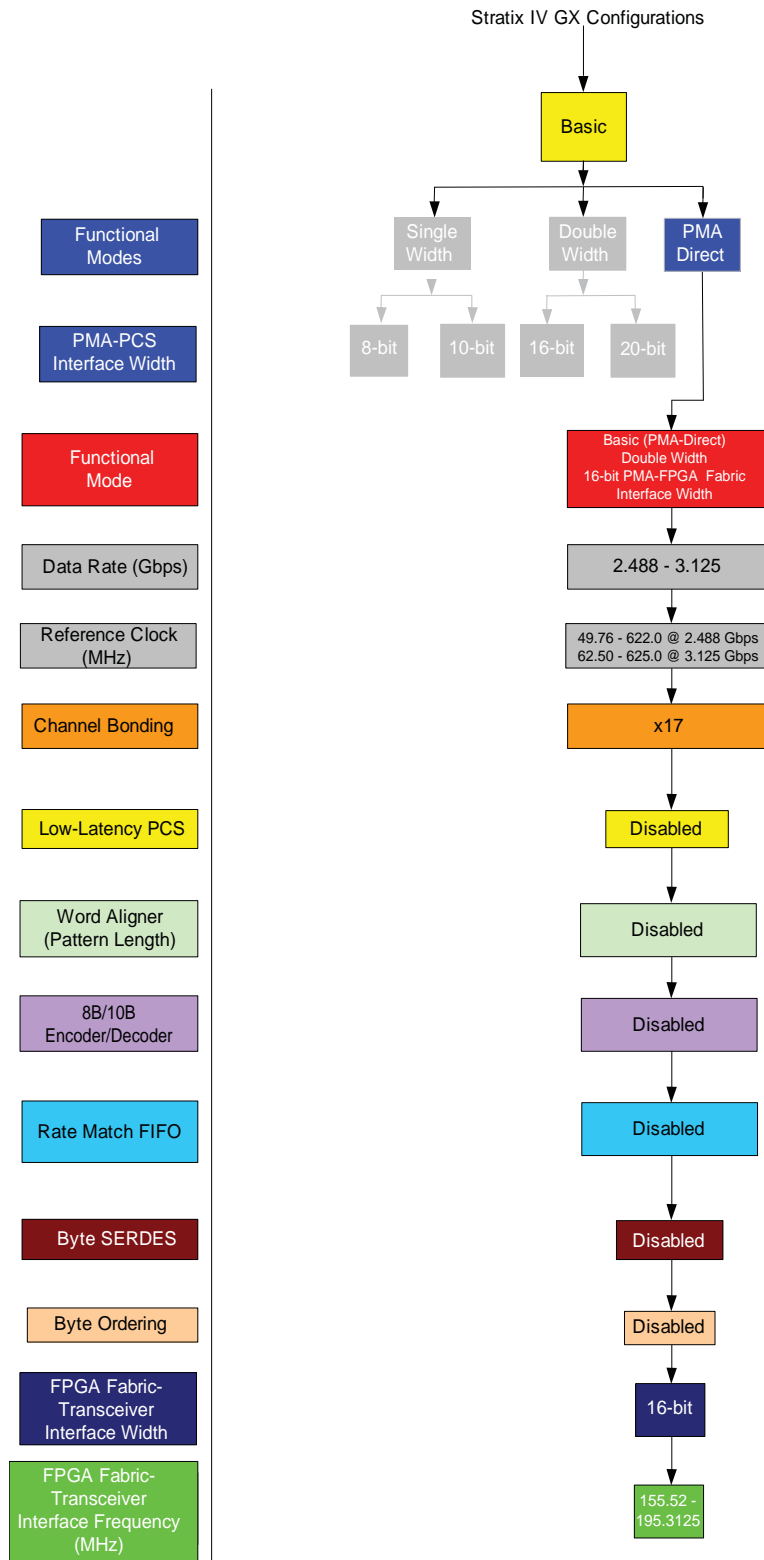
**Figure 3. Recommended Configuration to Implement 24 Receiver Channels in PMA-Direct Mode for the Interlaken Protocol in a Stratix IV GX FPGA**



## Recommended Configuration to Achieve SFI-5.1 Protocol Implementation

The serializer/deserializer (SERDES) Framer Interface Level 5.1 (SFI-5.1) protocol is a serial protocol intended for 40-Gbps applications. The 40G solution comprises 16 data channels and one de-skew control channel, for a total of 17 channels. Stratix IV GX FPGAs support SFI-5.1 data rates from 2.488 Gbps to 3.125 Gbps. [Figure 4](#) shows the recommended configuration to implement the SFI-5.1 protocol with 17 transceiver channels configured in Basic (PMA-Direct) double-width mode.

**Figure 4. Recommended Configuration to Implement 17 Transceiver Channels for the SFI-5.1 Protocol in a Stratix IV GX FPGA**



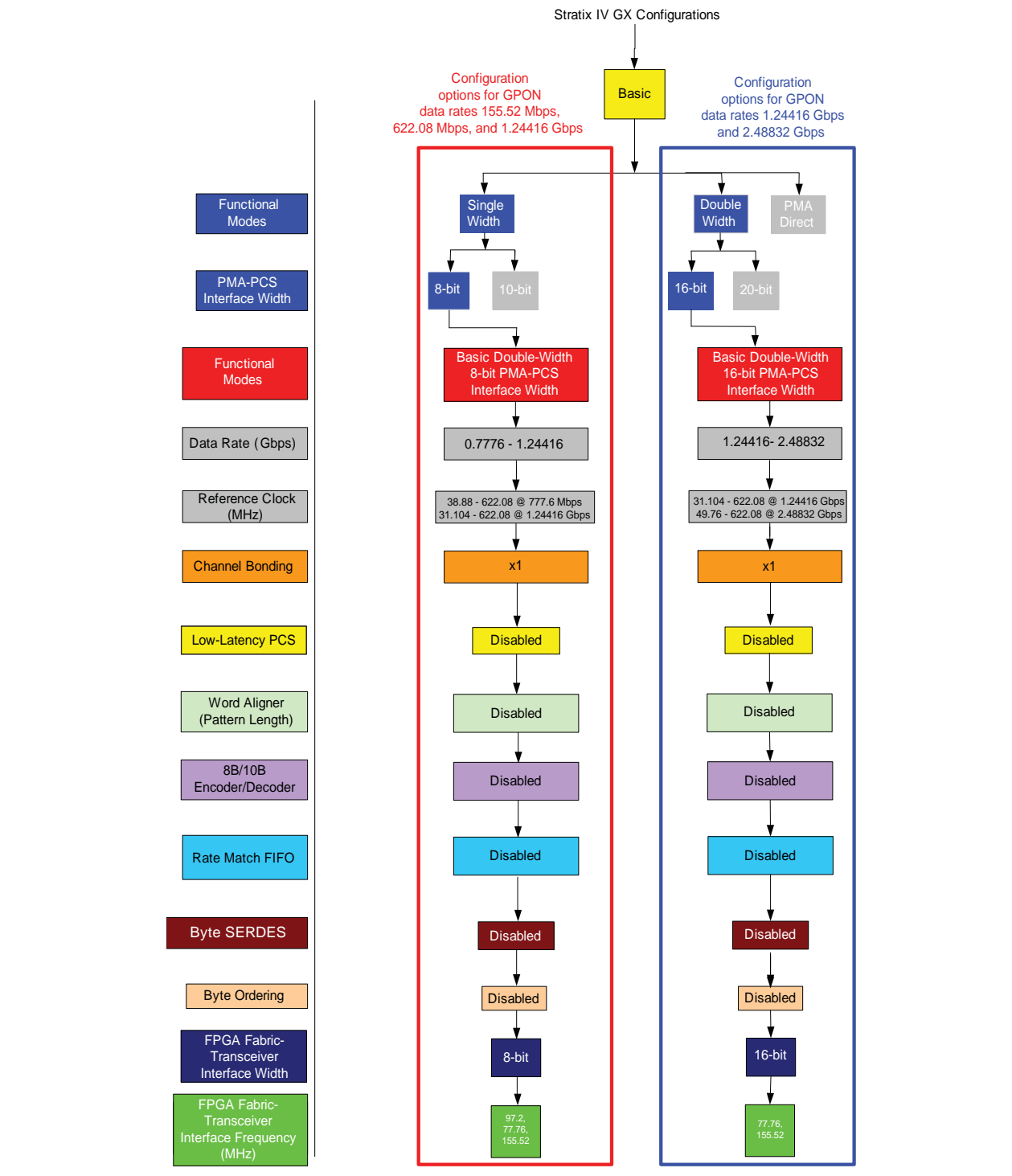


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## Recommended Configuration to Achieve GPON Protocol Implementation

The GPON protocol network provides optical fiber cabling and signals to the home and office using a point-to-multipoint scheme. Stratix IV GX FPGAs support GPON data rates of 155.52 Mbps, 622.08 Mbps, 1.24416 Gbps, and 2.48832 Gbps, with a reference clock of 155.52 MHz. The minimum supported data rate of Stratix IV GX FPGAs is 600 Mbps, so a 5x over-sampling factor is used for the GPON data rate of 155.52 Mbps, resulting in a data rate of 777.6 Mbps. [Figure 5](#) shows the recommended configurations for implementing the GPON protocol in Stratix IV GX FPGAs.

Figure 5. Recommended Configurations to Implement the GPON Protocol in a Stratix IV GX FPGA

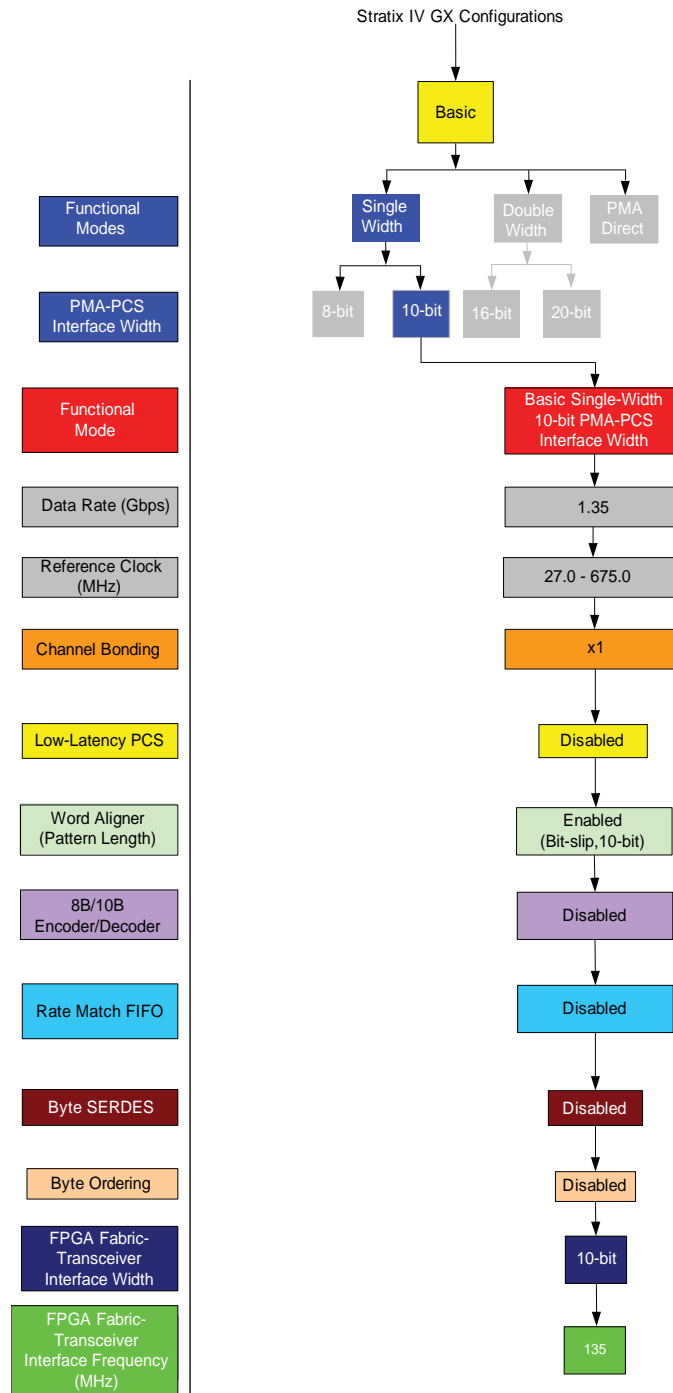


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## Recommended Configuration to Achieve ASI Protocol Implementation

The ASI protocol is a serial data-transmission protocol that carries an MPEG-2 video stream. Stratix IV GX FPGAs support an ASI data rate of 270 Mbps. The minimum supported data rate of Stratix IV GX FPGAs is 600 Mbps, so a 5x over-sampling factor is used for the ASI data rate of 270 Mbps, resulting in a data rate of 1.35 Gbps. [Figure 6](#) shows the recommended configuration for implementing the ASI protocol in Stratix IV GX FPGAs.

Figure 6. Recommended Configuration to Implement the ASI Protocol in a Stratix IV GX FPGA

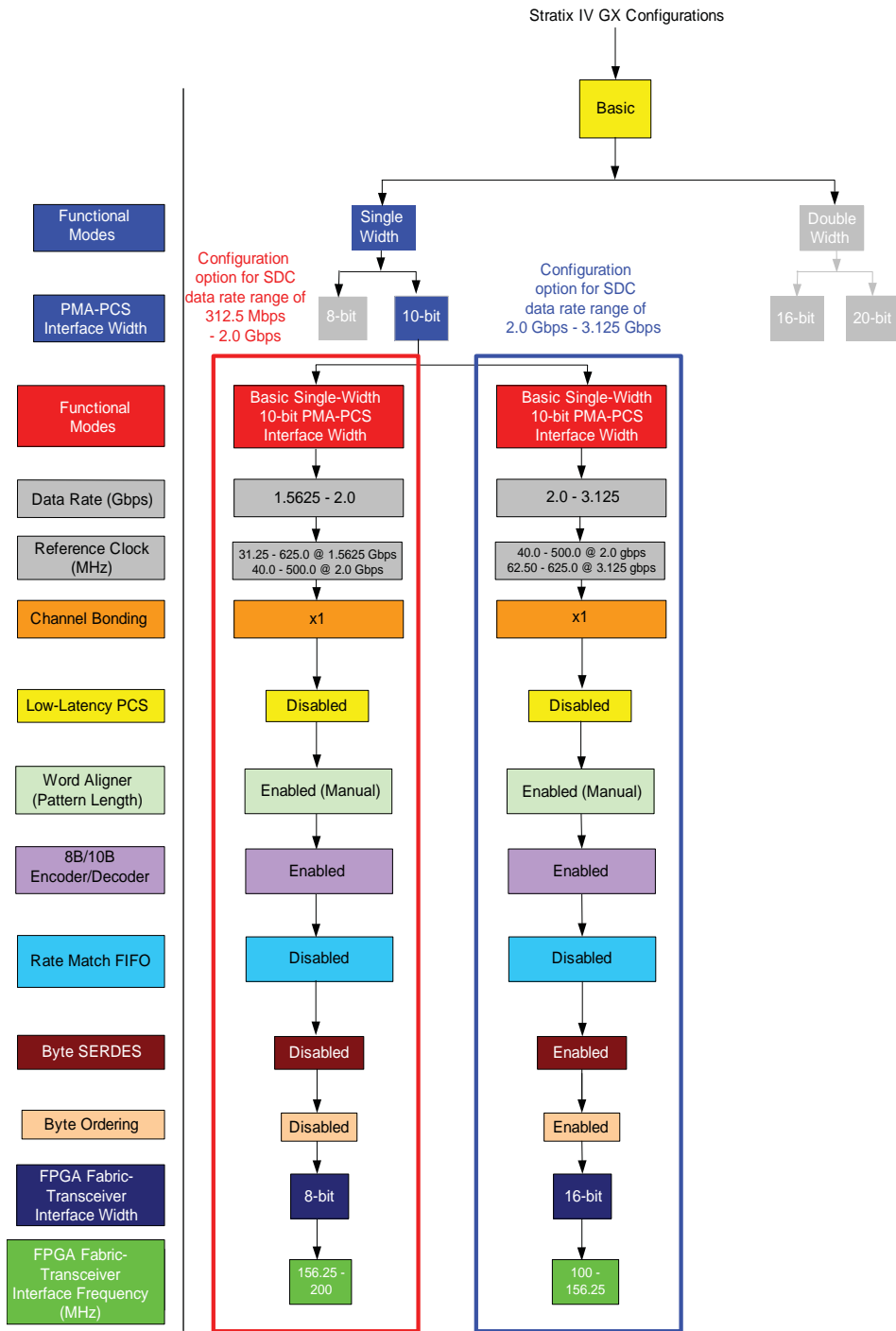


## Recommended Configuration to Achieve SDC (JESD204) Protocol Implementation

The SDC (JESD204) protocol follows JESD204, a JEDEC standard that enables a high-speed serial connection between analog-to-digital converters and logic devices using only a two-wire high-speed serial interface. Stratix IV GX FPGAs support an SDC (JESD204) data rate range of 312.5 Mbps to 3.125 Gbps. The minimum supported data rate of Stratix IV GX FPGAs is 600 Mbps, so a 5x over-sampling factor is used for the SDC (JESD204) data rate of 312.5 Mbps, resulting in a data rate of 1.5625 Gbps.

[Figure 7](#) shows the recommended configurations for implementing the SDC protocol in Stratix IV GX FPGAs.

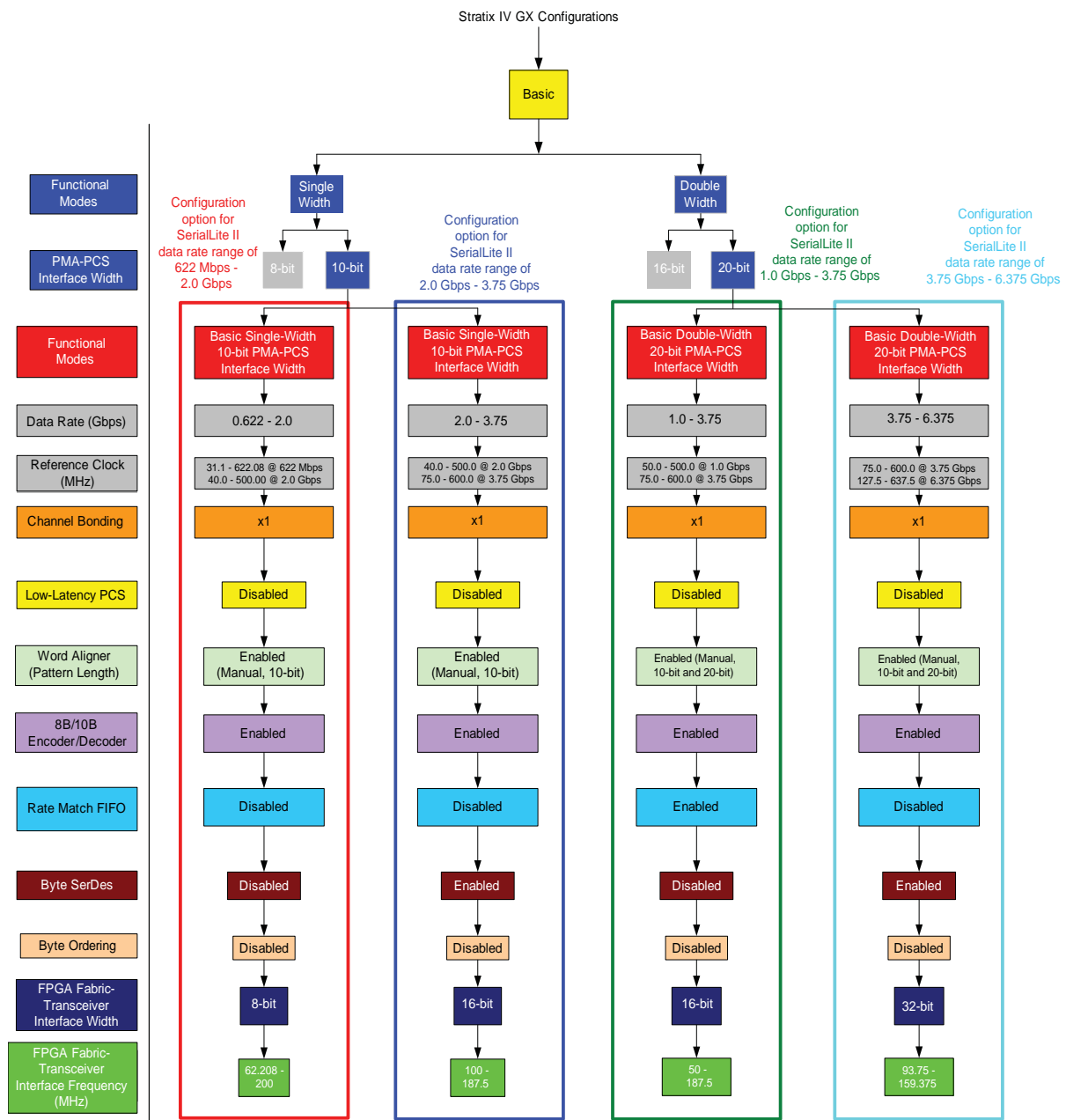
Figure 7. Recommended Configurations to Implement the SDC (JESD204) Protocol in a Stratix IV GX FPGA



# Recommended Configuration to Achieve SerialLite II Protocol Implementation

The SerialLite II protocol is a point-to-point communication protocol for data transmission over one or more lanes. The data rate of each lane can be between 622 Mbps and 6.375 Gbps. Figure 8 shows the recommended configurations for implementing the SerialLite II protocol in Stratix IV GX FPGAs.

Figure 8. Recommended Configurations to Implement the SerialLite II Protocol in a Stratix IV GX FPGA



## Recommended Configuration to Achieve SATA and SAS Protocols Implementation

SATA is a serial interface between the host bus adaptors and the mass storage devices, such as desktop class disk drives used in consumer PCs, workstations, and laptop computing applications. SAS is a serial interface between the host bus adaptors and the mass storage devices, such as enterprise class disk drives used in servers, disk arrays, and datacenter applications.

Table 3 lists the serial data rates supported by Altera's Stratix IV GX devices.

**Table 3. Serial Data Rates for SATA and SAS Protocols in Stratix IV GX Devices**

Protocol	SATA (Gbps)	SAS (Gbps)
Gen1	1.5	1.5
Gen1.1	—	3.0
Gen2	3.0	6.0
Gen3	6.0	—

Figure 9 shows the recommended configurations for implementing the SATA and SAS protocols in Stratix IV GX devices.

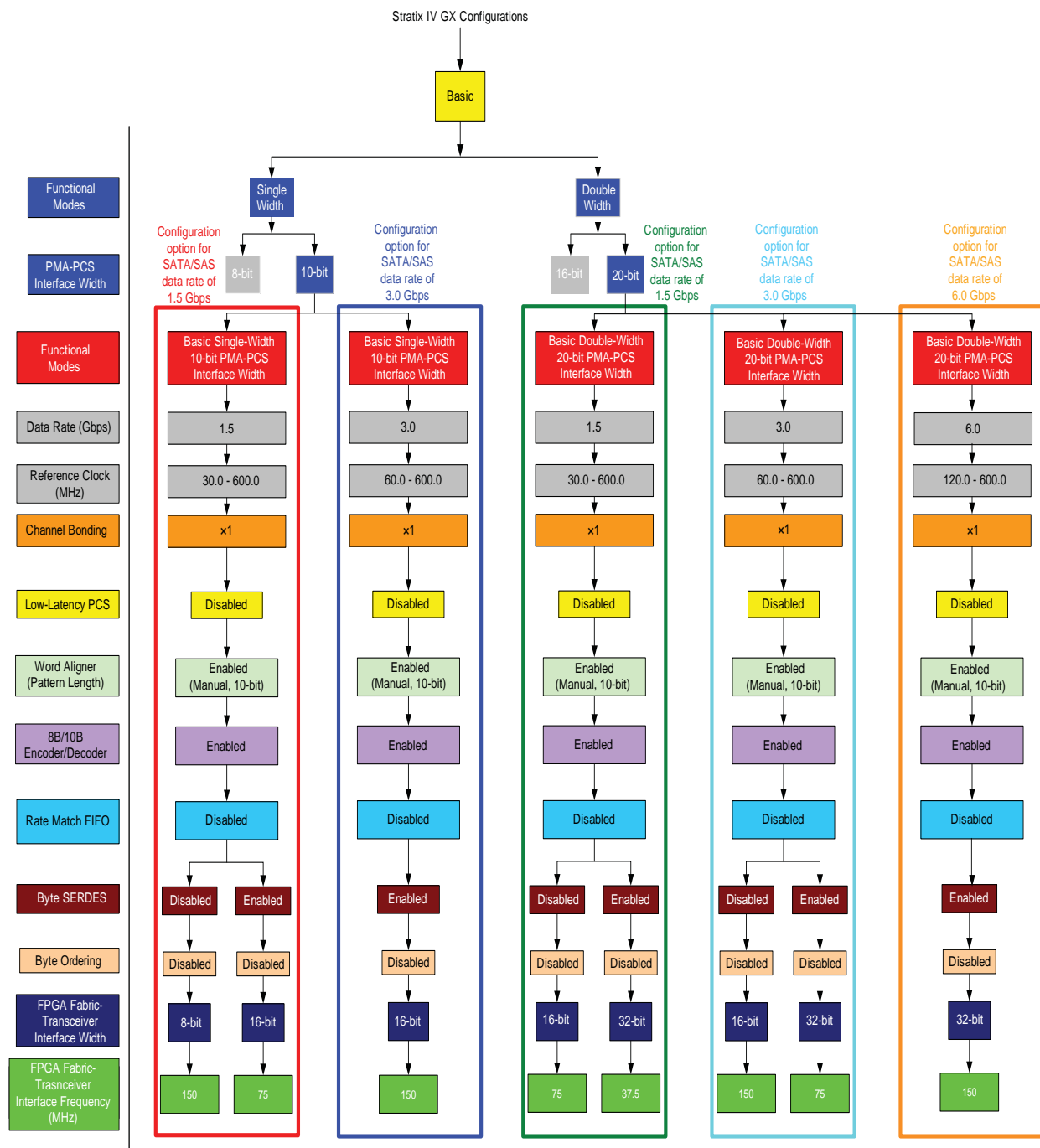
The two main requirements of SATA and SAS protocols, out-of-band signaling (OOB) and speed negotiation, are easily implemented in Stratix IV GX devices.

The OOB signaling required by SATA and SAS protocol's COMINIT, COMWAKE, COMRESET, and COMSAS sequences require the transmitter to be in the electrical idle power save state and the receiver to detect these valid sequence signals on the link. These requirements are easily implemented in Stratix IV GX devices by using the `tx_forceelectidle` port on the transmitter-to-transmit electrical idles and the `rx_signaldetect` port on the receiver-to-detect sequence signal levels above a certain threshold level at the input of the Stratix IV GX receiver. You can set the `rx_signaldetect` threshold using the Quartus II software version 9.1 or later.

The speed negotiation of SATA and SAS protocols requires both the host and device to exchange aligns at the fastest data rate they can both support. This requirement is implemented by using the Stratix IV GX device's capability to dynamically reconfigure data rates.



Figure 9. Recommended Configurations to Implement the SATA and SAS Protocol in a Stratix IV GX FPGA



## Document Revision History

Table 4 lists the revision history for this application note.

**Table 4. Document Revision History**

Date	Version	Changes
March 2011	3.0	<ul style="list-style-type: none"> <li>■ Updated the “Recommended Configuration to Achieve Interlaken Protocol Implementation”, “Recommended Configuration to Achieve GPON Protocol Implementation”, and “Recommended Configuration to Achieve SATA and SAS Protocols Implementation” sections.</li> <li>■ Updated Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, and Figure 9.</li> <li>■ Updated Table 2.</li> <li>■ Added Table 3.</li> <li>■ Removed Figure 4.</li> <li>■ Converted to the new template.</li> <li>■ Minor text edits.</li> </ul>
December 2009	2.0	Added “Recommended Configuration to Achieve SATA and SAS Protocols Implementation” on page 17.
May 2009	1.0	Initial release.