AN 549: Managing Designs with Multiple FPGAs

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Introduction

Managing designs that incorporate multiple FPGAs raises new challenges that are unique compared to designs using only one FPGA. There are several methods for managing multiple FPGAs in a single design, each of which has its pros and cons. One option is to create a master design, partition it into subsections, and assign one or two engineers per subsection. The challenge is not only how to account for signals that cross subsection boundaries, but also how to put the master design back together once the subsections are complete. Another option is to work from the bottom up, handling each section as a separate design, and then, as with the first option, magically put the sections back together to form the master design. The problems with the second option are the same as with the first option except that the second option doesn't give the team the ability to examine the entire design at once. A third option is to give the master design to every team member and establish processes that mitigate the effects of inter-sectional changes. For example, when one designer makes changes that might affect another section of the design that a second designer is working on (where the change might not show up in his work space), a means of communicating these changes must be established among the design team. As you can guess, the challenge with this method is dependent on how rigorously the processes are being adhered to among team members so that when the master design is fully assembled, the team is able to converge on a solution with minimal rework.

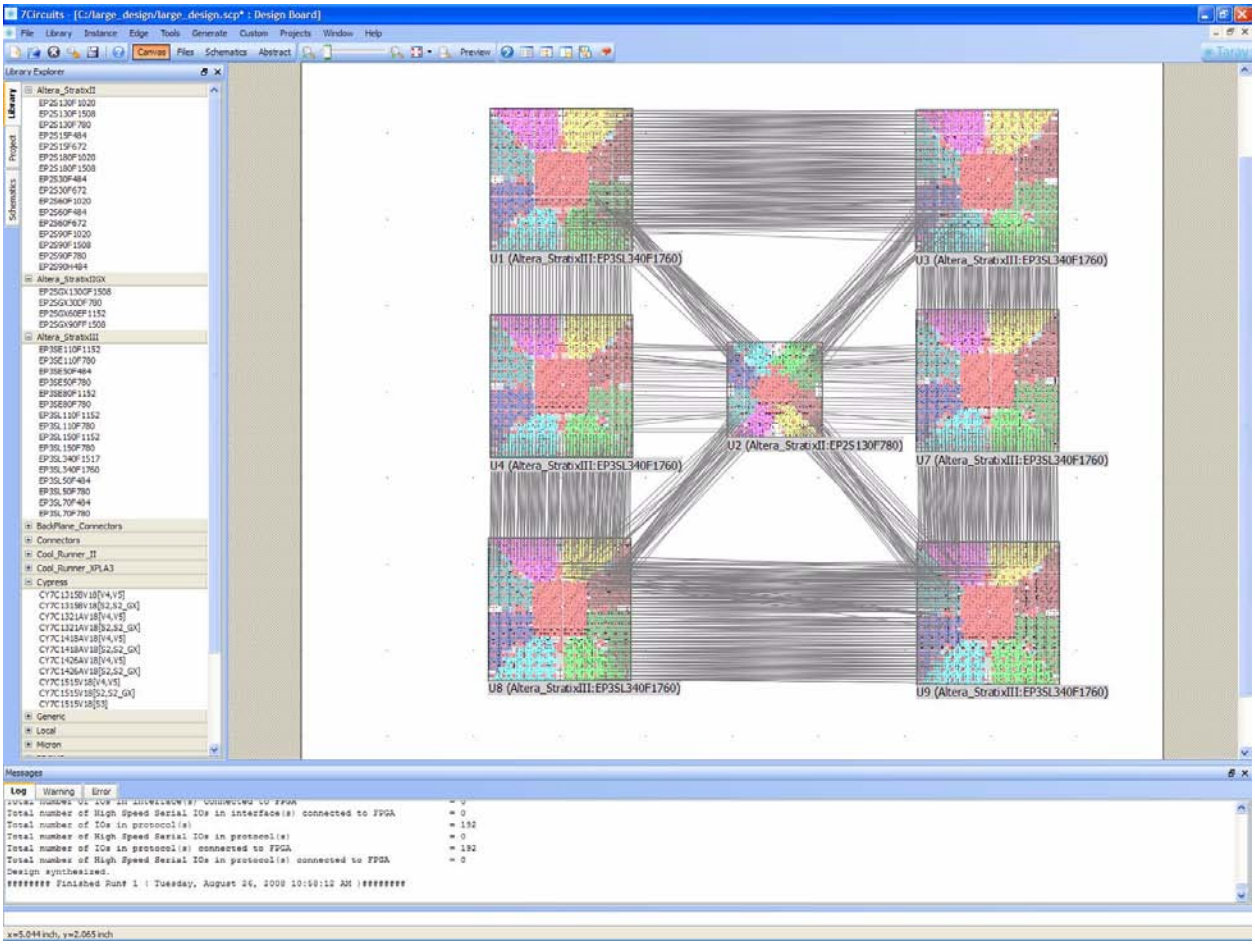
This application note describes a split-and-merge method using the 7Circuits product from Taray that enables easier multiple FPGA design management. This approach helps mitigate the challenges previously described and can help ensure final design success.

Splitting and Merging

Using splitting and merging techniques, large designs can be systematically split into as many subsections as necessary, assigned to multiple engineers, and ultimately subsections can be merged back into the master design. This process can be repeated as many times as needed, allowing for 'snapshots' to be taken of the master as the design progresses. The 7Circuits software also works with a bottom-up flow, in which case an initial master is not needed and is instead created from individually-created subsections.

This example uses six Altera EP3SL340F1760 FPGAs and a single EP2S130F780. The EP3S340FL1760's are connected in a ring fashion using 256 bit data busses while the center EP2S130F780 connects to each of the EP3S340's using 32 separate signals for each. This design will be referred to as the "master" design.

Figure 1. Master Design



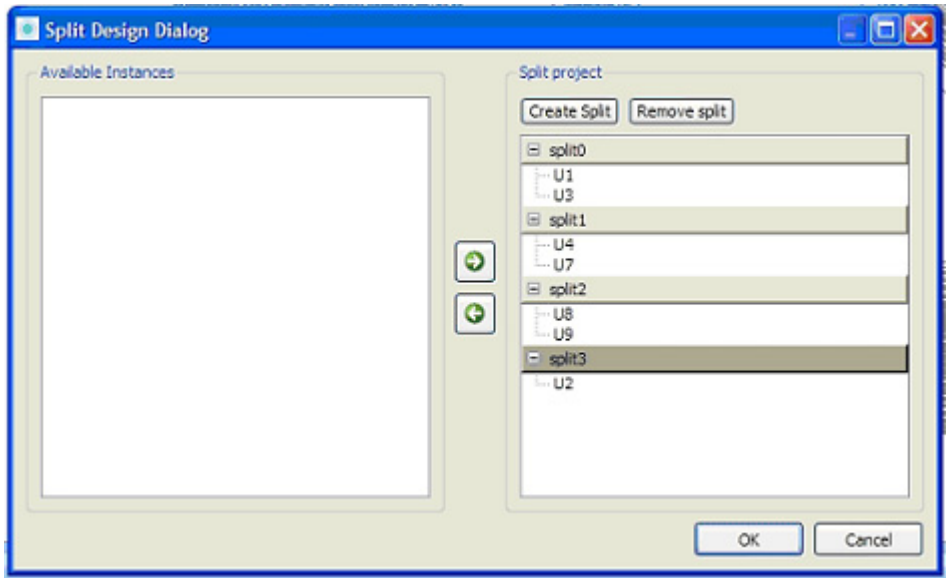
If a master design already exists, you can easily split it into smaller sections (Figure 1). The following steps and figures show the process necessary to accomplish the split and merge technique using the 7Circuits software.

1. On the **File** menu in the 7Circuits software, click **Open...** to load the Master Design.

2. On the **File** menu, click **Split Project**. This step opens a dialog box (Figure 2) that allows you to create splits in your design and add FPGAs to those splits.
3. Split your Master Design. All devices in the design must be placed in a split.
   a. In the **Split Design Dialog** box, click **Create Split**. Select the newly created split.
   b. From the **Available Instances** list, select an instance. Click the right green arrow to move the instance into the selected split.
   c. Repeat steps a and b until all instances are placed in a unique split. All devices in the design must be placed into a split.

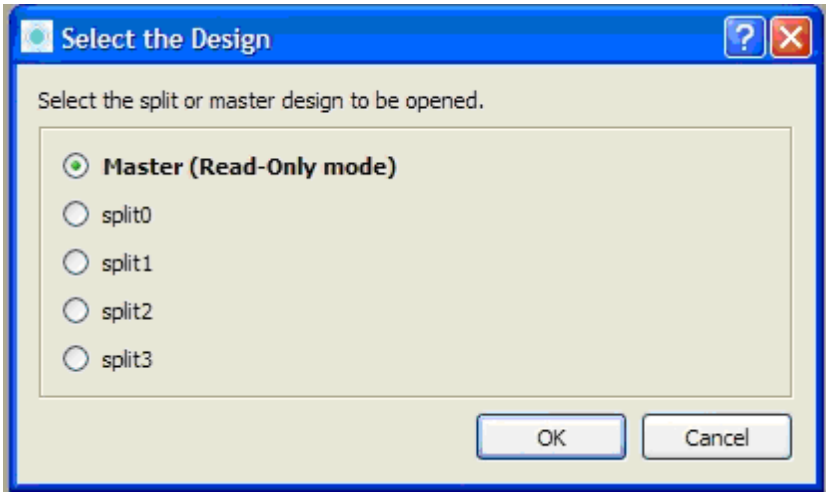
      In the example shown in Figure 2, four splits have been created, split0 to split3. The top two, middle two, bottom two, and center FPGA's have each been placed in a different split.

Figure 2. Split Design Dialog



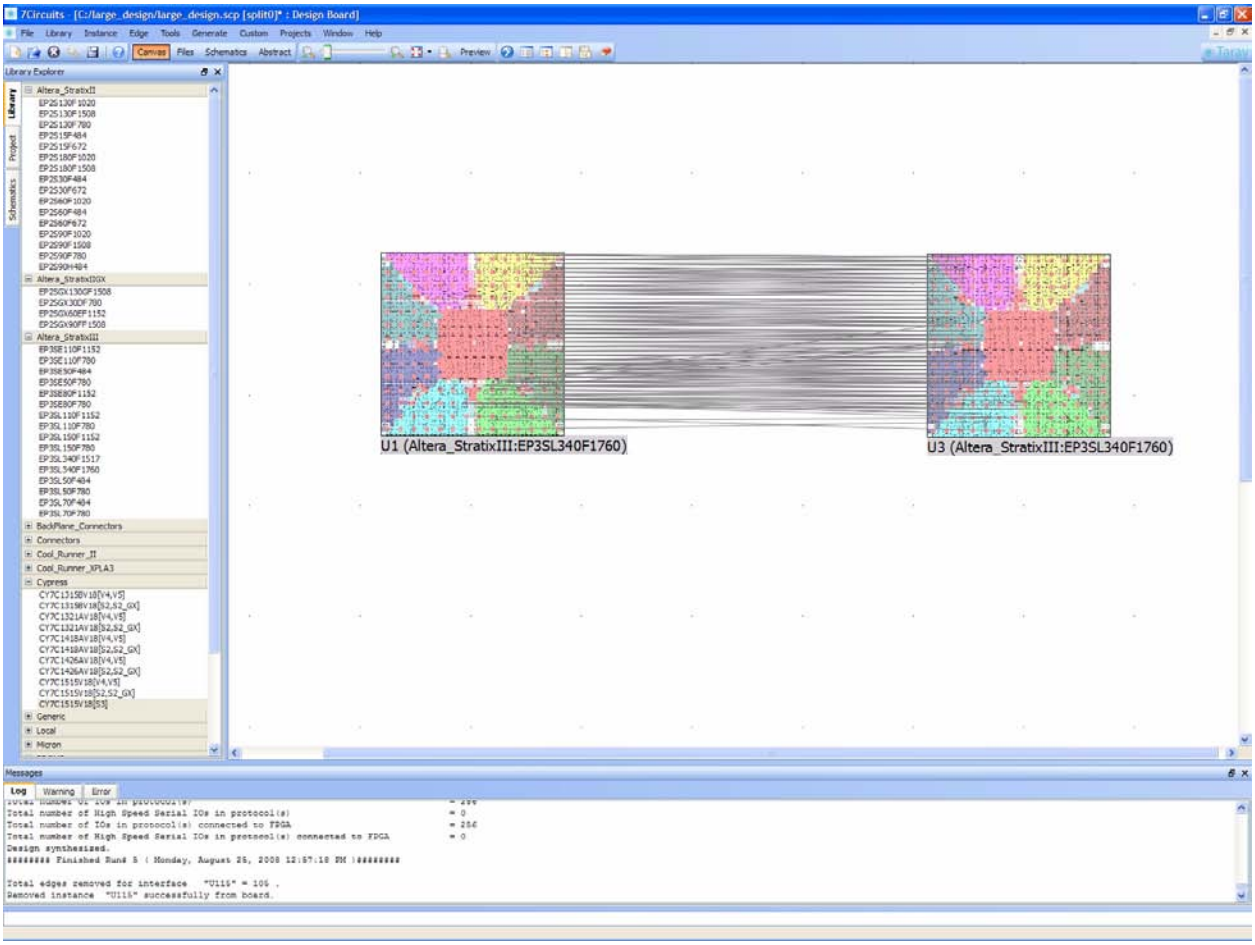
4. Once the master design is split, each split can be worked on as its own project. Close the master design.
5. Reopen the master design as you normally would. The **Select the Design** dialog box appears prompting you to select one of the splits that has been created (Figure 3).
6. Select a split and click **OK**.

Figure 3. Select Split Dialog



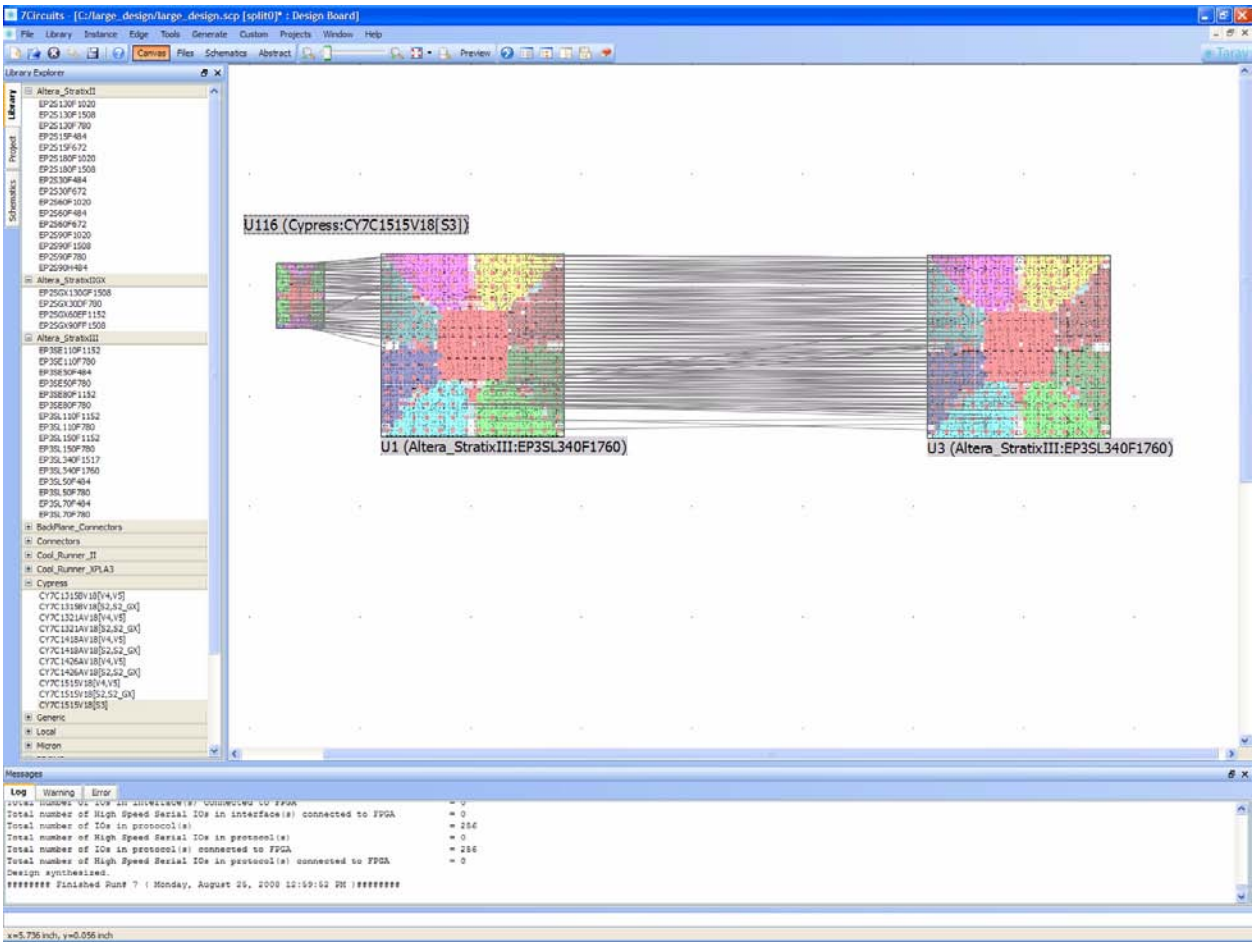
7. In Figure 4, split0 has been opened. At this point you can add components to this split as you normally would, but any components that have connections to other splits cannot be deleted.

Figure 4. Example Split Created from Master Design



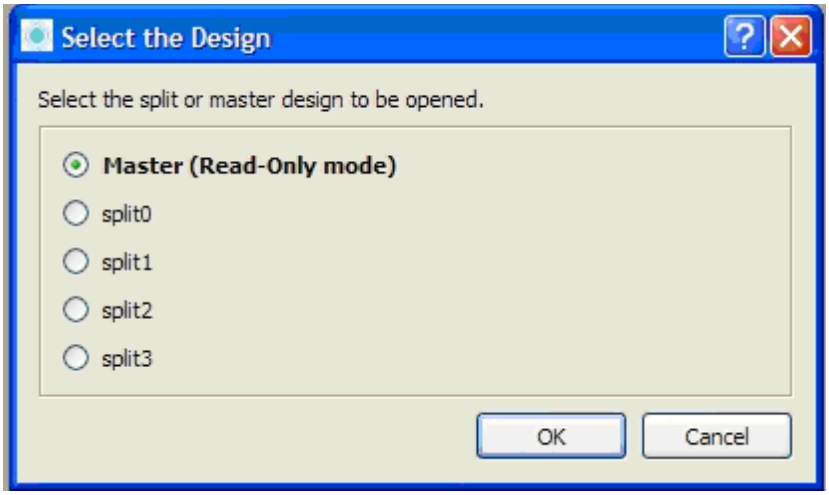
8. Edit the split as a stand-alone design. In Figure 5, a Cypress memory device has been added to the split and the design resynthesized. While not readily apparent in this figure, in order to get the Cypress device to connect to the left edge of the left FPGA (U1), the connections between the two FPGAs also had to be optimized. This is one of the benefits of working on the design at a smaller level; details like these are more obvious and easier to manage.

Figure 5. Cypress Memory Device Added to Split



9. After all edits have been made to the individual splits, the splits can be merged to recreate the master design. To do this, close the split, and reopen the master design (it will open in **Read Only Mode**).

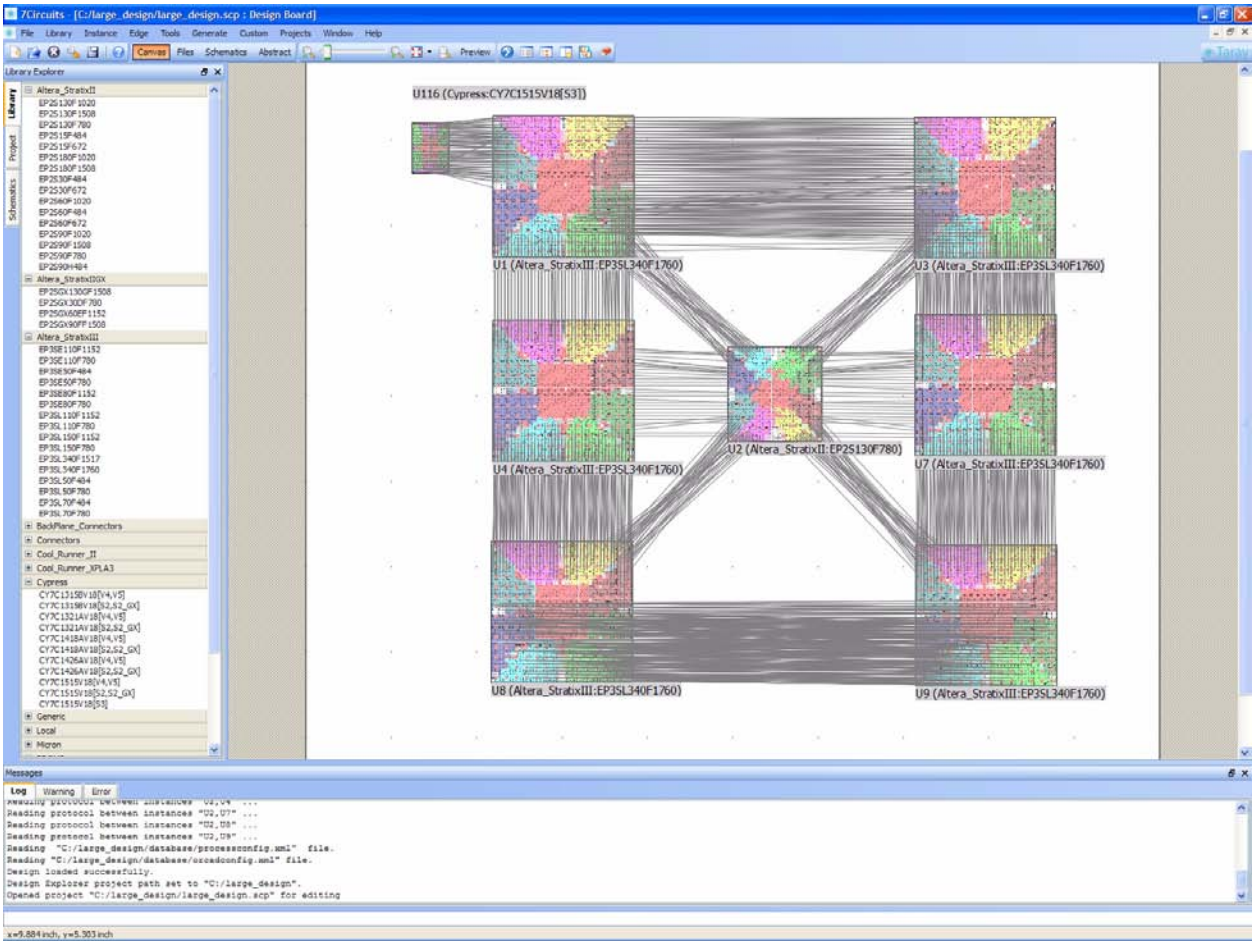
Figure 6. Open Master Design to Prepare to Merge



10. On the **File** menu, select **Merge Current Project**. The splits merge back into the master design.

If, during the process of editing the individual splits, net name or reference designator conflicts were inadvertently created, a dialog box appears that allows you to manually or automatically resolve any conflicts. In Figure 7, the master design has been merged and you can see the Cypress memory device added to what was split0. This new master design looks similar to the original master design as shown in Figure 1.

Figure 7. Master Design with Splits Merged



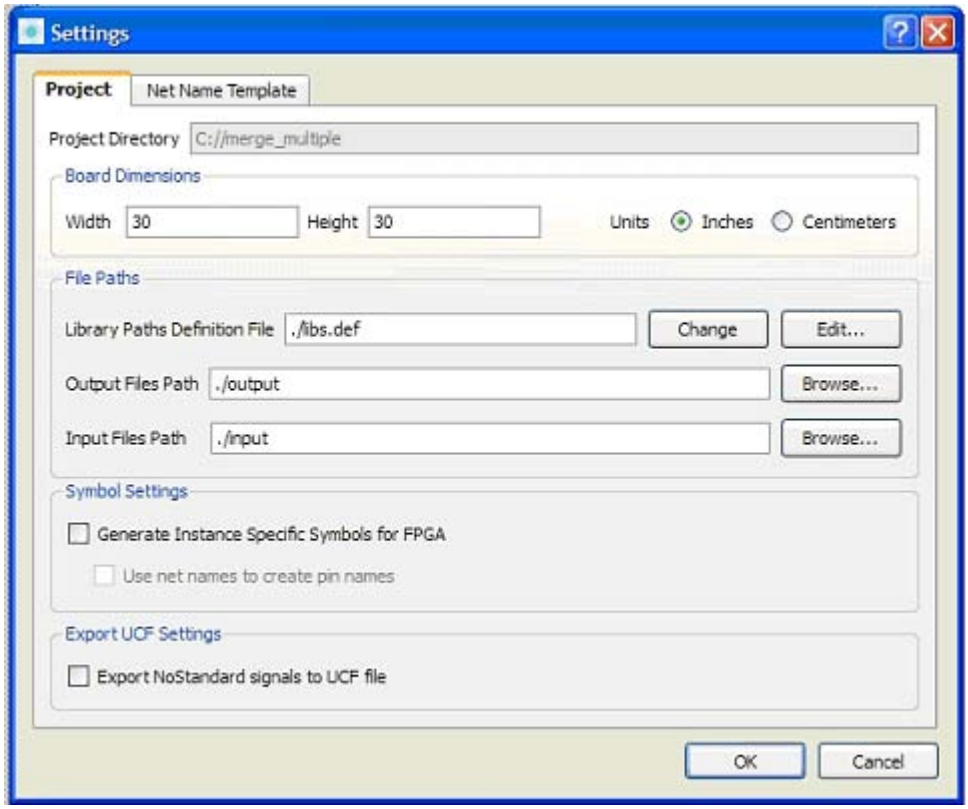
As can be seen from these few steps and figures, splitting and merging a previously-created master design is very easy using the 7Circuits software. Creating a master design by merging previously unrelated designs is discussed in the next section.

Merging Discrete Designs

This section describes how to merge three discrete designs that have never been represented in a master design. This example uses the same Altera FPGAs as used in the previous section.

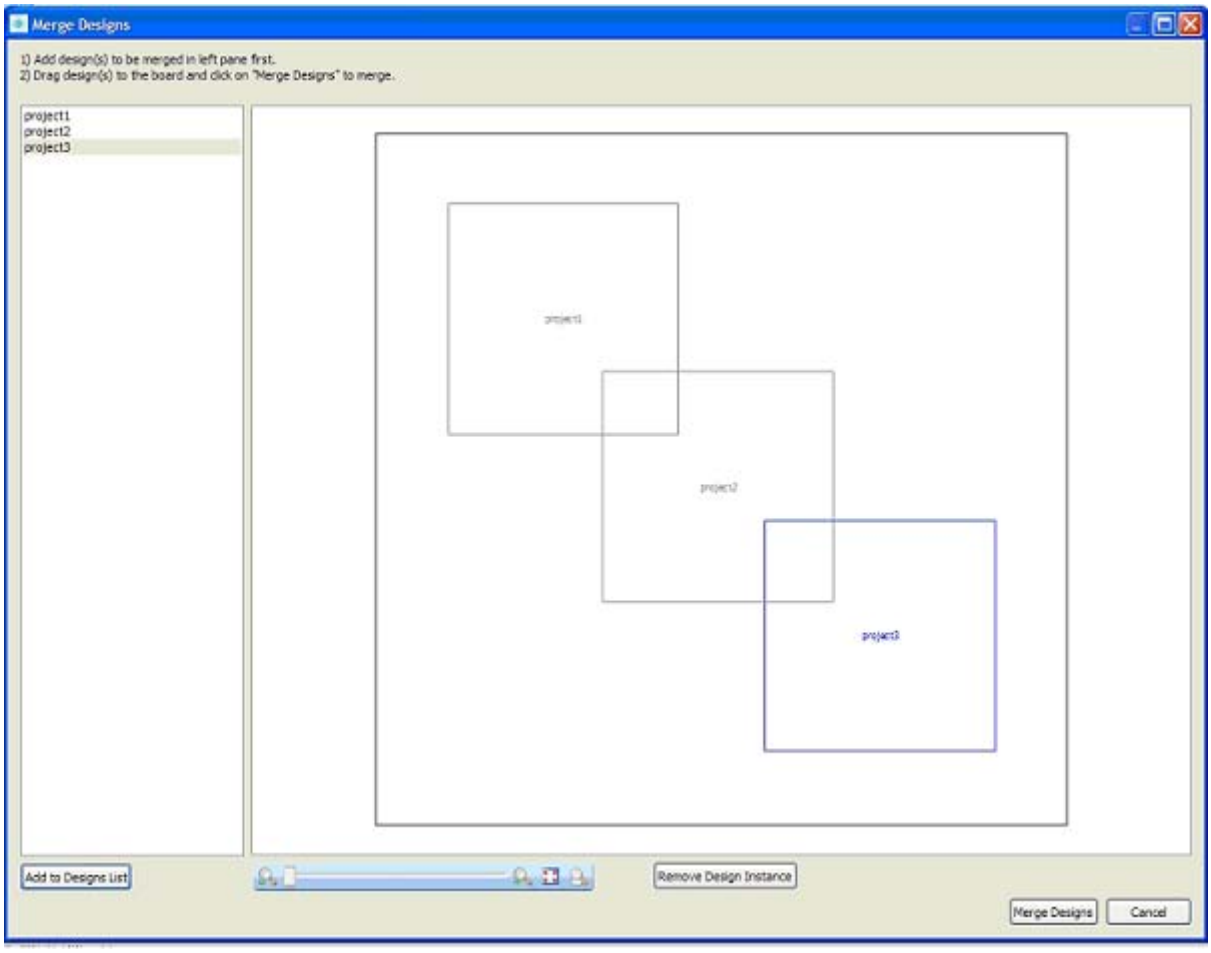
1. On the **File** menu, click **New** to open a new design. The **Settings** dialog box appears any time a new project is created, so that you can change the various parameters of the project.
2. In the **Settings** dialog box, ensure that the canvas is big enough to contain all of the projects that are about to be merged. Change the canvas size to something larger than the 10x10 default, say, 30x30 (Figure 8).
3. Click **OK** to accept your changes.

Figure 8. Project Settings Dialog Box



4. On the **File** menu, select **Merge Different Projects**. Merging discrete designs is done with the **Merge Design** form (Figure 9).
5. Click **Add Designs to List** at the bottom left of the form to add projects. A file browser appears.
6. Using the file browser, locate and select the 7Circuits project files (.scp files). Repeat this step for each design you want to merge into the new project. You can even merge the same project multiple times, allowing you to quickly create a larger design from several smaller blocks of duplicate functionality.

Figure 9. Merge Designs User Interface Form



7. After all designs have been selected and are listed in the left-hand pane of the **Merge Designs** form, drag and drop them into the canvas view.

   The locations of the outlines determine the relative locations of where the design appears in the master design. Only those projects dragged into the right hand window are merged. To delete a project, select it (which highlights the project outline in blue), and click **Remove Design Instance**.

8. After all the designs have been placed on the new canvas, click **Merge Designs**. If any instant- or net-name conflicts exist with the original designs, a dialog box appears and allows you to either manually or automatically resolve the conflicts. You can now save the design and treat it as you would any other.

The result is a master design containing all of the individual designs. Using the techniques described in the previous section, you can now use this design as a master (Figure 10), and can split it and recombine it at any time.

Figure 10. Master Design Created from Individual Projects

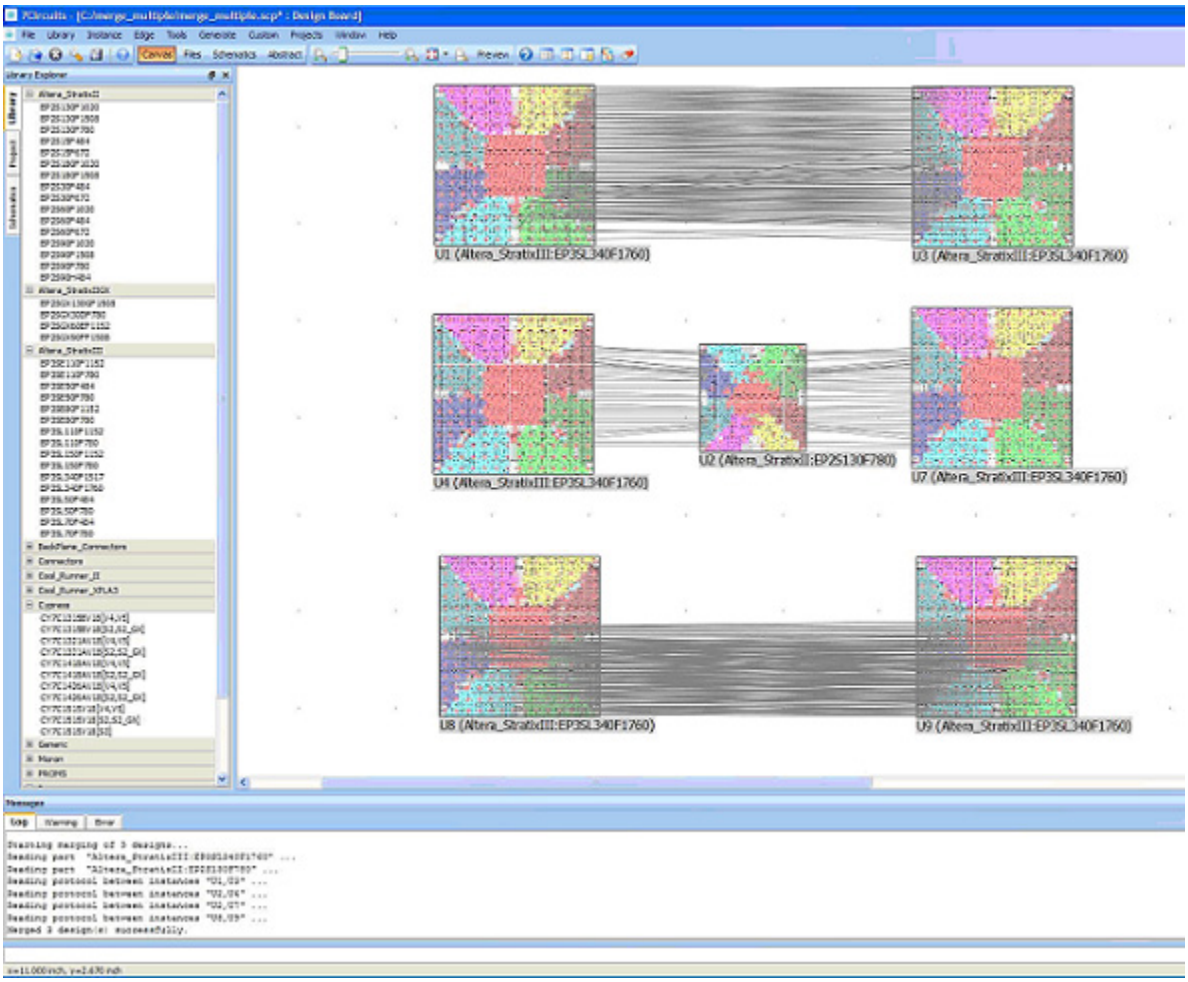
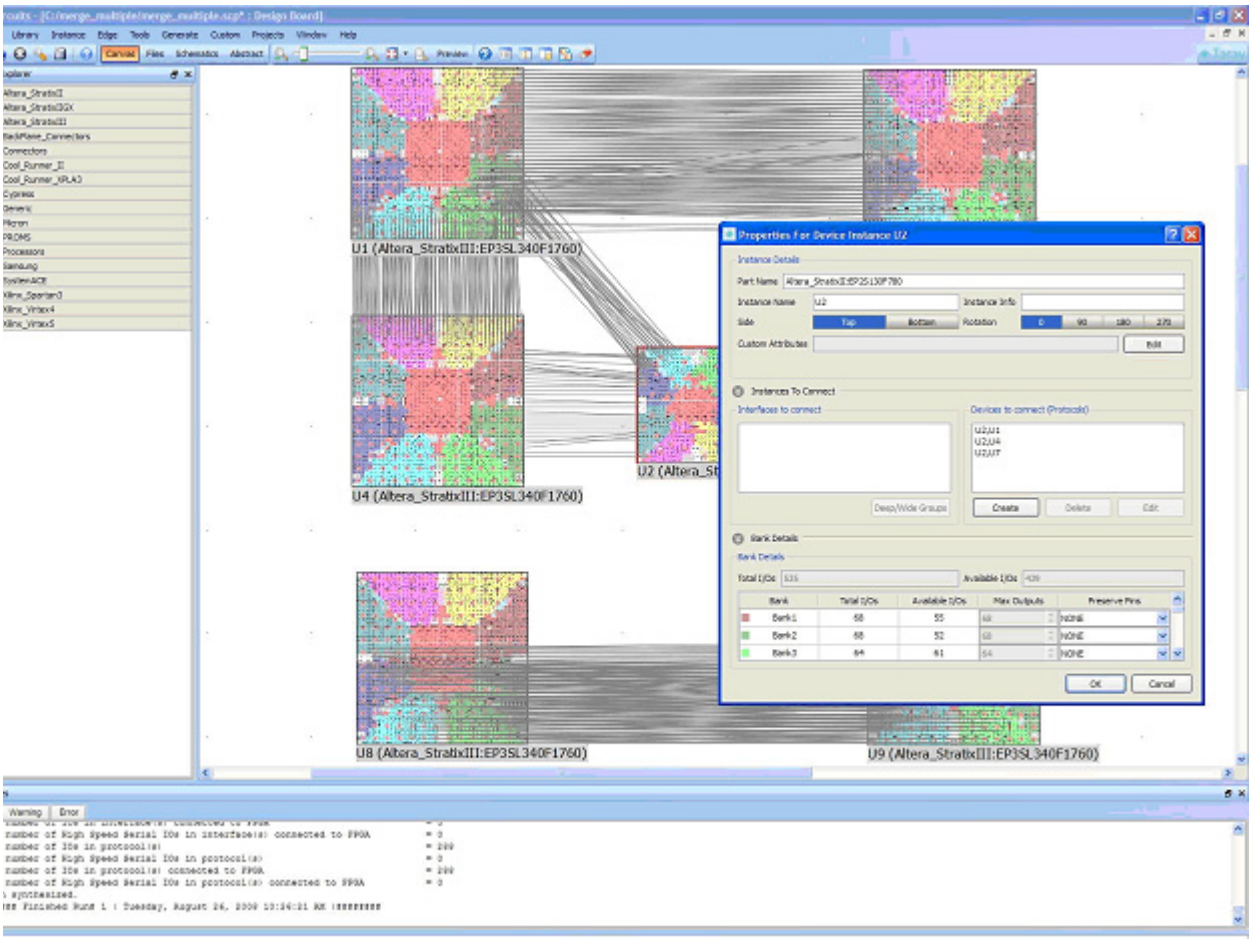


Figure 11 shows the new master design in progress, with further connections made between FPGA U1 at the top left and two other FPGA's, building towards the master design that was used in the initial example for how to split an existing master design.

Figure 11. Adding Connections to New Master Design



Conclusion

The 7Circuits software splitting and merging capabilities allow you to work from the top-down, the bottom-up, or a combination of both techniques, without changing your existing design methodologies. The examples used in this document illustrate how easy it is to work on large designs with multiple team members.

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.0	Initial Release.	—

101 Innovation Drive
San Jose, CA 95134
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Technical Support
www.altera.com/support