AN 542: High Definition (HD) Video Monitoring Reference Design (M5)

Introduction

The Altera® High Definition (HD) Video Monitoring Reference Designs demonstrate the application of Altera tools and devices to broadcast and video surveillance applications.

The reference designs provide a working template that can be used to rapidly build further broadcast applications using a flexible, re-usable and parameterizable video framework. All hardware functions in the reference designs use standard, open interfaces and protocols to facilitate function re-use and system design.

Specifically, the designs use the Altera Video and Image Processing Suite MegaCore® functions library, the SDI MegaCore® function, the DDR2 High Performance Memory Controller MegaCore® function, and supporting development tools.

> For information about these MegaCore functions, refer to the *Video and Image Processing Suite User Guide*, *SDI MegaCore function User Guide*, and *DDR and DDR2 SDRAM High-Performance Controller User Guide*.

The Milestone 5 (M5) release of the reference design demonstrates how to deal with input resolution change of a progressive high-definition (HD) video frame through a downscaling data path.

The downscaled video frame is mixed with a second frame coming from a 1920×1080 HD source in interlaced format (1080i60) that is deinterlaced using the new motion adaptive deinterlacer and downscaled to the same resolution.

You can switch between a multiple view, where both downscaled frames are shown as thumbnails side-by-side on the background layer, and a single view where either of the two frames is shown in its original size.

All the user interaction is performed using switches 1 and 2 of the dual in-line package DIP switch (S3) on the Stratix® II GX development board. Both frames are input over a 3G SDI interface and the mixed result is output via a 1080p60 DVI interface.

Video Design Flow

The M5 reference design provides a simple, yet highly parameterizable, design flow.

Each parameterizable IP block is implemented using standard interfaces:

- Avalon® Streaming (Avalon-ST) interfaces for point-to-point data connections using the Avalon-ST Video protocol

- Avalon® Memory-Mapped (Avalon-MM) for address based read and write transactions

> For information about the Avalon-MM and Avalon-ST interfaces, refer to the *Avalon Interface Specifications*. For information about the Avalon-ST Video protocol, refer to the *Interfaces* chapter in the *Video and Image Processing Suite User Guide*.

These interfaces allow you to rapidly, and cleanly, develop and/or integrate:

    a. video processing data paths

    b. control logic

    c. external memory controllers

The designs are implemented using the Quartus II software, SOPC Builder and the Nios Embedded Development Suite. The SOPC Builder system takes advantage of standard interfaces by presenting an abstracted view of the design, and generating an application specific switch fabric to construct the system. The control logic used is provided as a software project for the Nios II softcore processor.

For information on the Quartus II software and SOPC Builder, refer to the Quartus II online help.

Hardware Requirements

The video monitoring reference design requires the following hardware components:

- Audio Video Development Kit Stratix II GX Edition including:
    - Stratix II GX video development board
    - Digital video interface (DVI), serial digital interface (SDI), and asynchronous serial interface (ASI) inputs and outputs
    - DDR2 DIMM external memory
- A monitor or display with a DVI interface supporting 1,920×1,080 resolution
- One DVI cable to connect the `DVI_TX` output to the monitor
- A SDI source providing 1080i60 output connected to `SDI_IN0`
- A SDI source providing progressive output up to 1080p60 connected to `SDI_IN1`

Software Requirements

The video monitoring reference design is supported on Windows XP only. You must have the following software installed on your PC:
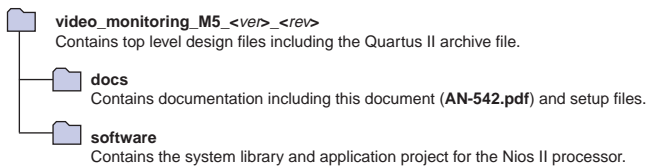
- Quartus II software, v8.0 SP1
- SOPC Builder, v8.0 SP1
- Nios II Embedded Development Suite, v8.0
- MegaCore IP Library, v8.0 SP1 (including the Video and Image Processing Suite, SDI and DDR2 MegaCore functions)
- Update to the IP and IP generation engine. See "Review the Example Design" on page 15 for instructions on updating the 8.0 SP1 installation.

Installing the Reference Design

The reference design is available as a zip file from the Altera Multimedia System Solutions Group.
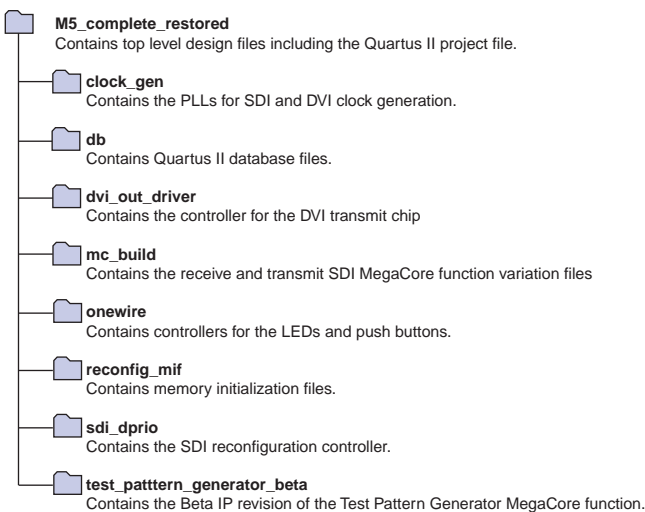
Figure 1 shows the directory structure for the reference design files when they have been extracted from the zip file.

Figure 1. Unzipped Reference Design

video_monitoring_M5_<*ver*>_<*rev*>
Contains top level design files including the Quartus II archive file.

docs
Contains documentation including this document (**AN-542.pdf**) and setup files.

software
Contains the system library and application project for the Nios II processor.

The top level directory contains a Quartus II archive file which can be opened in the Quartus II software. The structure shown in Figure 2 on page 3 is created when you restore the Quartus II project.

Figure 2. Reference Design Directory Structure

M5_complete_restored
Contains top level design files including the Quartus II project file.

clock_gen
Contains the PLLs for SDI and DVI clock generation.

db
Contains Quartus II database files.

dvi_out_driver
Contains the controller for the DVI transmit chip

mc_build
Contains the receive and transmit SDI MegaCore function variation files

onewire
Contains controllers for the LEDs and push buttons.

reconfig_mif
Contains memory initialization files.

sdi_dprio
Contains the SDI reconfiguration controller.

test_patttern_generator_beta
Contains the Beta IP revision of the Test Pattern Generator MegaCore function.

Tool Flow

The SOPC Builder system has four main external connections as shown in Figure 3 on page 4:

■ Video input from an external video interface. The connection to the external video interface is made using a parameterizable video conversion IP function. The IP function provides a bridge between a clocked video interface (such as a SDI MegaCore function) and the Avalon-ST flow controlled domain.

■ Video output to an external video interface. The connection to the external video interface is done using a parameterizable video conversion IP function. The IP function provides a bridge between the Avalon-ST flow controlled domain and a clocked video interface (such as DVI).

■ Connection to an external memory interface. This connection uses a DDR2 SDRAM Controller MegaCore function. SOPC Builder generates the application specific switch fabric to arbitrate between multiple masters trying to access the controller.

■ Connection to a control block. This block handles the run-time configuration of the Video and Image Processing MegaCore functions as a response to an input resolution or frame rate change, or user interaction via the DIP switches on the development board. All of the control block functionality is implemented in software running on a Nios® II processor.

Figure 3. Tool Flow Block Diagram
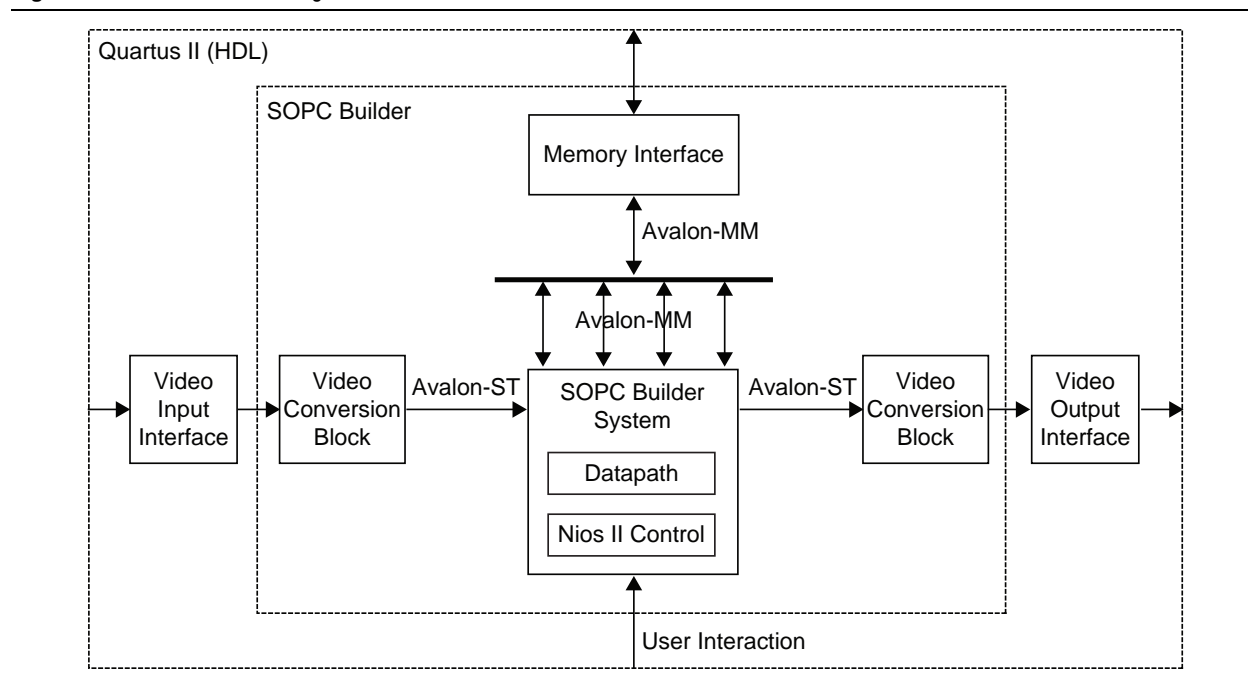
SOPC Builder

SOPC Builder provides an abstracted design environment that simplifies the process of system design, including the datapath, control logic and external memory integration.

All the connections in the SOPC Builder system use Avalon-ST and Avalon-MM interfaces. SOPC Builder provides arbitration for multiple Avalon-MM masters accessing a single memory interface.

The parameterizable video conversion MegaCore functions interface to the Datapath block with the standard Avalon-ST interface, using the same video protocol used by the Video and Image Processing Suite MegaCore functions.

Refer to the *Interfaces* chapter in the Video and Image Processing Suite User Guide for a full description of this protocol.

The Datapath block in Figure 3 contains multiple Video and Image Processing Suite MegaCore functions that are used to perform common video processing functions, including scaling, mixing, deinterlacing, chroma resampling, and color space conversion. The Datapath block also contains a parameterizable Frame Buffer MegaCore function that provides a convenient function for double or triple buffering data in external memory and supporting system rate changes.The MegaCore function GUIs are used to configure these functions in SOPC Builder.

The `SOPC Builder System` includes a Nios II processor subsystem which includes standard peripherals such as timers, and I/O interfaces.

Quartus II

The SOPC Builder system is connected to the external video interfaces (implemented by a SDI MegaCore Function and DVI Controller) using HDL. Pin assignments and I/O constraints are set in the Quartus II software. The Quartus II project file is **M5_complete.qpf**.

# Features

The Video Monitoring Reference Design is provided as a Quartus II project supporting:

■ One background layer in format R′G′B, 4:4:4, consisting of a color bar.

■ One 3G 1080i60 (1920×1080, interlaced) SDI input as source 1 (stream 1).

■ One 3G SDI input (progressive and variable resolution between 640×360 and 1920×1080) as source 2 (stream 2).

■ Chroma upsampling from 4:2:2 to 4:4:4 for both stream 1 and stream 2.

■ Color Space conversion of both streams from Y'CbCr to R'G'B'.

■ Deinterlacing of stream 1 using the motion adaptive deinterlacer.

■ Downscaling of both stream 1 (1920×1080) and stream 2 (variable) to 640×360 using frame buffers to support data throughput changes and synchronization.

■ Reconfiguration of the stream 2 data processing path at run-time as a result of resolution or frame rate change at source 2.

■ Three mixing modes (selected by DIP switch S3) using the Alpha Blending Mixer:

   ■ Thumbnail view (DIP1 =0): Downscaled streams 1 and 2 side-by-side on the graphical layer (see Figure 4).

Figure 4. Alpha Blending Mixer Thumbnail View
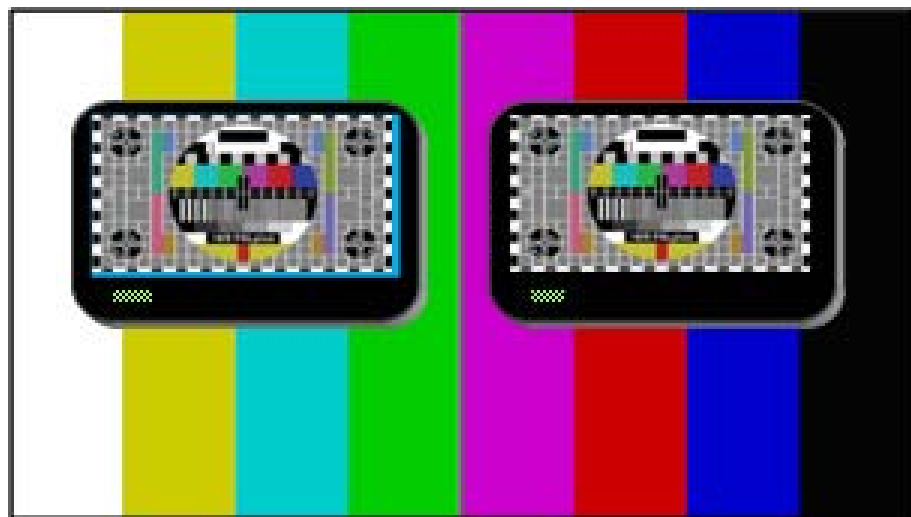
■ Video view (DIP1=1 and DIP2 =0): Stream 1 in original size (see Figure 5).

Figure 5. Alpha Blending Mixer Video View (Stream 1)
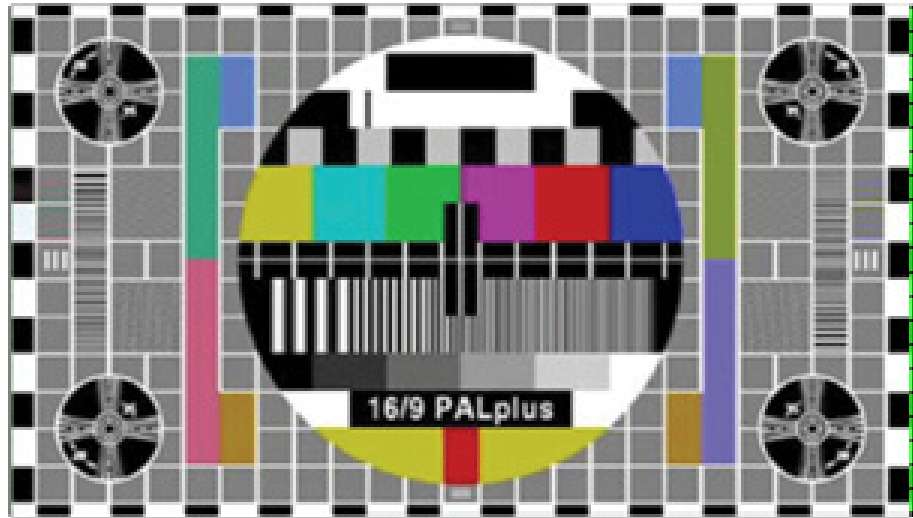
■ Video view (DIP1=1 and DIP 2 = 1): Stream 2 in original size (see Figure 6).

Figure 6. Alpha Blending Mixer Video View (Stream 2)

■ One 1080p60 (1920×1080) DVI output.

Design Description

Figure 7 on page 7 shows a block diagram of the Video Monitoring Reference Design system.

Figure 7. System Block Diagram
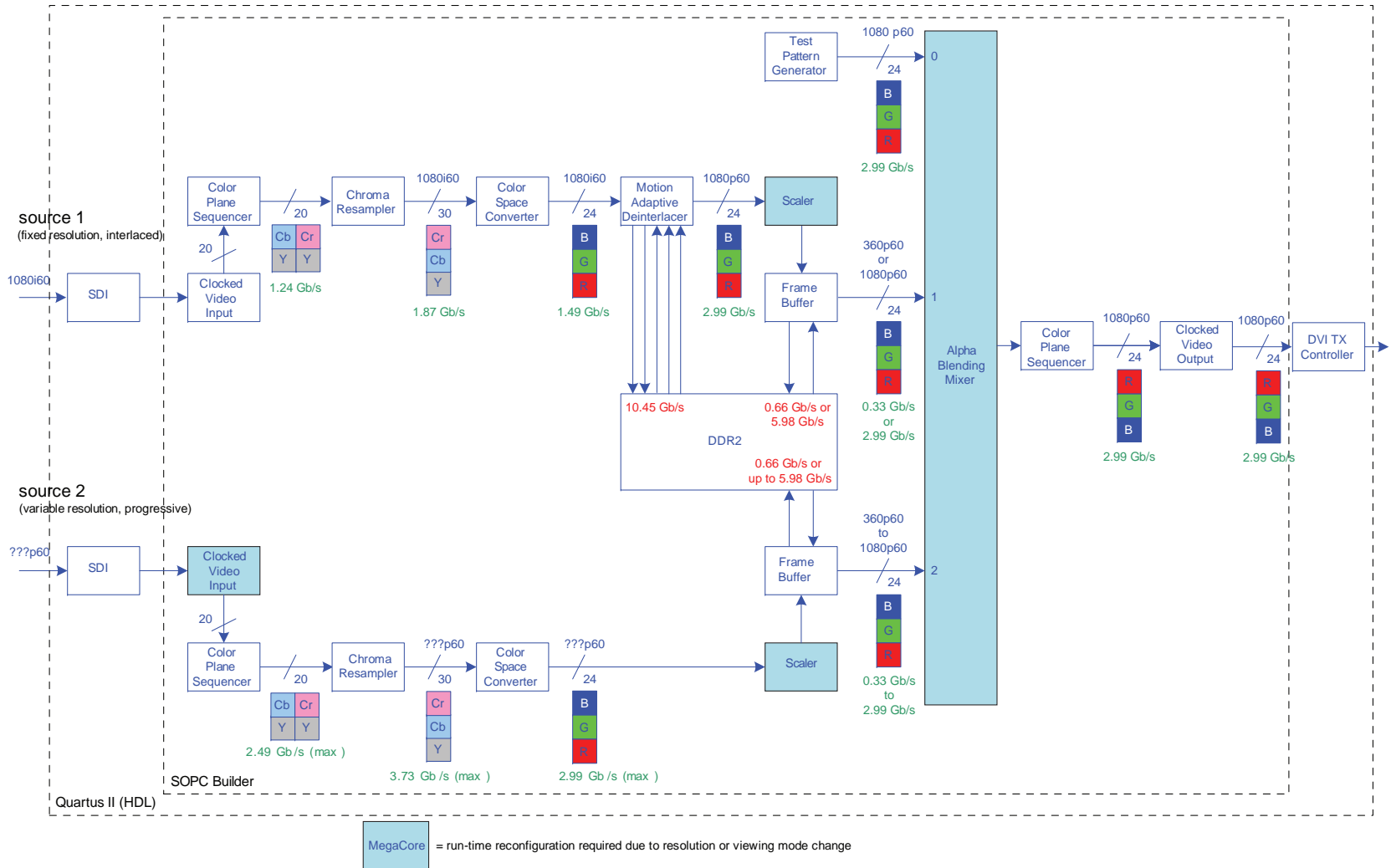
Notes to Figure 7:

(1) 360p60 means 640×360 progressive @ 60 Hz.

(2) The shaded blocks in the data path from source 2 require run-time configuration due to possible resolution change at the input.

Block Descriptions

The following blocks are used in the Video Monitoring reference design:

SDI MegaCore Function

The SDI MegaCore function is configured as a triple rate receiver serial digital interface. Two instances are required, one for each source. The SDI input clock frequency is 148.5 MHz for 3Gb/s HD or 74.25 MHz for 1.5Gb/s HD video inputs, and 27.0 MHz for SD video inputs. In this design, a clock frequency of 148.5 MHz is used.

For more information about the SDI MegaCore function, refer to the *SDI MegaCore Function User Guide*.

Clocked Video Input MegaCore Function

The Clocked Video Input MegaCore function converts a clocked video input to the Avalon-ST Video protocol used by the Video and Image Processing Suite MegaCore functions (removing blanking information). This block provides clock domain crossing that allows the image stream to run at a different frequency to the video input.

It has the following features:

- Support for sequential and parallel color planes (different data widths and formats)

- Support for different data streams:

    - BT656 (Composite or SD, HD & 3G SDI)

    - RGB (DVI)

- Configurable FIFO size

- Support for clock domain crossing

- Feedback about FIFO over/underflow

Two instances of the Clocked Video Input block are required, one for each video stream. Both instances are configured for:

- 20-bit HD SDI (BT656) input

- FIFO depth of two 1080p lines. Each line contains 1,920 samples giving a FIFO depth of one 1080p line and a width of 20 bits (9.4Kbit)

- Both input streams have run-time control enabled

For more information about the Clocked Video Input MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Color Plane Sequencer MegaCore Function

Three instances of the Color Plane Sequencer MegaCore function are required (in stream 1, stream 2 and the output stream).

The MegaCore functions in stream 1 are configured to swap the luminance (Y') and color (CbCr) components.

The MegaCore function in the output stream is configured to swap the red (R') and blue (B') components.

For more information about the Color Plane Sequencer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Chroma Resampler MegaCore Function

Two instances of the Chroma Resampler MegaCore Function are required. Both instances are configured for:

■ Input of two 10-bit color planes in parallel (Y' and alternating Cb or Cr), 4:2:2

■ Output of three10-bit color planes in parallel, 4:4:4

■ Luma adaptive algorithm for horizontal resampling

Resolution changes for both streams are handled by control packets in the Avalon-ST Video protocol.

For more information about the Chroma Resampler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Color Space Converter MegaCore Function

Two instances of the Color Space Converter MegaCore function are required. Both instances are configured for:

■ Input of three 10-bit color planes in parallel (Y'CbCr)

■ Output of three 8-bit color planes in parallel (R'G'B')

■ Y'CbCr: HDTV to Computer R'G'B' coefficients

Stream 1 has the resolution fixed as 1920×1080.

Stream 2 is set to a maximum resolution of 1920×1080.

For more information about the Color Space Converter MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Deinterlacer MegaCore Function

The Deinterlacer MegaCore function is configured for:

■ Fixed resolution of 1920×1080

■ Input of three 8-bit color planes in parallel (R'G'B') at 1080i60

■ Output of three 8-bit color planes in parallel (R'G'B') at 1080p60

■ Motion-adaptive deinterlacing method

■ Double-buffering with Avalon-MM port width set to 256 bits

■ Output frame rate set as input field rate

For more information about the Deinterlacer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Scaler MegaCore Function

Two instances of the Scaler MegaCore function are required. Both instances are configured for:

■ Input and output of three 8-bit color planes in parallel (R'G'B')

■ Run-time control used to change output resolution depending on the viewing mode

■ Polyphase mode with 12×12 taps and Lanczos-2 coefficients

Both Stream 1 and Stream 2 have run-time control turned on with the maximum output resolution set to 1920×1080.

For more information about the Scaler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Frame Buffer MegaCore Functions

The Frame Buffer MegaCore function takes image stream frames and buffers them into memory using an Avalon-MM connection (in this case DDR2 memory). The Frame Buffer can also drop or repeat frames where necessary to smooth out the data flow. This block has the following features:

■ Parameterizable GUI

■ Support for different frame width/heights

■ Support for different sequential/parallel color planes and different data widths

■ Support for different memory data widths

■ Support for run-time control

Two instances of the Frame Buffer MegaCore function are required, one for each input stream. All instances are configured for:

■ 24-bit wide Avalon-ST source and sink

■ Three 8-bit color planes in parallel

■ 256-bit wide Avalon-MM read and write masters (for 64-bit DDR2)

The first input stream is configured for:

■ Resolution set by control packets with maximum resolution of 1920×1080

■ Neither frame dropping nor frame repeating allowed

The second input stream is configured for:

■ Resolution set by control packets with maximum resolution of 1920×1080

■ Both frame dropping and frame repeating allowed

For more information about the Frame Buffer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

DDR2 SDRAM High Performance Controller MegaCore Function

This is the controller block for the external DDR2 SDRAM required as buffer for the Deinterlacer and the three Frame Buffers described above. It is configured for:

■ Micron MT9HF6472AY-5EB38 (72-bit, 512MByte, 533MT/s, CL4, 266.7MHz)

■ Data width set to use 64 bits (SOPC Builder cannot handle non power of 2 data widths)

■ Memory set up in Half-Rate mode (266.7MHz internally, 133.35MHz externally)

For more information about the DDR2 SDRAM High Performance Controller MegaCore Function, refer to the *DDR and DDR2 SDRAM High Performance Controller User Guide*.

Test Pattern Generator (Beta) MegaCore Function

This block generates a color bar which is used as the background layer for the Alpha Blending Mixer. It is configured for:

■ Resolution 1920×1080

■ 8 bits per color plane in parallel

■ R′G′B

■ 4:4:4

■ Progressive output

Alpha Blending Mixer MegaCore Function

This block mixes three input layers under software control at run-time. It is configured for:

■ Three input layers:

   ■ Layer 0 (background) - 1920×1080, color bar.

   ■ Layer 1 (stream 1) - 1920×1080 or 640×360, output from scaler depending on viewing mode.

   ■ Layer 2 (stream 2) - 640×360, output from run-time configurable scaler or variable resolution output of scaler depending on viewing mode.

■ 1920×1080 output mixed according to three modes (see Figure 4 on page 5, Figure 5 on page 6 and Figure 6 on page 6):

   ■ Thumbnail view: Layers 1 and 2 side-by-side at size 640×360 on layer 0.

   ■ Video view (Stream 1): Layer 1 only in original resolution.

   ■ Video view (Stream 2): Layer 2, with some of the background (layer 0) visible if the resolution of stream 2 is less than 1920×1080.

For more information about the Alpha Blending Mixer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Control Block (Nios II Processor)

This block is based on a Nios II embedded processor connected to DDR2-SDRAM, together with the Video and Image Processing Suite MegaCore functions, through an Avalon-MM master. The Control block initializes the run-time reconfigurable blocks at startup, after mode change as caused by user interface interaction, or when a resolution change is detected.

Clocked Video Output MegaCore Function

The Clocked Video Output MegaCore function takes an Avalon-ST video stream and converts it to a clocked video stream (reconstructing blanking information). This block provides clock domain crossing that allows the Avalon-ST image stream to run at a different frequency to the clocked video output. It has the following features:

■ Compile time parameterizable GUI

■ Support for sequential and parallel color planes (different data widths and formats)

■ Support for different data streams:

    ■ BT656 (Composite or SD, HD & 3G SDI)

    ■ RGB (DVI)

■ Configurable FIFO size

■ Supports clock domain crossing

■ Feedback about FIFO over/underflow

The Clocked Video Output block is configured for:

■ 24-bit DVI (RGB) output

■ Video input and output use the same clock

■ Run-time control enabled

■ FIFO depth of 1 1080p line. This gives a FIFO depth of 1,920 and a width of 20 bits (9.4Kbit)

For more information about the Clocked Video Output MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

DVI TX Controller

The DVI TX Controller controls the DVI transmitter block on the Stratix II GX Audio Video development board to output the video stream. This block provides:

■ Compile time parameterizable HDL

■ Support for different resolutions (720p30/60 and 1080p30/60)

The DVI TX Controller block is configured for:

■ 24-bit (RGB), 1080p60 (1920×1080) output

■ 148.5MHz output frequency

Clock Domains

The Nios II processor runs at 100MHz while the memory controller subsystem runs at 133.35MHz. The remainder of the SOPC Builder system, including the video datapath, run at 148.5MHz.

The DDR2 memory runs at its maximum rate of 266MHz. This requires the memory controller to run in half-rate mode.

The Clocked Video Input and Clocked Video Output blocks provide clock domain crossing which allows the DVI output and SDI input to run at the speed of the relevant standard being used.

Clock domain crossing is also used in the Deinterlacer and the Frame Buffers, as the Avalon-ST based data path runs at 148.5MHz, while the Avalon-MM based memory connections run at 133.35 MHz.

Reconfiguration Sequence

When the resolution changes at the input of video stream 2, the Nios II processor updates the scaler output resolution based on the new resolution that is read from the Clocked Video Input block.

All other resolution updates are handled by Avalon-ST Video control packets that are transmitted from block to block in addition to the video data.

Memory Bandwidth Calculations

Access to external memory is required (through the DDR2 SDRAM High Performance Memory Controller) for the Motion Adaptive Deinterlacer (five masters), and the two Frame Buffers (two masters each).

Motion Adaptive Deinterlacer

- Input format: 1080i60
  $1920 \times 1080 \times 24bits \times 60/2s = 1.493Gbit/s$

- Output format: 1080p60
  $1920 \times 1080 \times 24bits \times 60 = 2.986Gbit/s$

- Memory access:
  $1 \times$ write at input rate: 1.493Gbit/s
  $1 \times$ write at 1/2 output rate: 1.493Gbit/s
  $1 \times$ read at 1/2 output rate: 1.493Gbit/s
  $2\times$ read at output rate: 5.972Gbit/s

- Total: 10.451Gbit/s

Frame Buffer 1 (Stream 1 after Scaling)

- Input format: 640×360 (multiview) or 1920×1080 (single view) progressive at 60Hz
  Minimum: $640 \times 360 \times 24bits \times 60/s = 0.332Gbit/s$
  Maximum: $1920 \times 1080 \times 24bits \times 60/s = 2.986Gbit/s$:

- Output format: 640×360 (multiview) or 1920×1080 (single view) progressive at 60Hz
  Minimum: $640 \times 360 \times 24bits \times 60/s = 0.332Gbit/s$
  Maximum: $1920 \times 1080 \times 24bits \times 60/s = 2.986Gbit/s$

- Memory access:
  - 1 × write at input rate: Either 0.332Gbit/s or 2.986Gbit/s
  - 1 × read at output rate: Either 0.332Gbit/s or 2.986Gbit/s

- Total (per frame buffer):   Either 0.664Gbit/s or 5.972Gbit/s

Frame Buffer 2 (Stream 2 after Scaling)

- Input format: Between 640×360 and 1920×1080 progressive at 60Hz
  Minimum: $640 \times 360 \times 24bits \times 60/s = 0.332Gbit/s$
  Maximum: $1920 \times 1080 \times 24bits \times 60/s = 2.986Gbit/s$

- Output format: Between 640×360 and 1920×1080 progressive at 60Hz
  Minimum: $640 \times 360 \times 24bits \times 60/s = 0.332Gbit/s$
  Maximum: $1920 \times 1080 \times 24bits \times 60/s = 2.986Gbit/s$

- Memory access:
  - 1 × write at input rate: Between 0.332Gbit/s and 2.986Gbit/s
  - 1 × read at output rate: Between 0.332Gbit/s and 2.986Gbit/s

- Total (per frame buffer):   Between 0.664Gbit/s and 5.972Gbit/s

Total Bandwidth

- Deinterlacer: 10.451Gbit/s

- Frame Buffer 1:   0.664Gbit/s or 5.972 Gbit/s

- Frame Buffer 2:   Between 0.664Gbit/s and 5.972Gbit/s

- Total: Between 11.78Gbit/s and 16.42Gbit/s

☞ For the calculation of the maximum total bandwidth, only the Deinterlacer and one Frame Buffer are taken into account as the other Frame Buffer does not access external memory in single viewing mode when the maximum bandwidth is required.

The Stratix II GX development board when used with the Micron MT9HTF6472AY-53EB3 high-performance DDR2 SDRAM provides a maximum theoretical bandwidth of:

266.7 MHz × 64 bits × 2 (both clock edges used) = 34.133 Gbit/s

This results in a memory access efficiency requirement of up to 48%.

Memory bandwidth efficiency is determined by a number of factors, such as randomness of addresses, refresh rate, turnaround times between reads and writes, and burst lengths.

Altera's memory controllers can reach an efficiency of up to about 90% if the access conditions are right (long bursts of writes to the same column followed by long bursts of reads).

The use of a half-rate memory controller in order to satisfy the memory bandwidth requirements means that the local interface width between memory controller and internal FPGA logic is 256 bits (= 4 × 64 bits).

Both DDR2 memory and memory controller will run at 266MHz, while the internal FPGA blocks will run at half this rate, that is, 133MHz.

Replacing the SDI Input with DVI

An all DVI system is much simpler and can be produced by the following steps:

1. Replace the SDI MegaCore function with a DVI RX Controller.

2. Configure the Clocked Video Input MegaCore function for the DVI input.

3. Remove the Chroma Resampler and Color Space Converter MegaCore functions.

4. Regenerate the SOPC Builder system and recompile the Quartus II project.

Review the Example Design

This section describes how you can open the High Definition (HD) Video Monitoring Reference Design components in SOPC Builder.

To review the complete High Definition (HD) Video Monitoring Reference Design in SOPC Builder perform the following steps:

1. Run the Quartus II software to ensure the *QUARTUS_ROOTDIR* environment variable is correctly set.

2. Close the Quartus II software.

3. In Windows Explorer, browse to *<install directory>***docs** and double-click on **setup.bat** to install the Video and Image Processing toolkit blocks.

4. Re-open the Quartus II software.

5. Choose Open Project (File menu), browse to the *<install directory>* and select the Quartus II archive file: **M5_complete.qar**.

6. Click **OK** to open the restored project **(M5_complete.qpf)** and update the included file information.

7. Copy the file **tpg.ipx** from *<install_directory>***docs** to into the Quartus II project directory (for example, **M5_complete_restored** if you use the default name). This makes the Test Pattern Generator (Beta) MegaCore function available in SOPC Builder.

8. Choose **SOPC Builder** from the Tools menu in the Quartus II software.

☞ If any there are any blocks are missing from your SOPC Builder project, check that step 3 completed without errors. If necessary, you can add any missing directories to your IP Search Path by choosing **Options** from the Tools menu in SOPC Builder.

The complete SOPC Builder design is shown in (Figure 8 on page 16, Figure 9 on page 17, and Figure 10 on page 18).

Clock Settings

Name	Source	MHz
clk	External	100.0
altmemddr_sysclk	altmemddr.sysclk	133.333499
altmemddr_auxfull	altmemddr.auxfull	266.666999
altmemddr_auxhalf	altmemddr.auxhalf	133.333499

Target — Device Family: Stratix II GX

Use	Connections	Module Name	Description	Clock	Base	End	IRQ
☑		⊟ **my_alt_vip_cti_1**	Clocked Video Input				
		control	Avalon Memory Mapped Slave	**vip_clk**	0x00000000	0x000000ff	
		dout	Avalon Streaming Source				
☑		⊟ **my_alt_vip_cpr_1**	Color Plane Sequencer				
		din0	Avalon Streaming Sink	**vip_clk**			
		dout0	Avalon Streaming Source				
☑		⊟ **my_alt_vip_crs_1**	Chroma Resampler				
		din	Avalon Streaming Sink	**vip_clk**			
		dout	Avalon Streaming Source				
☑		⊟ **my_alt_vip_csc_1**	CSC				
		din	Avalon Streaming Sink	**vip_clk**			
		dout	Avalon Streaming Source				
☑		⊟ **my_alt_vip_dil_1**	Deinterlacer				
		write_master	Avalon Memory Mapped Master	altmemddr...			
		read_master_0	Avalon Memory Mapped Master	altmemddr...			
		read_master_1	Avalon Memory Mapped Master	altmemddr...			
		din	Avalon Streaming Sink	**vip_clk**			
		dout	Avalon Streaming Source				
		motion_write_master	Avalon Memory Mapped Master	altmemddr...			
		motion_read_master	Avalon Memory Mapped Master	altmemddr...			
☑		⊟ **my_alt_vip_scl_1**	Scaler				
		din	Avalon Streaming Sink	**vip_clk**			
		dout	Avalon Streaming Source				
		control	Avalon Memory Mapped Slave		0x00013a80	0x00013aff	
☑		⊟ **my_alt_vip_vfb_1**	Frame Buffer				
		din	Avalon Streaming Sink	**vip_clk**			
		dout	Avalon Streaming Source				
		read_master	Avalon Memory Mapped Master	altmemddr...			
		write_master	Avalon Memory Mapped Master	altmemddr...			
☑		⊟ **my_alt_vip_cti_2**	Clocked Video Input				
		control	Avalon Memory Mapped Slave	**vip_clk**	0x00013800	0x000138ff	1
		dout	Avalon Streaming Source				
☑		⊟ **my_alt_vip_cpr_2**	Color Plane Sequencer				
		din0	Avalon Streaming Sink	**vip_clk**			
		dout0	Avalon Streaming Source				
☑		⊟ **my_alt_vip_crs_2**	Chroma Resampler				

Remove | Edit... | ▲ Move Up | ▼ Move Down | Address Map... | Filter...

Figure 9. Video Monitoring Reference Design in SOPC Builder (Part 2 of 3)

Figure 10. Video Monitoring Reference Design in SOPC Builder (Part 3 of 3)

Building the Software in the Nios II IDE

Perform the following steps to build the software in the Nios II Integrated Development Environment (IDE):

1. Start the Nios II IDE, v8.0 software.

2. Choose **Switch Workspac**e from the File menu and browse to the **software** subdirectory of the M5 design install directory.

Figure 11. Nios II IDE Workspace Launcher
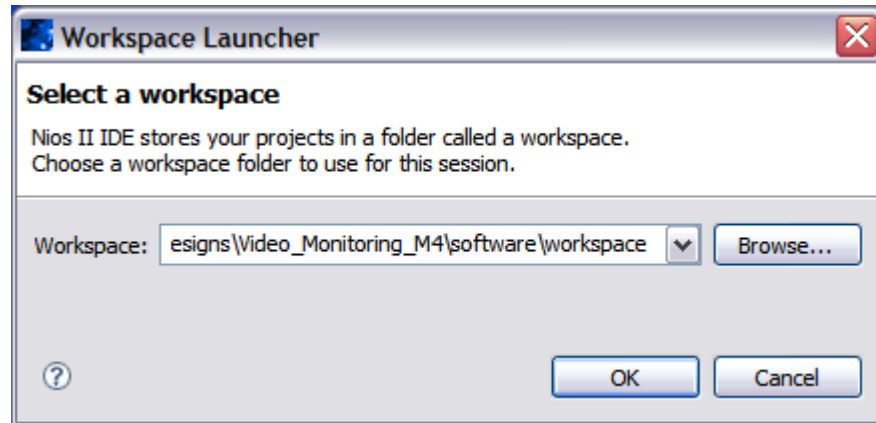
3. Add workspace to the end of the path name and click **OK** to create a new workspace.

4. Choose **Import** from the File menu and click on **Altera Nios II** in the Import dialog box. Choose **Existing Nios II IDE project into workspace** and click **Next**.

5. Browse to the application project (**m5_controller**) and click **Finish**.

6. Repeat step 4 for the library project (**m5_syslib**) and click **Finish**.

7. Browse to the PTF file (**data_path.ptf**) in the (**M5_complete_restored**) Quartus II project directory and confirm that cpu appears in the **CPU** field. Click **Finish** to import the project from the file system.

8. Check that the application project (**m5_controller**) and system library project (**m5_syslib**) are shown in the workspace (Figure 12 on page 20).

9. Browse the application source code listed below **m5_controller**.

10. Right click on **m5_controller** and choose **System Library Properties** to browse the library properties.

11. Right click on **m5_controller** and select **Build Project**. Confirm that the **debug** directory (containing the **m5_controller.elf** file) appears after a few minutes.

12. After programming the development board with hardware, right click on **m5_controller** and select **Run As->Nios II Hardware** to download the control software.

☞ The default software is already included in the .**sof** and .**pof** files.

Figure 12. Nios II Integrated Development Environment (IDE) Workspace
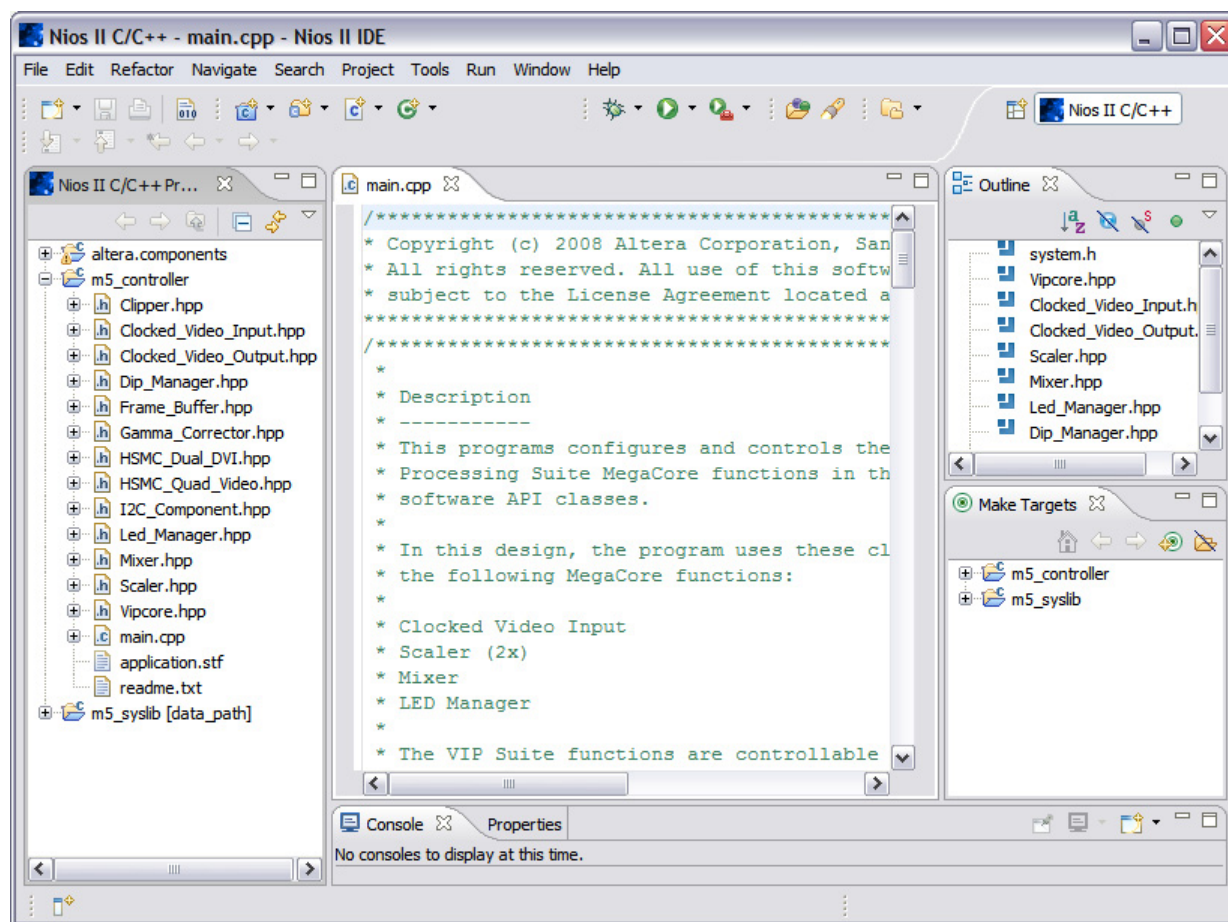
Conclusion

The High Definition (HD) Video Monitoring Reference Design demonstrate a re-usable and flexible video framework for rapid development of video and image processing designs.

The use of standard open interfaces and protocols throughout the system allows you to build further applications, by re-using parameterizable IP from the Altera IP library or by adding your own IP to the framework.

The video framework does not preclude use of HDL to connect the IP components. However, the HD Video Monitoring Reference Designs demonstrate that the SOPC Builder environment significantly accelerates system design by:

■ Automatic generation of an application specific switch fabric and ability to insert a custom priority arbitration scheme.

■ Providing an abstracted view of the video system.

■ Detecting and displaying Altera and user IP in an immediately accessible form.

Revision History

Table 1 shows the revision history for the *AN-542: High Definition (HD) Video Monitoring Reference Design M5* application note.

Table 1. AN-542 Revision History

Version	Date	Errata Summary
1.2	November 2008	Updated the bandwidth calculations and block diagram.
1.1	September 2008	Updated the bandwidth calculations.
1.0	July 2008	First release of this application note.

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